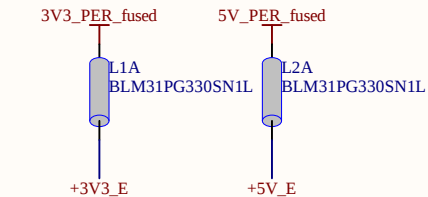
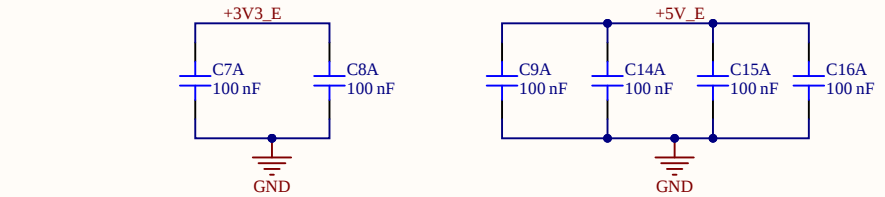
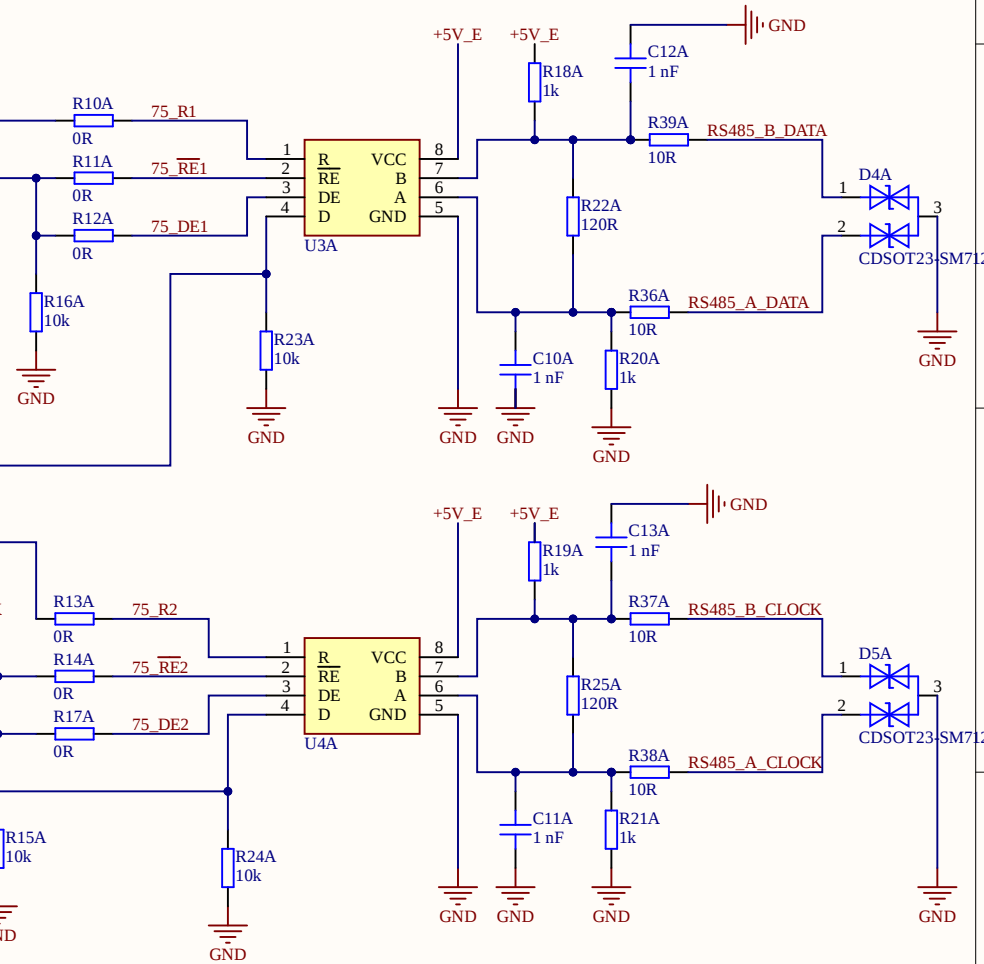
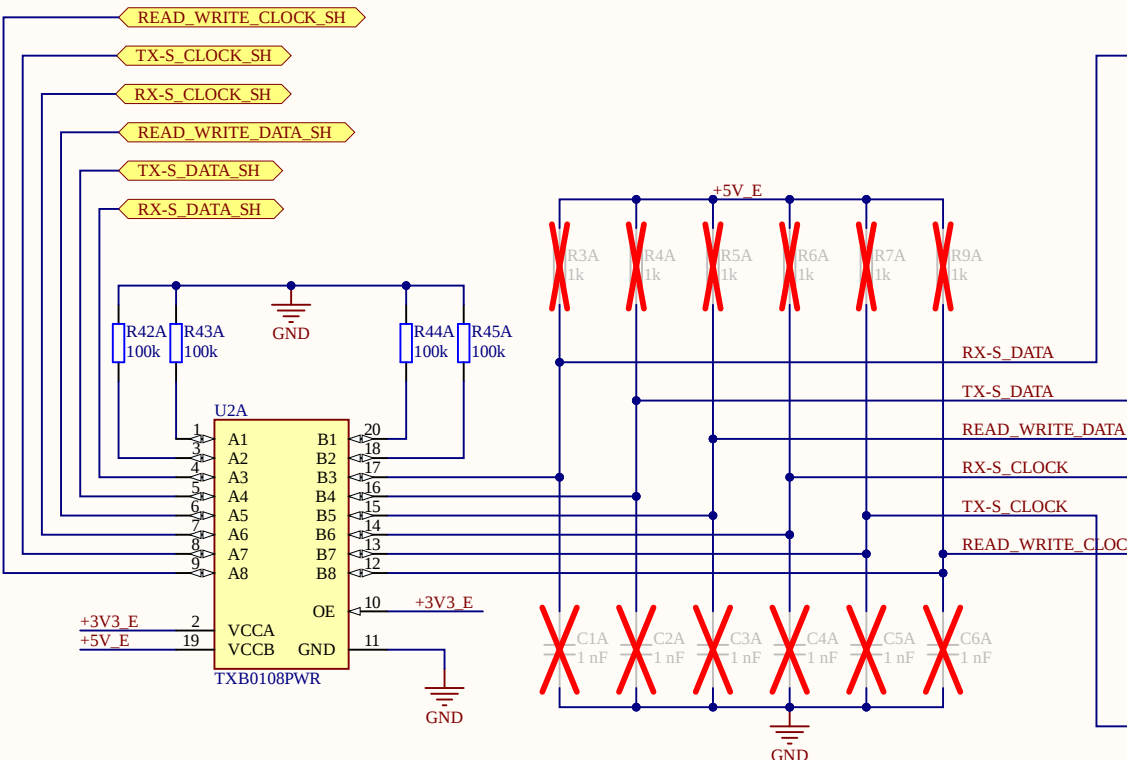
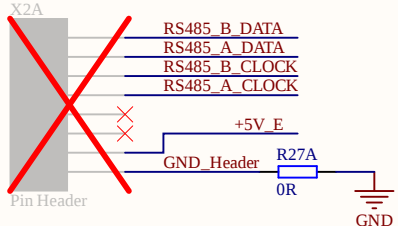
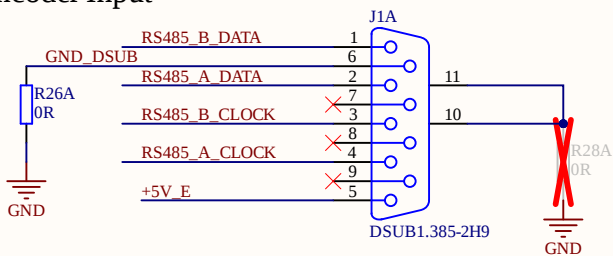


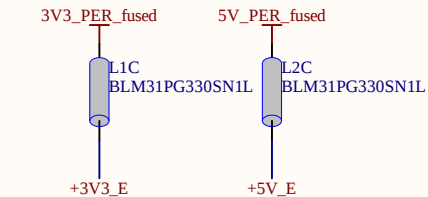
Power Supply Encoder



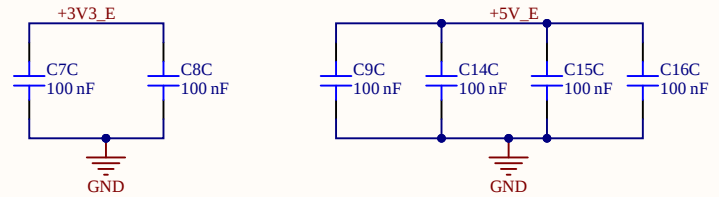
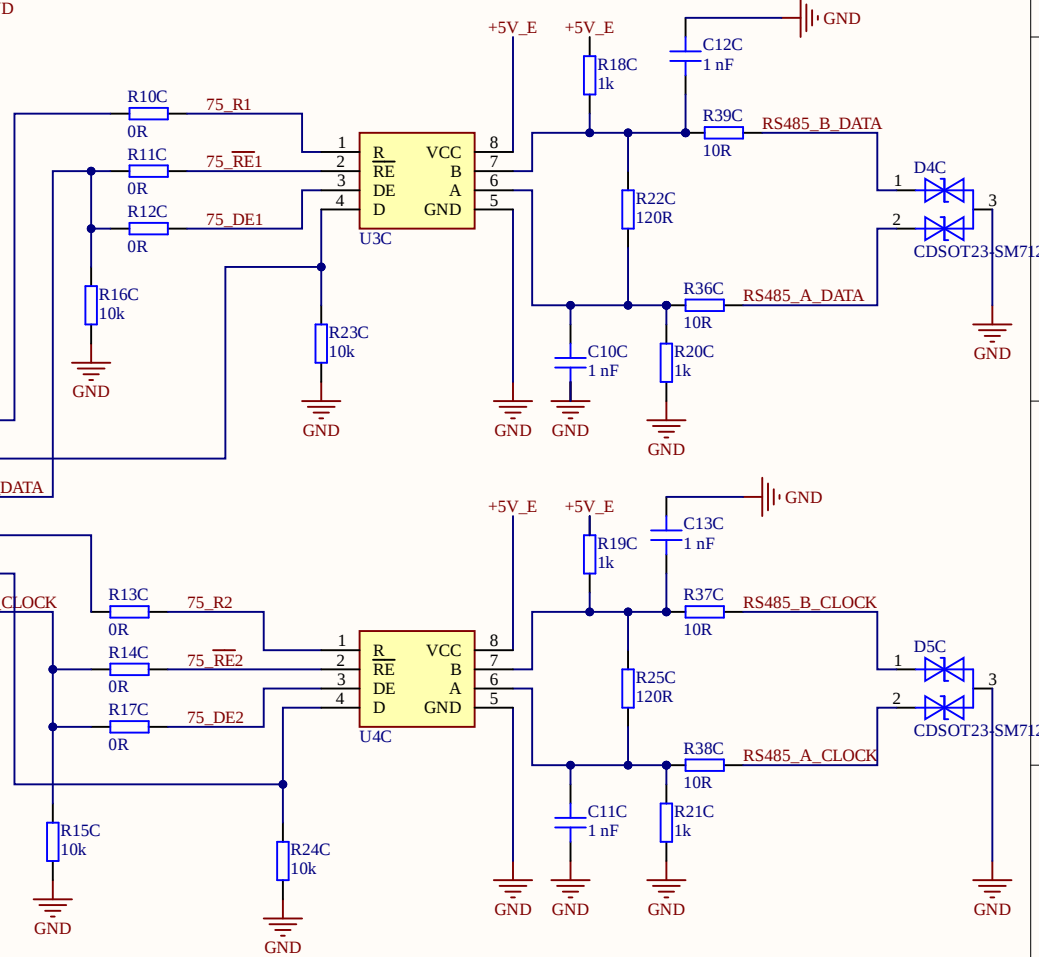
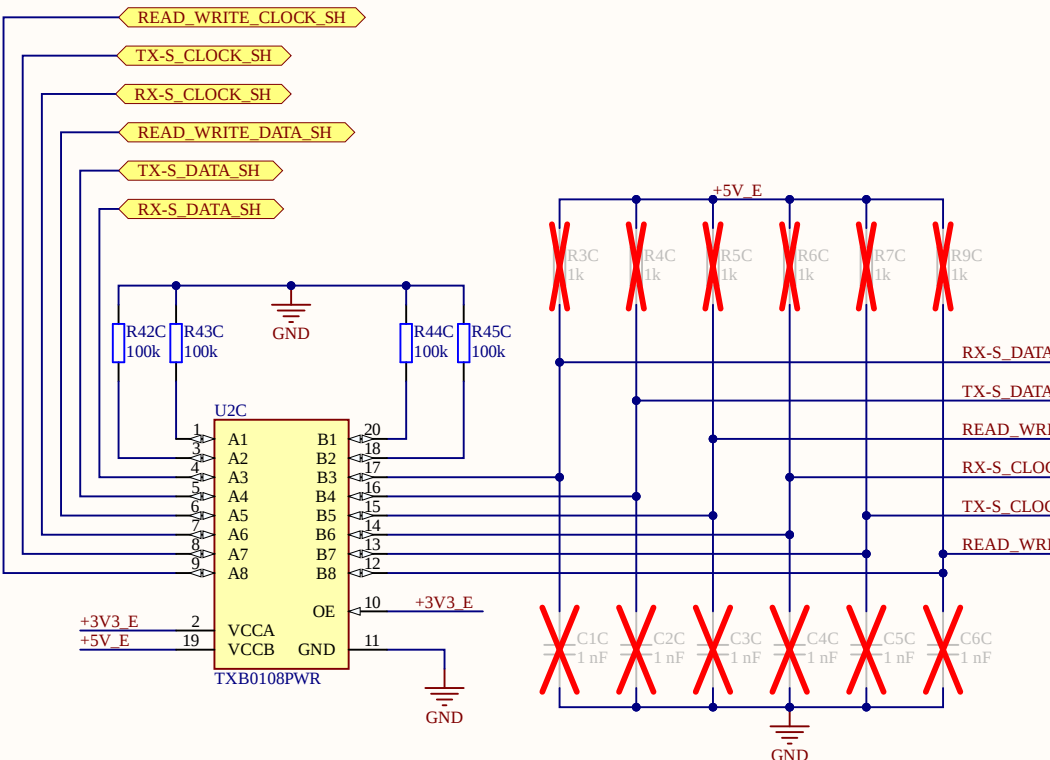
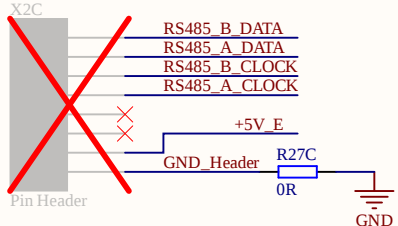
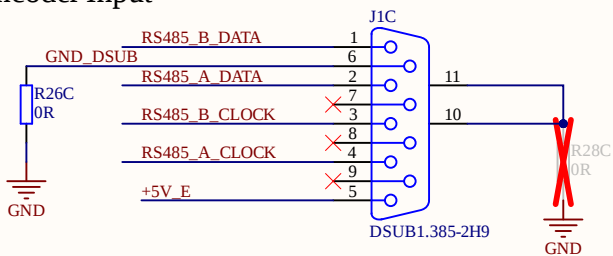
Encoder Input



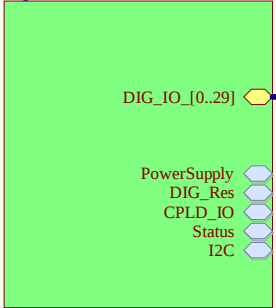
Power Supply Encoder



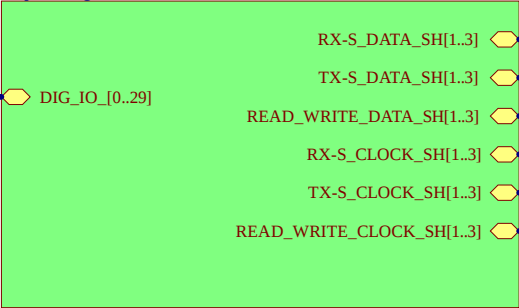
Encoder Input



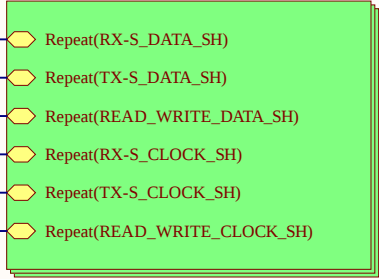
CarrierConnector
DigitalCarrierJack



DIG_IO_assignment
output_assignment



Repeat(encoder,1,3)
Encoder_Interface.SchDoc



Chose size of UZ logo
by chosing footprint
type



LOGO

T. Gaupp

Designer

uz_d_absolute_encoder

Project

01/25

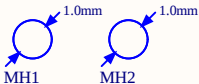
Date

Rev01

Revision

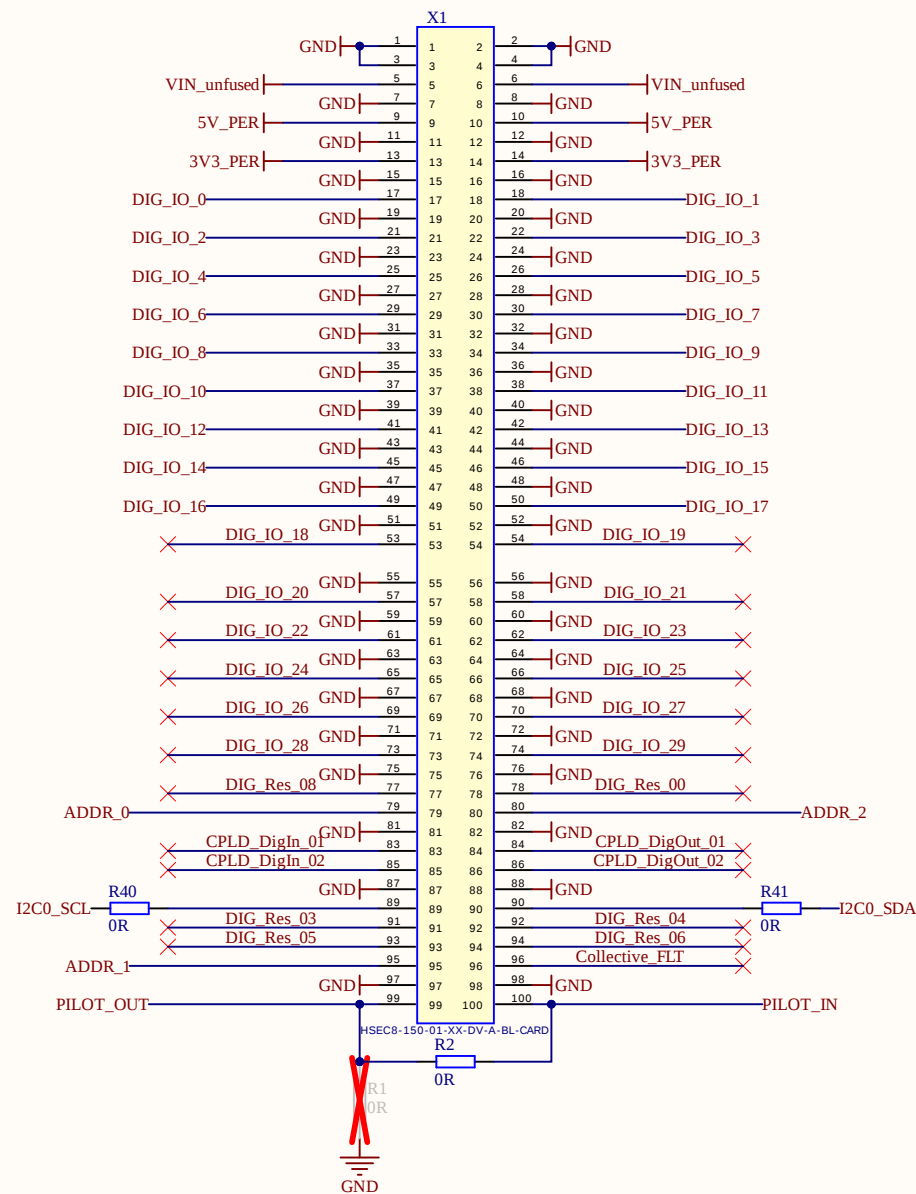
Serial

Serial



Title TopSheet.SchDoc		UltraZohm www.ultrazohm.com Date: 24.04.2026 Sheet 1 of 6	
Revision: Rev01	Design Engineer: T. Gaupp		
Project: uz_d_absolute_encoder.PrjPCB			

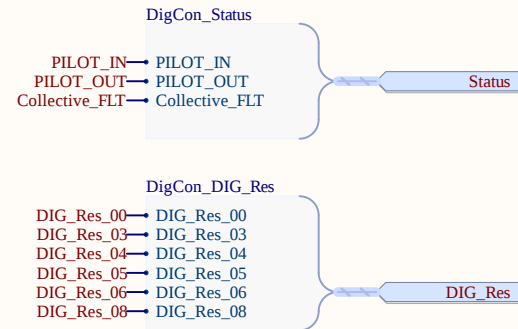
A



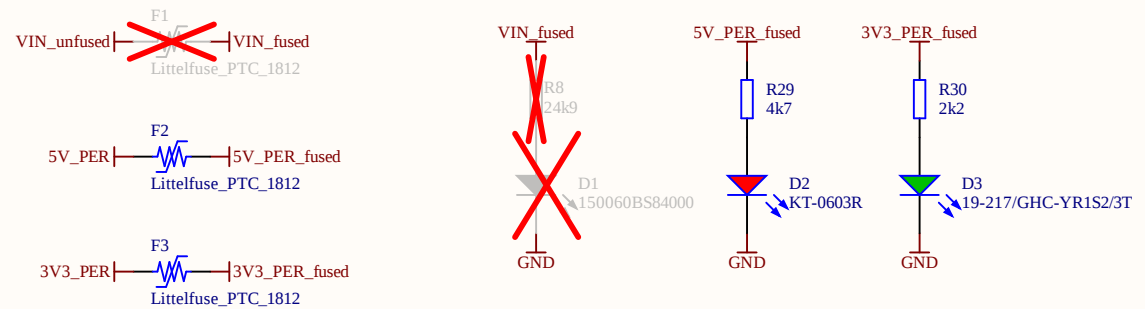
B

C

D

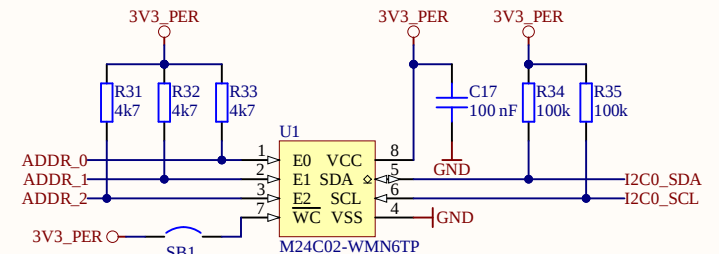


Fused Voltages



EEPROM Interface

(please do not exclude or delete from design)



Note: place solder bump to protect EEPROM memory from write access.

Title DigitalCarrierJack.SchDoc

Revision: Rev01

Design Engineer: T. Gaupp

Project: uz_d_absolute_encoder.PrjPCB

UltraZohm

www.ultrazohm.com

Date: 24.04.2026

Sheet 2 of 6



CPLD program uz_d_abs_encoder_ssi:

Attention! IO Mapping shown here is different to that you will need to respect in the FPGA design, since the CPLD program reroutes the signals in order to make the adapter board compatible to all D-slots:

Adapter Board - FPGA IO Pin - Function
DIG_IO_00->Dig_IO_06: RX-Data_2
DIG_IO_01->DIG_IO_07: RX-Data_1
DIG_IO_04<-DIG_IO_10: RW_Data_2
DIG_IO_05<-DIG_IO_11: RW_Data_1
DIG_IO_08<-DIG_IO_14: TX-Clock_2
DIG_IO_09<-DIG_IO_15: TX-Clock_1
DIG_IO_10<-DIG_IO_16: RW-Clock_2
DIG_IO_11<-DIG_IO_17: RW-Clock_1
DIG_IO_12->DIG_IO_18: RX-Data_3
DIG_IO_16<-DIG_IO_22: TX-Clock_3
DIG_IO_17<-DIG_IO_23: RW-Clock_3

