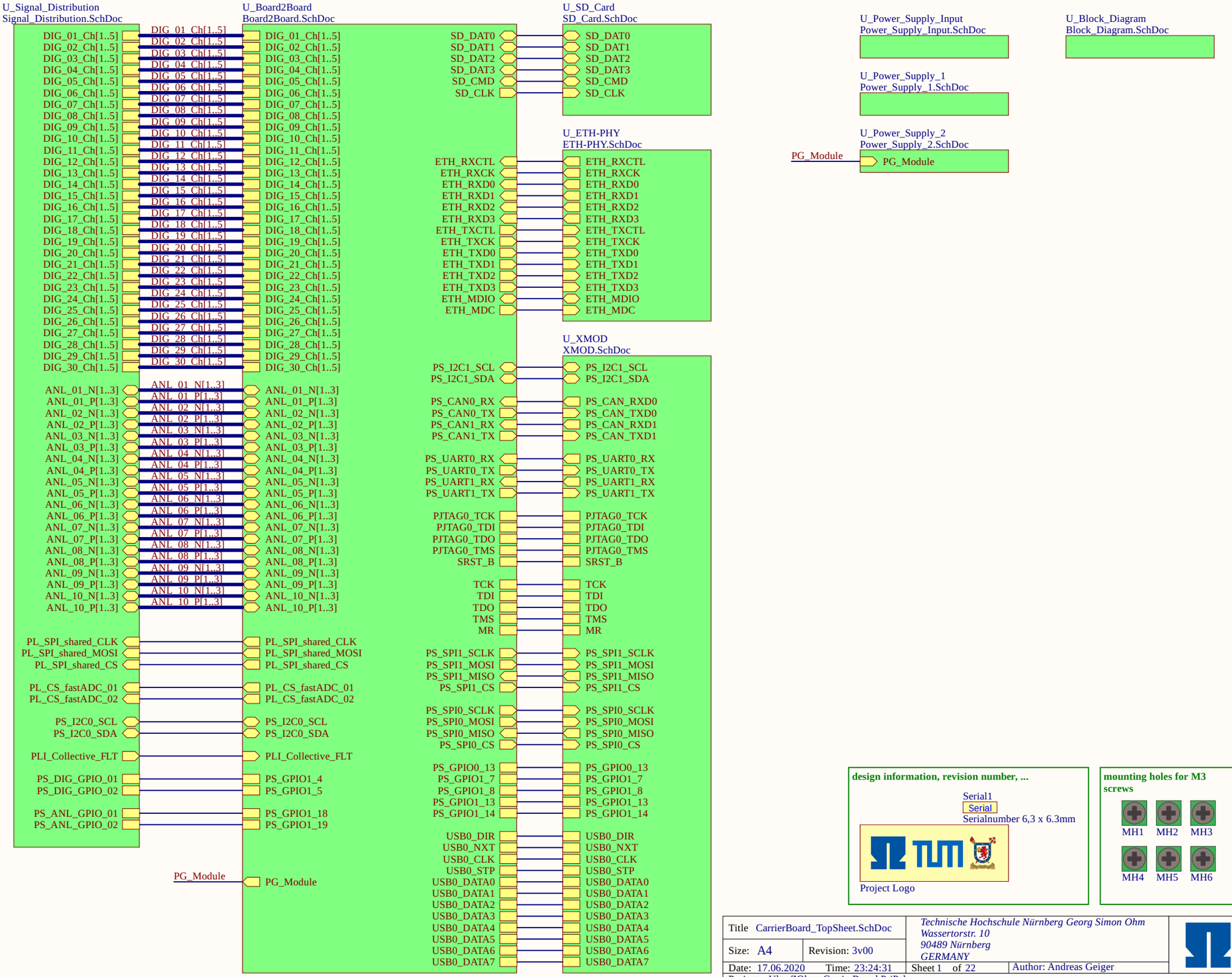
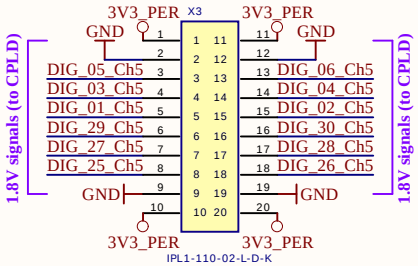
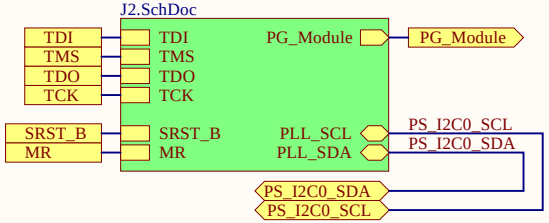

U_Signal_Distribution
Signal_Distribution.SchDoc
U_Board2Board
Board2Board.SchDoc
U_SD_Card
SD_Card.SchDoc
U_ETH-PHY
ETH-PHY.SchDoc
U_XMOD
XMOD.SchDoc
U_Power_Supply_Input
Power_Supply_Input.SchDoc
U_Block_Diagram
Block_Diagram.SchDoc
U_Power_Supply_1
Power_Supply_1.SchDoc
U_Power_Supply_2
Power_Supply_2.SchDoc
PG_Module
DIG_01_Ch[1..5]
DIG_02_Ch[1..5]
DIG_03_Ch[1..5]
DIG_04_Ch[1..5]
DIG_05_Ch[1..5]
DIG_06_Ch[1..5]
DIG_07_Ch[1..5]
DIG_08_Ch[1..5]
DIG_09_Ch[1..5]
DIG_10_Ch[1..5]
DIG_11_Ch[1..5]
DIG_12_Ch[1..5]
DIG_13_Ch[1..5]
DIG_14_Ch[1..5]
DIG_15_Ch[1..5]
DIG_16_Ch[1..5]
DIG_17_Ch[1..5]
DIG_18_Ch[1..5]
DIG_19_Ch[1..5]
DIG_20_Ch[1..5]
DIG_21_Ch[1..5]
DIG_22_Ch[1..5]
DIG_23_Ch[1..5]
DIG_24_Ch[1..5]
DIG_25_Ch[1..5]
DIG_26_Ch[1..5]
DIG_27_Ch[1..5]
DIG_28_Ch[1..5]
DIG_29_Ch[1..5]
DIG_30_Ch[1..5]
ANL_01_N[1..3]
ANL_01_P[1..3]
ANL_02_N[1..3]
ANL_02_P[1..3]
ANL_03_N[1..3]
ANL_03_P[1..3]
ANL_04_N[1..3]
ANL_04_P[1..3]
ANL_05_N[1..3]
ANL_05_P[1..3]
ANL_06_N[1..3]
ANL_06_P[1..3]
ANL_07_N[1..3]
ANL_07_P[1..3]
ANL_08_N[1..3]
ANL_08_P[1..3]
ANL_09_N[1..3]
ANL_09_P[1..3]
ANL_10_N[1..3]
ANL_10_P[1..3]
PL_SPI_shared_CLK
PL_SPI_shared_MOSI
PL_SPI_shared_CS
PL_CS_fastADC_01
PL_CS_fastADC_02
PS_I2C0_SCL
PS_I2C0_SDA
PLI_Collective_FLT
PS_DIG_GPIO_01
PS_DIG_GPIO_02
PS_ANL_GPIO_01
PS_ANL_GPIO_02
PS_GPIO1_4
PS_GPIO1_5
PS_GPIO1_18
PS_GPIO1_19
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
SD_CMD
SD_CLK
ETH_RXCTL
ETH_RXCK
ETH_RXD0
ETH_RXD1
ETH_RXD2
ETH_RXD3
ETH_TXCTL
ETH_TXCK
ETH_TXD0
ETH_TXD1
ETH_TXD2
ETH_TXD3
ETH_MDIO
ETH_MDC
PS_I2C1_SCL
PS_I2C1_SDA
PS_CAN0_RX
PS_CAN0_TX
PS_CAN1_RX
PS_CAN1_TX
PS_CAN_RXD0
PS_CAN_TXD0
PS_CAN_RXD1
PS_CAN_TXD1
PS_UART0_RX
PS_UART0_TX
PS_UART1_RX
PS_UART1_TX
PJTAG0_TCK
PJTAG0_TDI
PJTAG0_TDO
PJTAG0_TMS
SRST_B
TCK
TDI
TDO
TMS
MR
PS_SPI1_SCLK
PS_SPI1_MOSI
PS_SPI1_MISO
PS_SPI1_CS
PS_SPI0_SCLK
PS_SPI0_MOSI
PS_SPI0_MISO
PS_SPI0_CS
PS_GPIO0_13
PS_GPIO1_7
PS_GPIO1_8
PS_GPIO1_13
PS_GPIO1_14
USB0_DIR
USB0_NXT
USB0_CLK
USB0_STP
USB0_DATA0
USB0_DATA1
USB0_DATA2
USB0_DATA3
USB0_DATA4
USB0_DATA5
USB0_DATA6
USB0_DATA7
design information, revision number, ...
Serial1
Serial
Serialnumber 6,3 x 6.3mm
Project Logo
mounting holes for M3 screws
MH1
MH2
MH3
MH4
MH5
MH6
Title CarrierBoard_TopSheet.SchDoc
Size: A4
Revision: 3v00
Technische Hochschule Nürnberg Georg Simon Ohm
Wassertorstr. 10
90489 Nürnberg
GERMANY
Date: 17.06.2020
Time: 23:24:31
Sheet 1 of 22
Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb

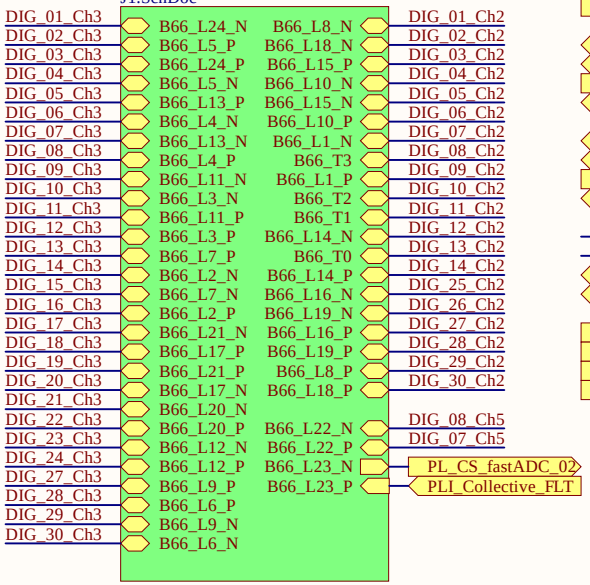
The 5th digital socket is not full connected with FPGA pins. DIG_01...DIG06 and DIG_25...DIG_30 of this socket can be used externally via this connector.



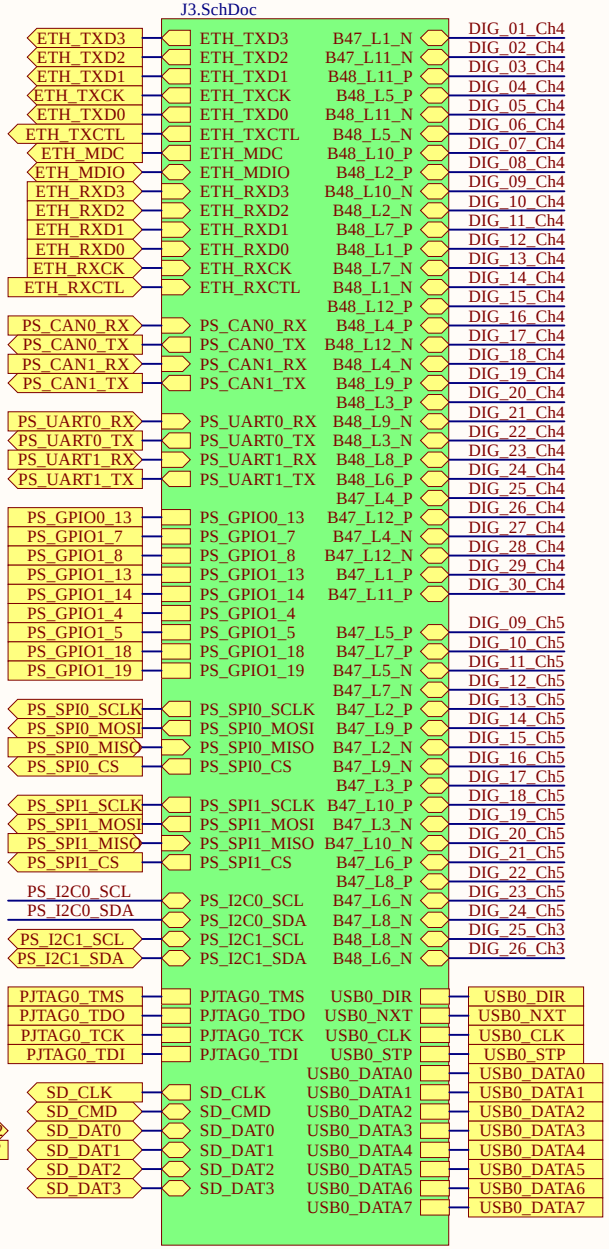
U_J2
J2.SchDoc



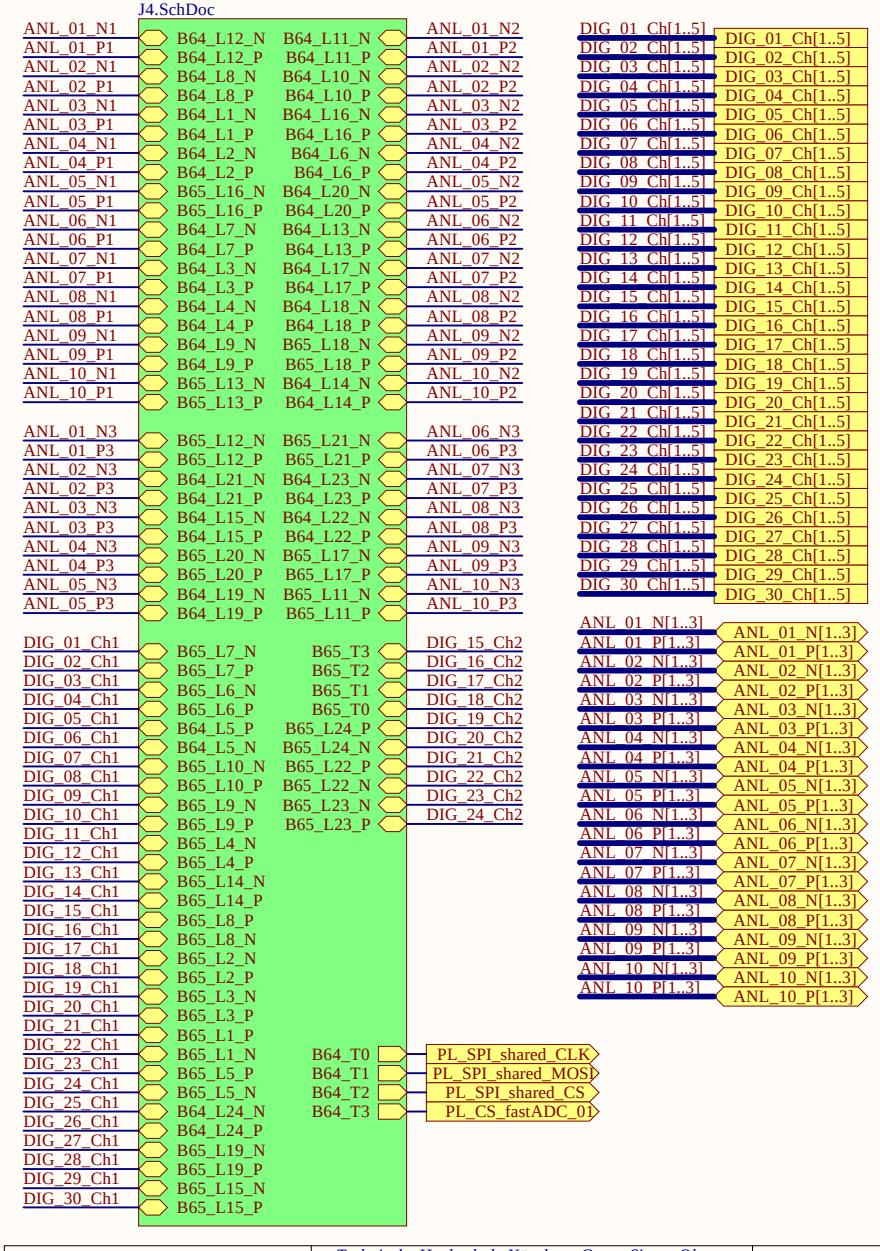
U_J1
J1.SchDoc



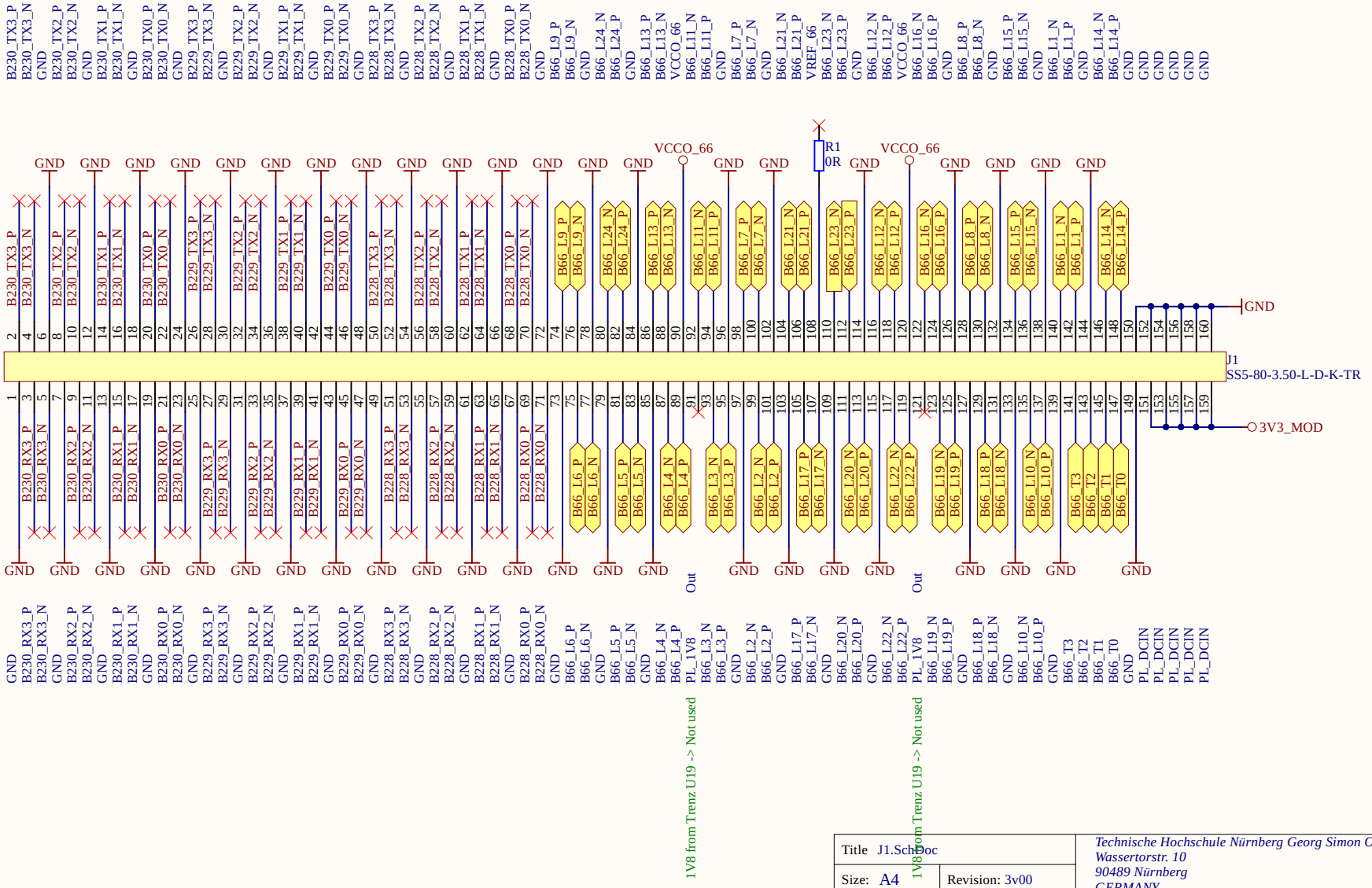
U_J3
J3.SchDoc



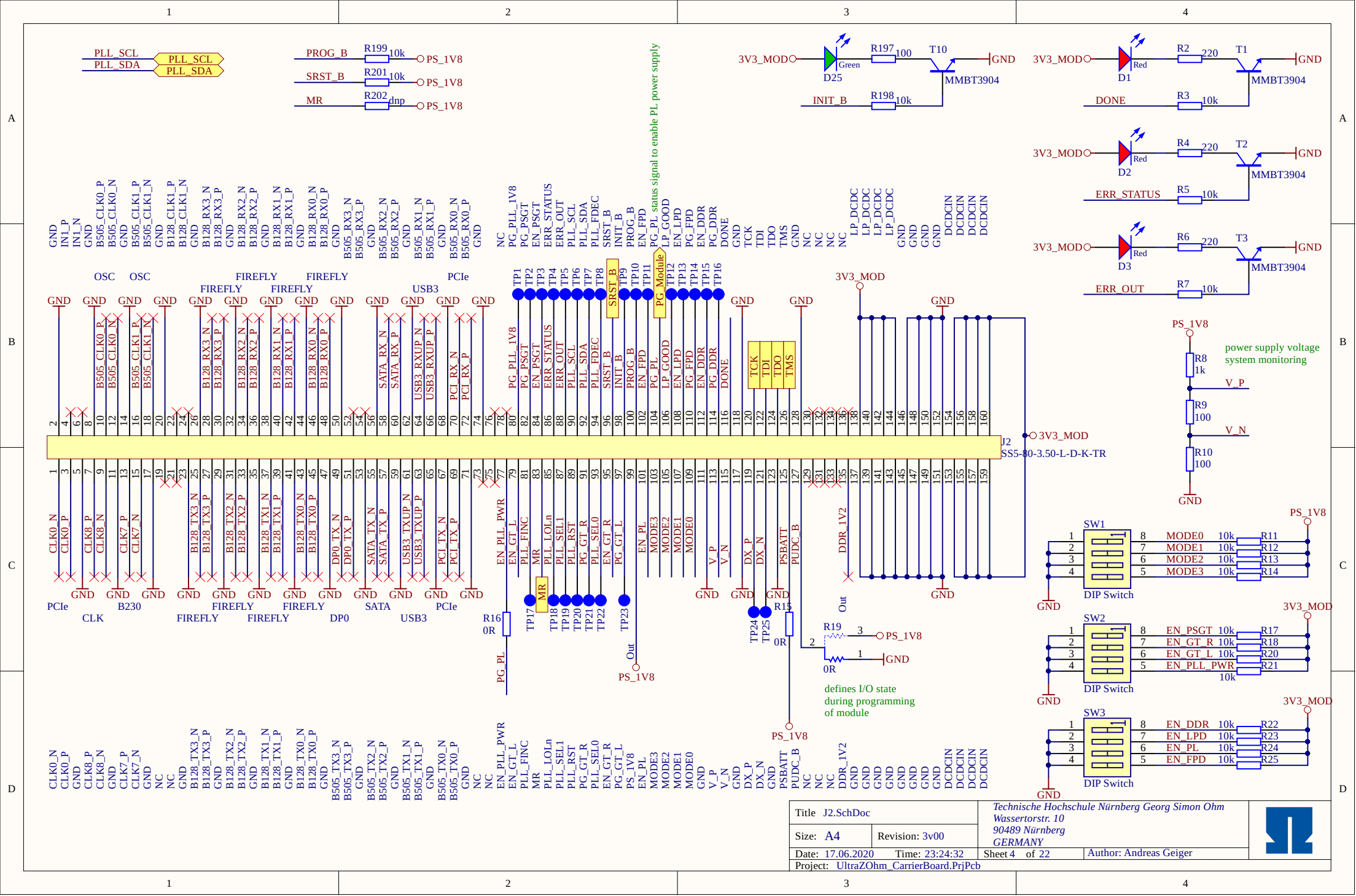
U_J4
J4.SchDoc

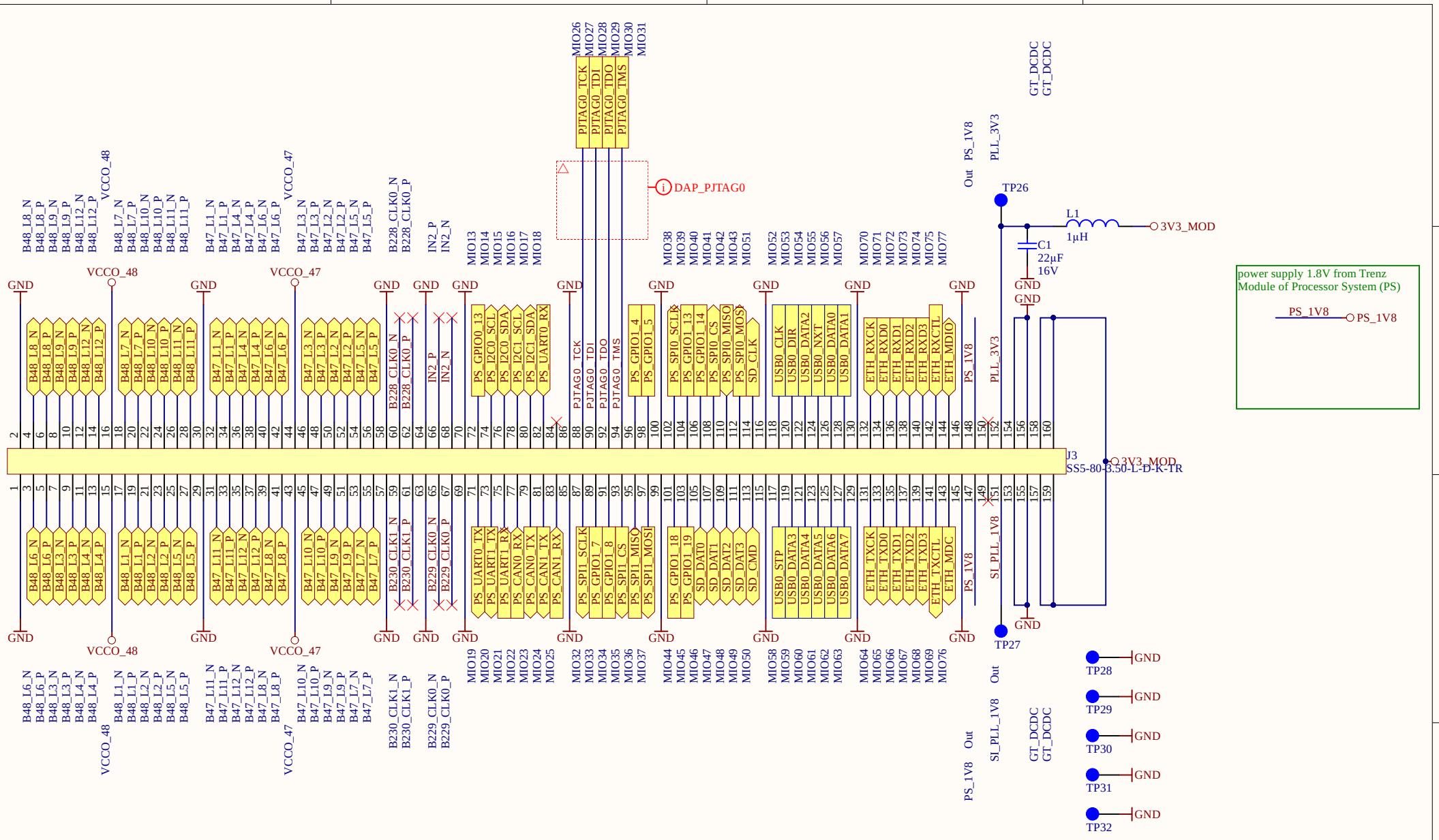


Title: Board2Board.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:31	Sheet 2 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			

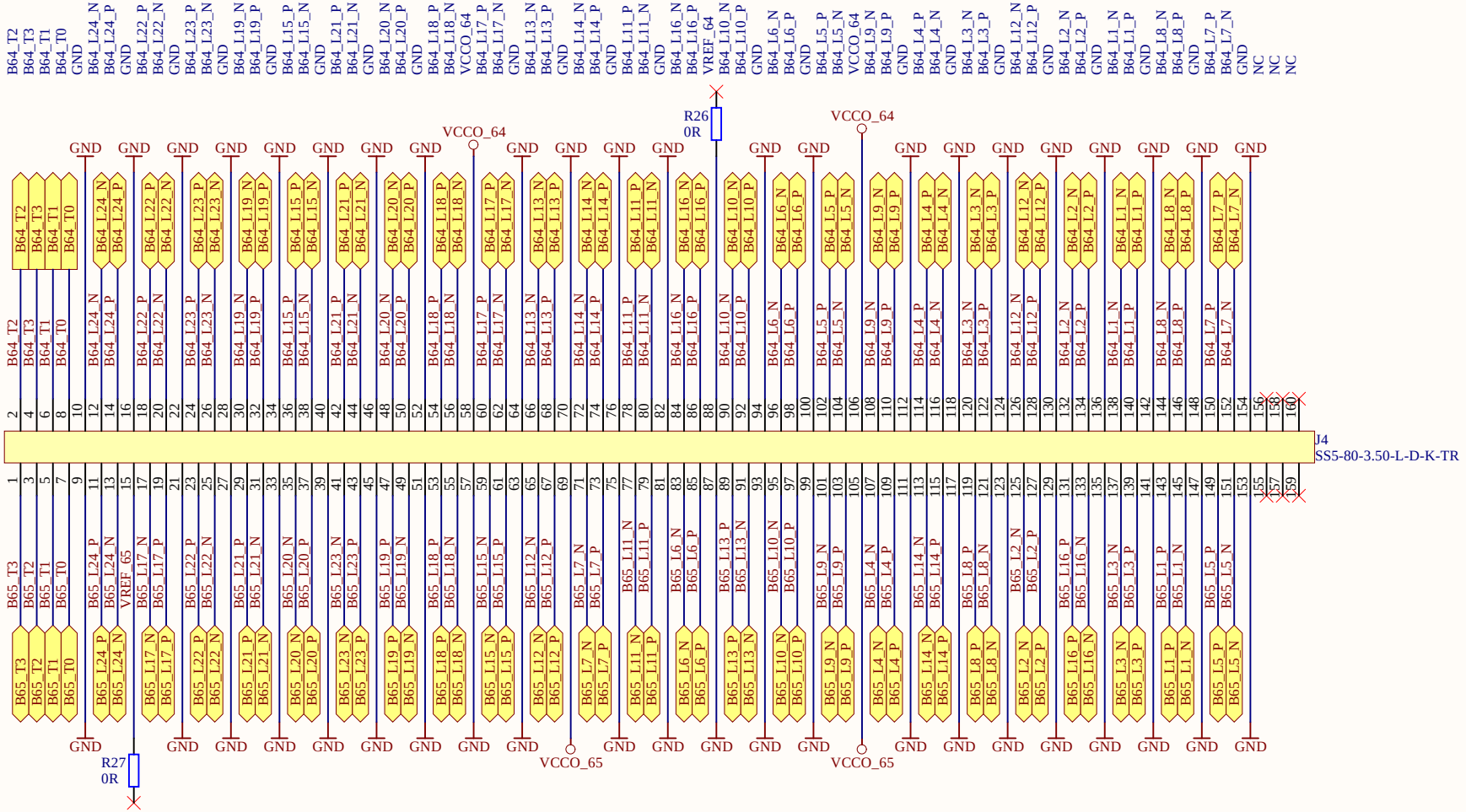


Title J1.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY
Size: A4	Revision: 3v00	
Date: 17.06.2020 Time: 23:24:32	Sheet 3 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb		

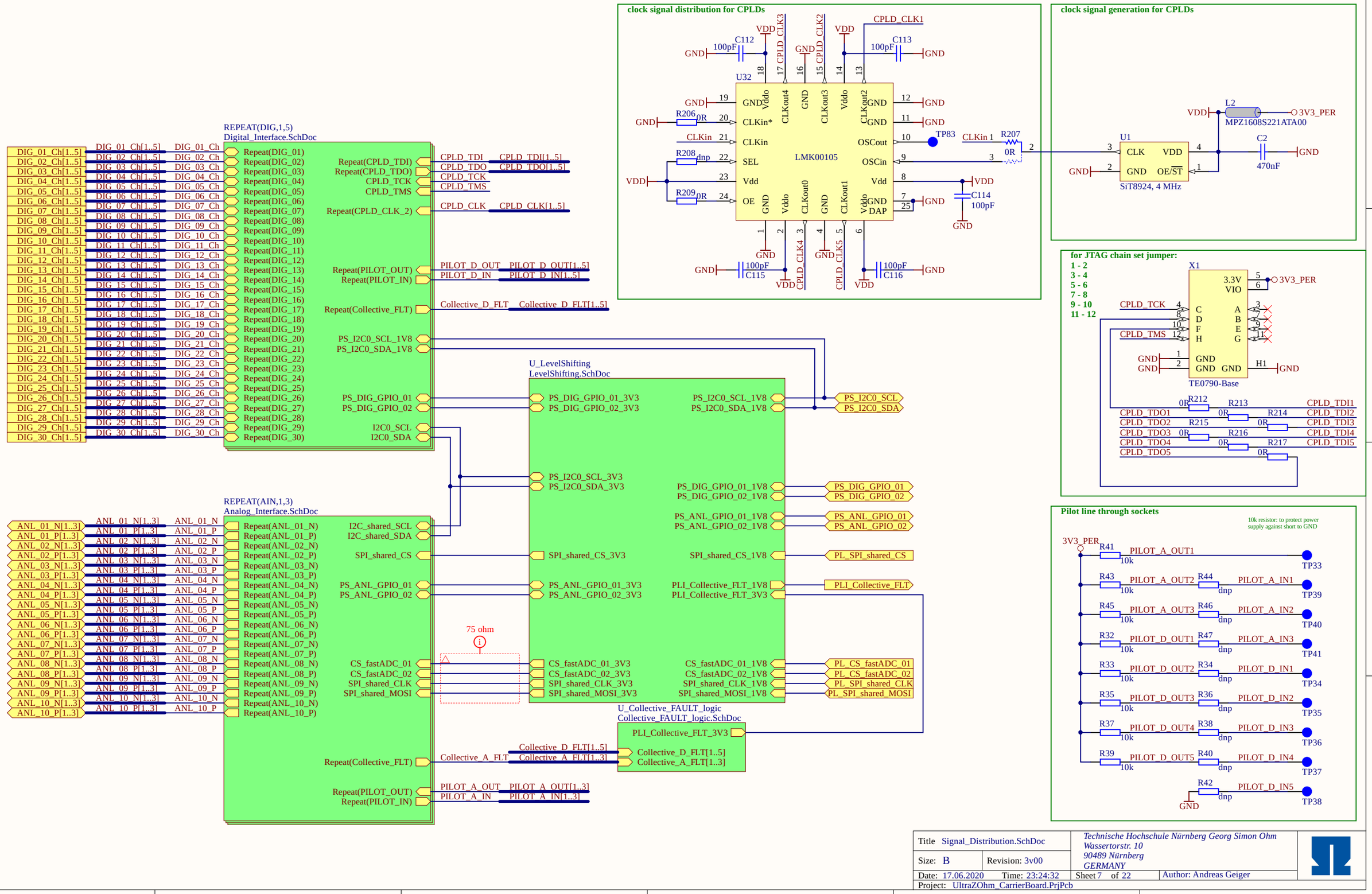

PLL_SCL
PLL_SDA
PROG_B
SRST_B
MR
R199 10k
R201 10k
R202 dnp
PS_1V8
3V3_MOD
D25 Green
R197 100
T10 MMBT3904
INIT_B
R198 10k
GND
D1 Red
R2 220
T1 MMBT3904
DONE
R3 10k
D2 Red
R4 220
T2 MMBT3904
ERR_STATUS
R5 10k
D3 Red
R6 220
T3 MMBT3904
ERR_OUT
R7 10k
PG_PL status signal to enable PL power supply
PG_Module
J2
SS5-80-3.50-L-D-K-TR
power supply voltage system monitoring
R8 1k
R9 100
R10 100
V_P
V_N
SW1
SW2
SW3
DIP Switch
MODE0 10k R11
MODE1 10k R12
MODE2 10k R13
MODE3 10k R14
EN_PSGT 10k R17
EN_GT_R 10k R18
EN_GT_L 10k R20
EN_PLL_PWR 10k R21
EN_DDR 10k R22
EN_LPD 10k R23
EN_PL 10k R24
EN_FPD 10k R25
R16 0R
R15 0R
R19
defines I/O state during programming of module
OSC
FIREFLY
USB3
PCIe
CLK
B230
DP0
SATA
Title J2.SchDoc
Size: A4
Revision: 3v00
Date: 17.06.2020
Time: 23:24:32
Sheet 4 of 22
Project: UltraZOhm_CarrierBoard.PrjPcb
Technische Hochschule Nürnberg Georg Simon Ohm
Wassertorstr. 10
90489 Nürnberg
GERMANY
Author: Andreas Geiger

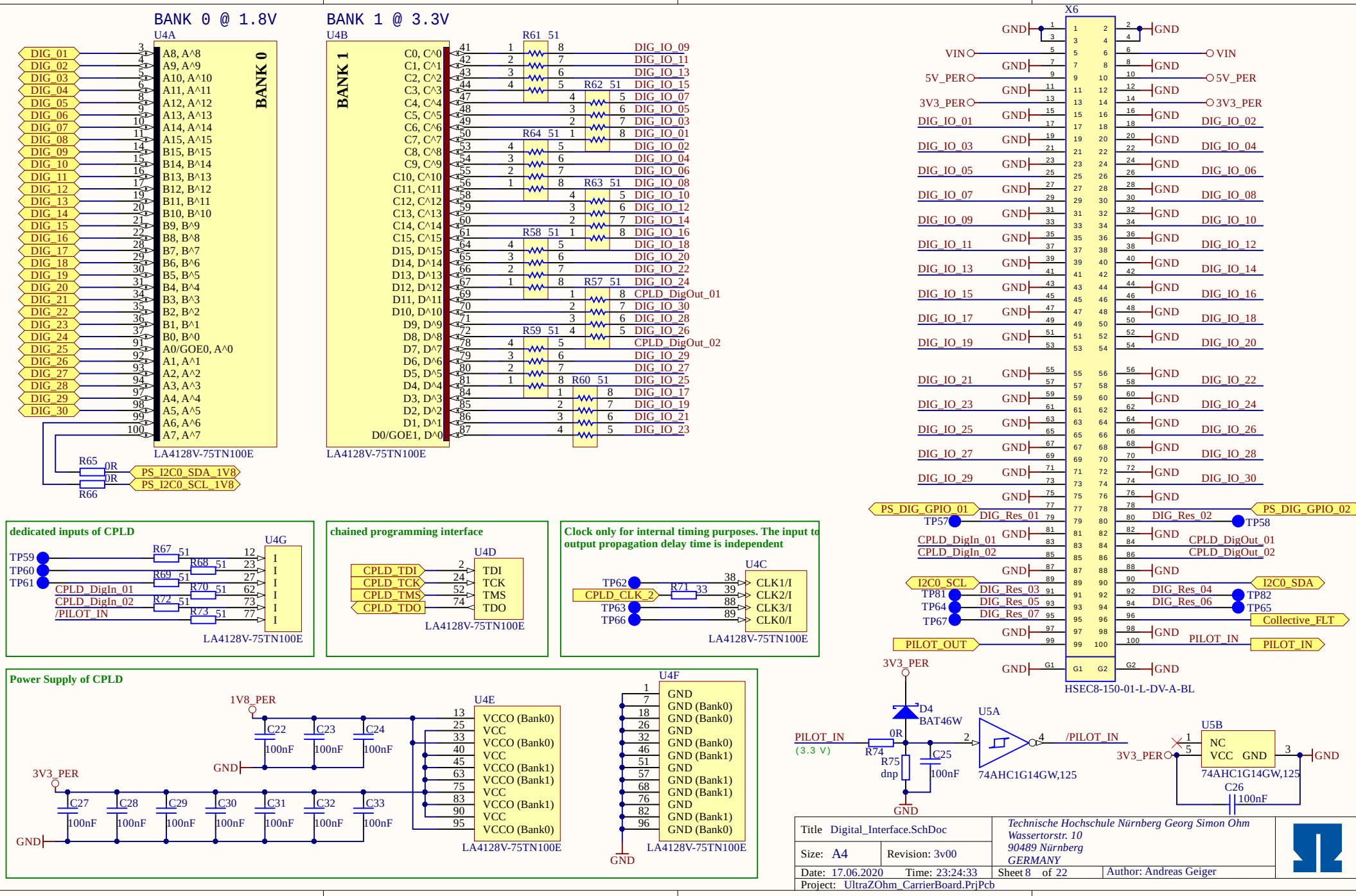


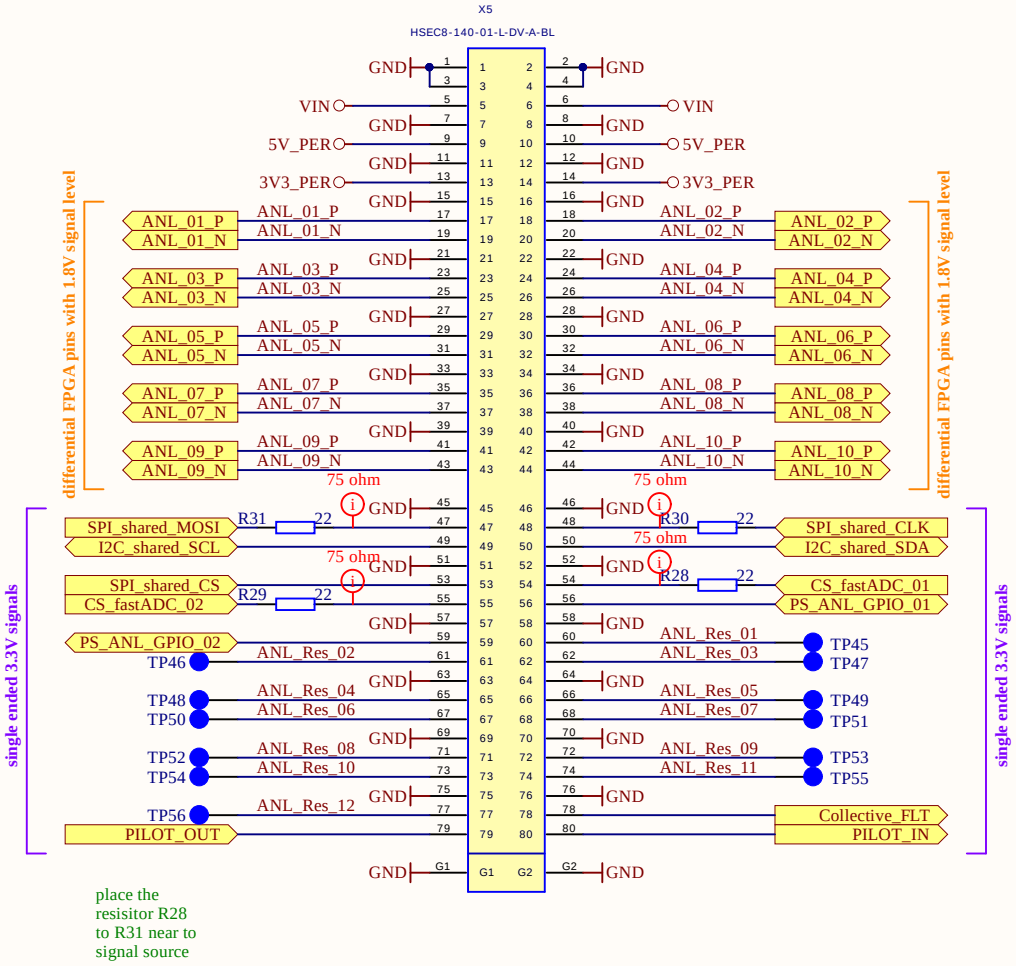
Title J3.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm*	
Size: A4	Revision: 3v00	*Wassertorstr. 10*	
Date: 17.06.2020	Time: 23:24:32	*90489 Nürnberg*	Sheet 5 of 22
Project: UltraZOhm_CarrierBoard.PrjPcb		*GERMANY*	Author: Andreas Geiger



Title J4.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:32	Sheet 6 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			


clock signal distribution for CPLDs
clock signal generation for CPLDs
for JTAG chain set jumper:
1 - 2
3 - 4
5 - 6
7 - 8
9 - 10
11 - 12
Pilot line through sockets
10k resistor: to protect power supply against short to GND
REPEAT(DIG,1,5)
Digital_Interface.SchDoc
REPEAT(AIN,1,3)
Analog_Interface.SchDoc
U_LevelShifting
LevelShifting.SchDoc
U_Collective_FAULT_logic
Collective_FAULT_logic.SchDoc
LMK00105
SiT8924, 4 MHz
TE0790-Base
75 ohm
Title Signal_Distribution.SchDoc
Size: B
Revision: 3v00
Date: 17.06.2020
Time: 23:24:32
Sheet 7 of 22
Project: UltraZOhm_CarrierBoard.PrjPcb
Technische Hochschule Nürnberg Georg Simon Ohm
Wassertorstr. 10
90489 Nürnberg
GERMANY
Author: Andreas Geiger


BANK 0 @ 1.8V
U4A
BANK 0
A8, A^8
A9, A^9
A10, A^10
A11, A^11
A12, A^12
A13, A^13
A14, A^14
A15, A^15
B15, B^15
B14, B^14
B13, B^13
B12, B^12
B11, B^11
B10, B^10
B9, B^9
B8, B^8
B7, B^7
B6, B^6
B5, B^5
B4, B^4
B3, B^3
B2, B^2
B1, B^1
B0, B^0
A0/GOE0, A^0
A1, A^1
A2, A^2
A3, A^3
A4, A^4
A5, A^5
A6, A^6
A7, A^7
DIG_01
DIG_02
DIG_03
DIG_04
DIG_05
DIG_06
DIG_07
DIG_08
DIG_09
DIG_10
DIG_11
DIG_12
DIG_13
DIG_14
DIG_15
DIG_16
DIG_17
DIG_18
DIG_19
DIG_20
DIG_21
DIG_22
DIG_23
DIG_24
DIG_25
DIG_26
DIG_27
DIG_28
DIG_29
DIG_30
LA4128V-75TN100E
R65 0R
R66 0R
PS_I2C0_SDA_1V8
PS_I2C0_SCL_1V8
BANK 1 @ 3.3V
U4B
BANK 1
C0, C^0
C1, C^1
C2, C^2
C3, C^3
C4, C^4
C5, C^5
C6, C^6
C7, C^7
C8, C^8
C9, C^9
C10, C^10
C11, C^11
C12, C^12
C13, C^13
C14, C^14
C15, C^15
D15, D^15
D14, D^14
D13, D^13
D12, D^12
D11, D^11
D10, D^10
D9, D^9
D8, D^8
D7, D^7
D6, D^6
D5, D^5
D4, D^4
D3, D^3
D2, D^2
D1, D^1
D0/GOE1, D^0
R61 51
R62 51
R63 51
R64 51
R57 51
R58 51
R59 51
R60 51
DIG_IO_09
DIG_IO_11
DIG_IO_13
DIG_IO_15
DIG_IO_07
DIG_IO_05
DIG_IO_03
DIG_IO_01
DIG_IO_02
DIG_IO_04
DIG_IO_06
DIG_IO_08
DIG_IO_10
DIG_IO_12
DIG_IO_14
DIG_IO_16
DIG_IO_18
DIG_IO_20
DIG_IO_22
DIG_IO_24
CPLD_DigOut_01
DIG_IO_30
DIG_IO_28
DIG_IO_26
CPLD_DigOut_02
DIG_IO_29
DIG_IO_27
DIG_IO_25
DIG_IO_17
DIG_IO_19
DIG_IO_21
DIG_IO_23
LA4128V-75TN100E
X6
GND
VIN
5V_PER
3V3_PER
DIG_IO_01
DIG_IO_02
DIG_IO_03
DIG_IO_04
DIG_IO_05
DIG_IO_06
DIG_IO_07
DIG_IO_08
DIG_IO_09
DIG_IO_10
DIG_IO_11
DIG_IO_12
DIG_IO_13
DIG_IO_14
DIG_IO_15
DIG_IO_16
DIG_IO_17
DIG_IO_18
DIG_IO_19
DIG_IO_20
DIG_IO_21
DIG_IO_22
DIG_IO_23
DIG_IO_24
DIG_IO_25
DIG_IO_26
DIG_IO_27
DIG_IO_28
DIG_IO_29
DIG_IO_30
PS_DIG_GPIO_01
PS_DIG_GPIO_02
DIG_Res_01
DIG_Res_02
TP57
TP58
CPLD_DigIn_01
CPLD_DigIn_02
CPLD_DigOut_01
CPLD_DigOut_02
I2C0_SCL
I2C0_SDA
DIG_Res_03
DIG_Res_04
DIG_Res_05
DIG_Res_06
TP81
TP82
TP64
TP65
TP67
Collective_FLT
PILOT_OUT
PILOT_IN
HSEC8-150-01-L-DV-A-BL
dedicated inputs of CPLD
U4G
TP59
TP60
TP61
CPLD_DigIn_01
CPLD_DigIn_02
/PILOT_IN
R67 51
R68 51
R69 51
R70 51
R72 51
R73 51
I
LA4128V-75TN100E
chained programming interface
U4D
CPLD_TDI
CPLD_TCK
CPLD_TMS
CPLD_TDO
TDI
TCK
TMS
TDO
LA4128V-75TN100E
Clock only for internal timing purposes. The input to output propagation delay time is independent
U4C
TP62
CPLD_CLK_2
TP63
TP66
R71 33
CLK1/I
CLK2/I
CLK3/I
CLK0/I
LA4128V-75TN100E
Power Supply of CPLD
1V8_PER
3V3_PER
GND
C22 100nF
C23 100nF
C24 100nF
C27 100nF
C28 100nF
C29 100nF
C30 100nF
C31 100nF
C32 100nF
C33 100nF
U4E
VCCO (Bank0)
VCC
VCCO (Bank0)
VCC
VCCO (Bank1)
VCCO (Bank1)
VCC
VCCO (Bank1)
VCC
VCCO (Bank0)
LA4128V-75TN100E
U4F
GND
GND (Bank0)
GND (Bank0)
GND
GND (Bank0)
GND (Bank1)
GND
GND (Bank1)
GND (Bank1)
GND
GND (Bank1)
GND (Bank0)
LA4128V-75TN100E
D4 BAT46W
PILOT_IN
(3.3 V)
R74 0R
R75 dnp
C25 100nF
U5A
74AHC1G14GW,125
/PILOT_IN
U5B
NC
VCC
GND
74AHC1G14GW,125
C26 100nF
Title Digital_Interface.SchDoc
Size: A4
Revision: 3v00
Date: 17.06.2020
Time: 23:24:33
Sheet 8 of 22
Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb
Technische Hochschule Nürnberg Georg Simon Ohm
Wassertorstr. 10
90489 Nürnberg
GERMANY



place the resisitor R28 to R31 near to signal source

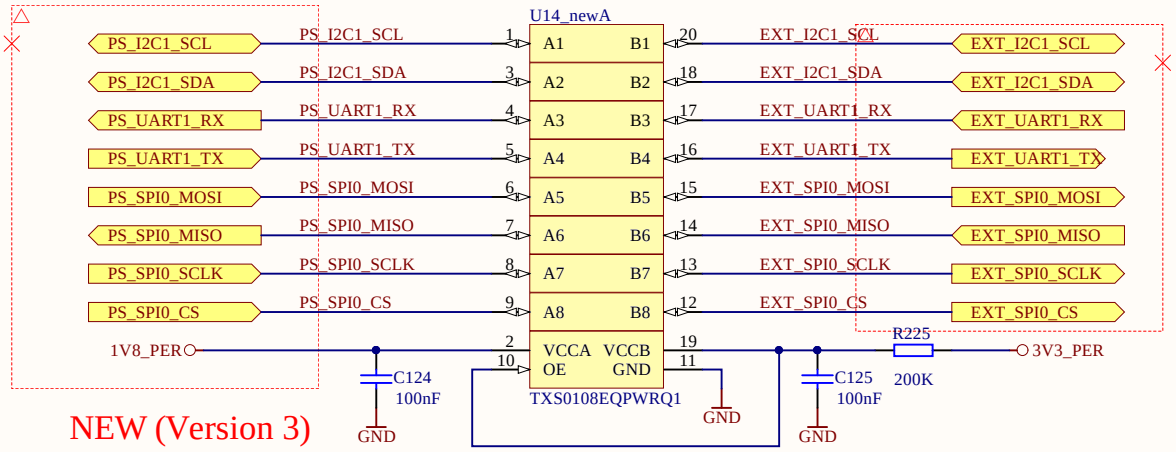
ANL_01_P
ANL_01_N
ANL_02_P
ANL_02_N
ANL_03_P
ANL_03_N
ANL_04_P
ANL_04_N
ANL_05_P
ANL_05_N
ANL_06_P
ANL_06_N
ANL_07_P
ANL_07_N
ANL_08_P
ANL_08_N
ANL_09_P
ANL_09_N
ANL_10_P
ANL_10_N

Note: The net labels do not float but altium says that they do because the nets are not connected to a pin

Collective_FAULT goes to all sockets

Title Analog_Interface.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:33	Sheet 9 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			

Bidirectional Level Shifting 1.8V to 3.3V

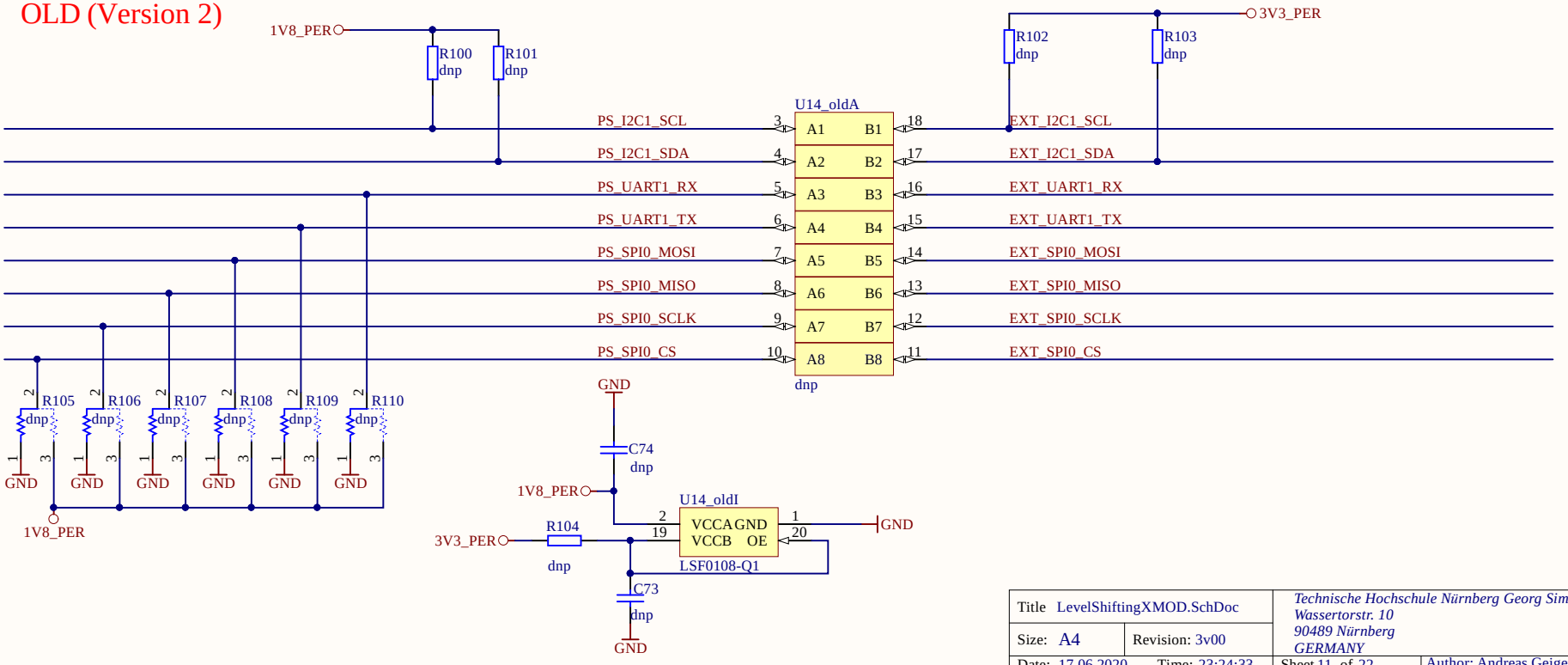


Note: In the layout U14_old and U14_new do not have a alphabetical suffix it is only called U14_old and U14_new.

Either the old or the new level shifter must be assembled but not both

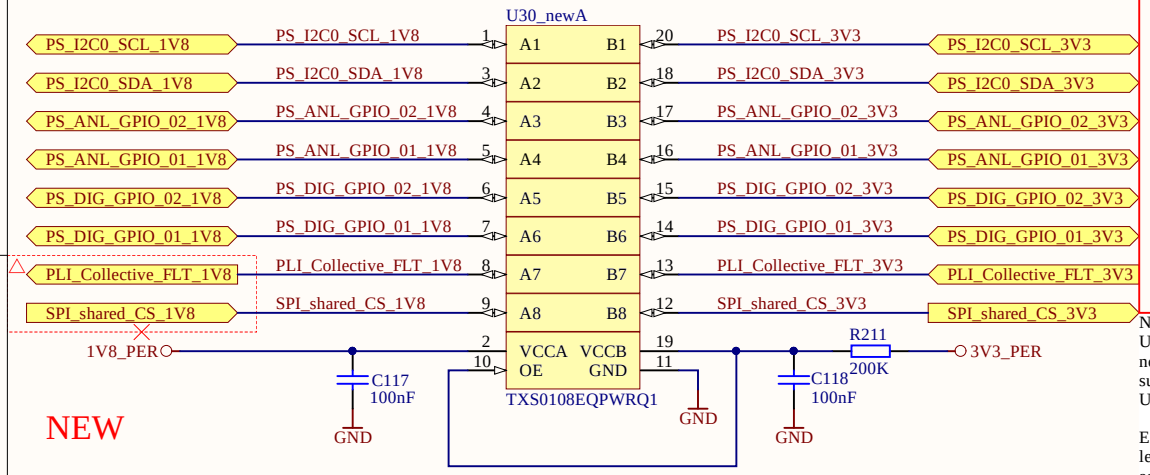
NEW (Version 3)

OLD (Version 2)



Title LevelShiftingXMOD.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:33	Sheet 11 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			

Bidirectional Level Shifting 1.8V to 3.3V

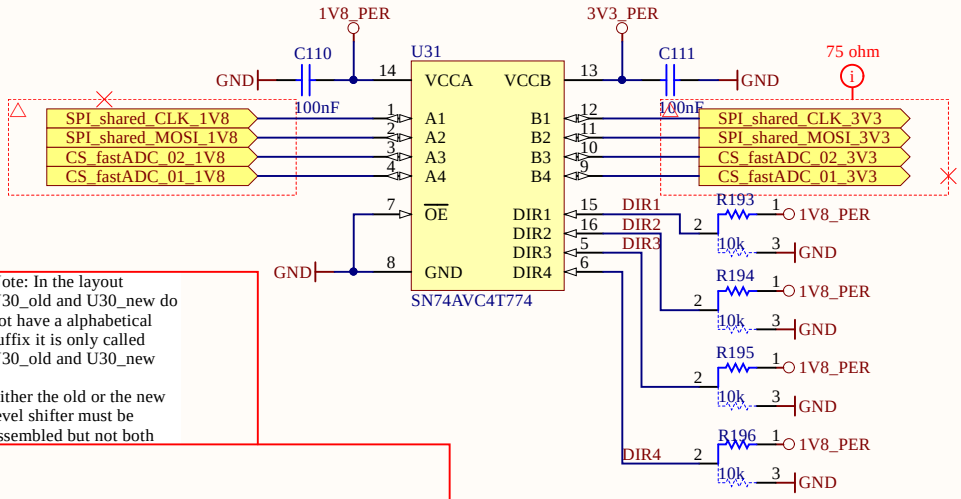


NEW

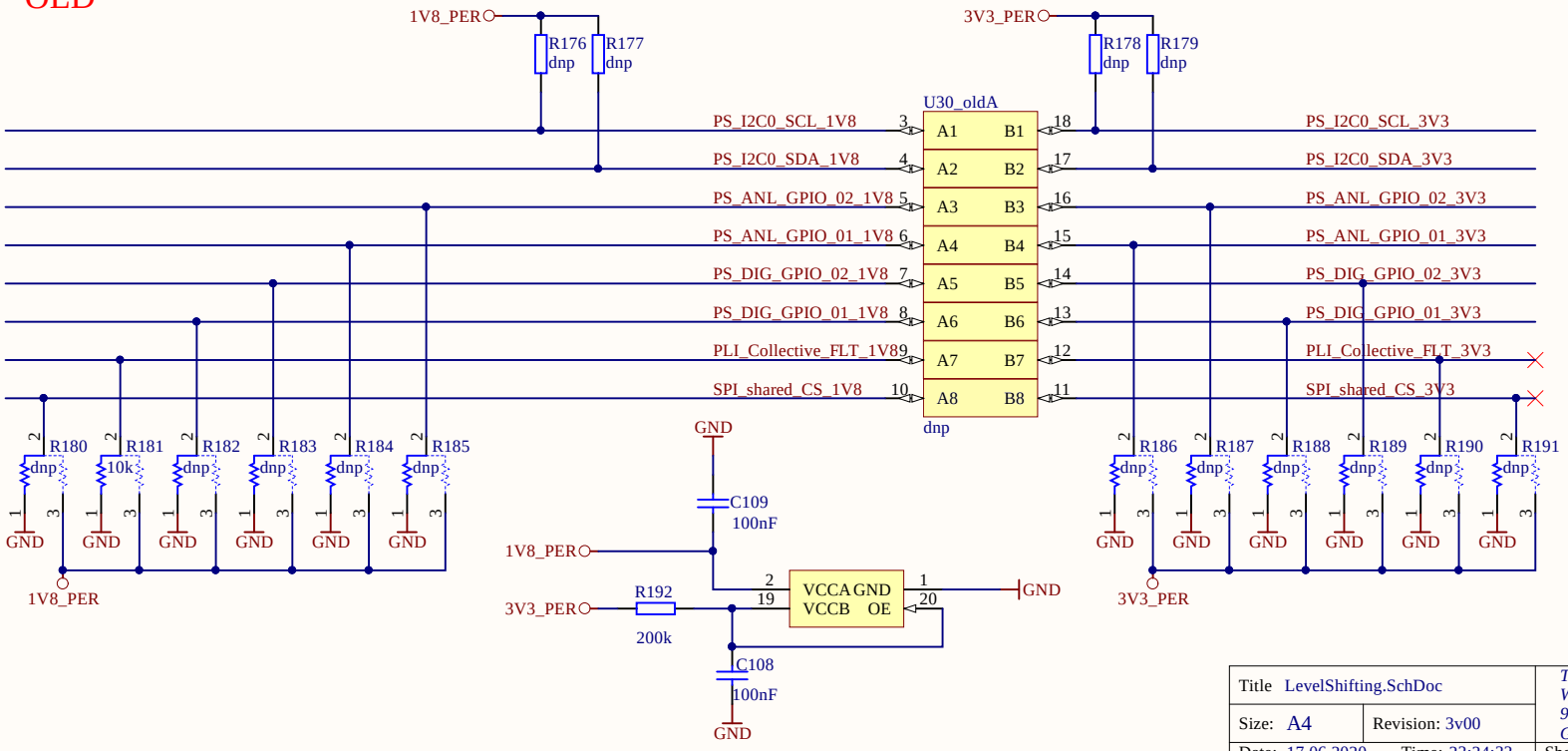
Note: In the layout U30_old and U30_new do not have a alphabetical suffix it is only called U30_old and U30_new

Either the old or the new level shifter must be assembled but not both

Unidirectional level Shifting 1.8V to 3.3V



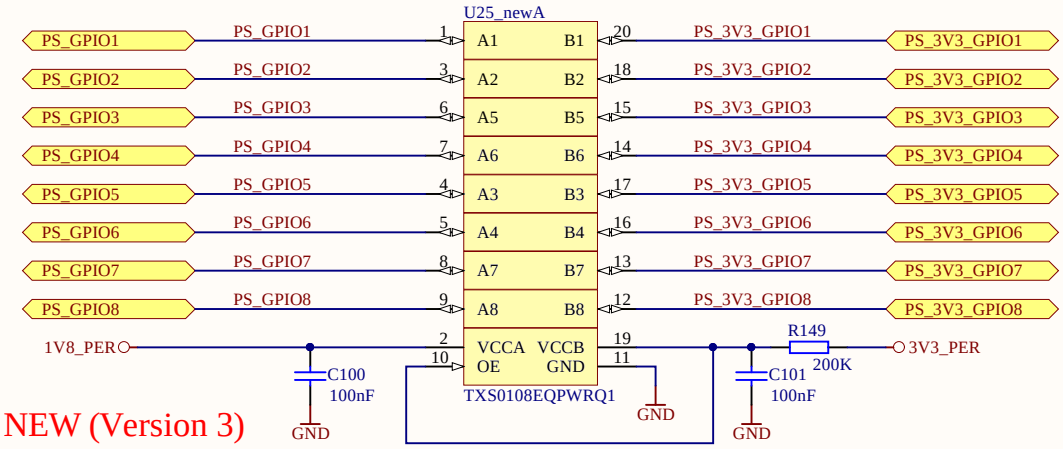
OLD



Note: by the correct configuration of the DIR pins the IO ports act as input and output as specified by the port direction

Title LevelShifting.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:33	Sheet 11 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			

Bidirectional Level Shifting 1.8V to 3.3V

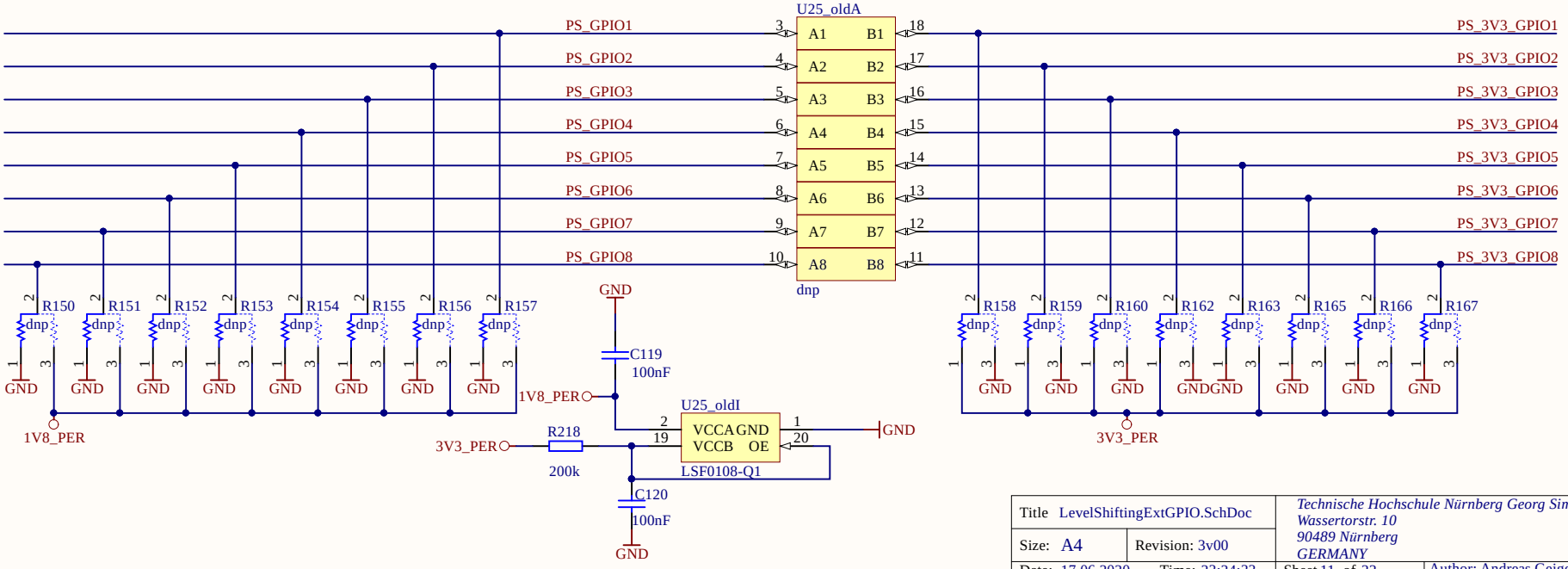


Note: In the layout U25_old and U25_new do not have a alphabetical suffix it is only called U25_old and U25_new.

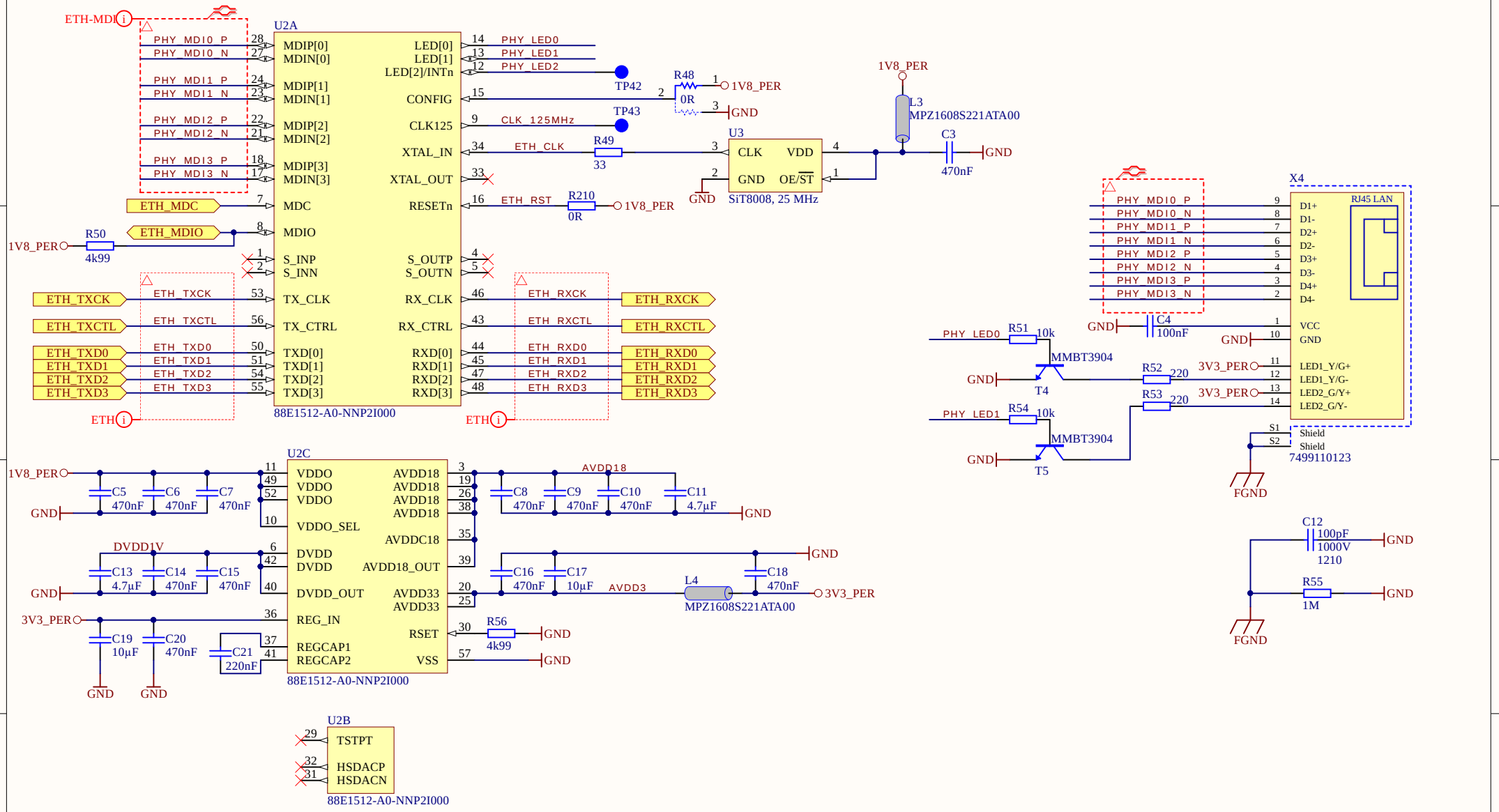
Either the old or the new level shifter must be assembled but not both

NEW (Version 3)

OLD (Version 2)

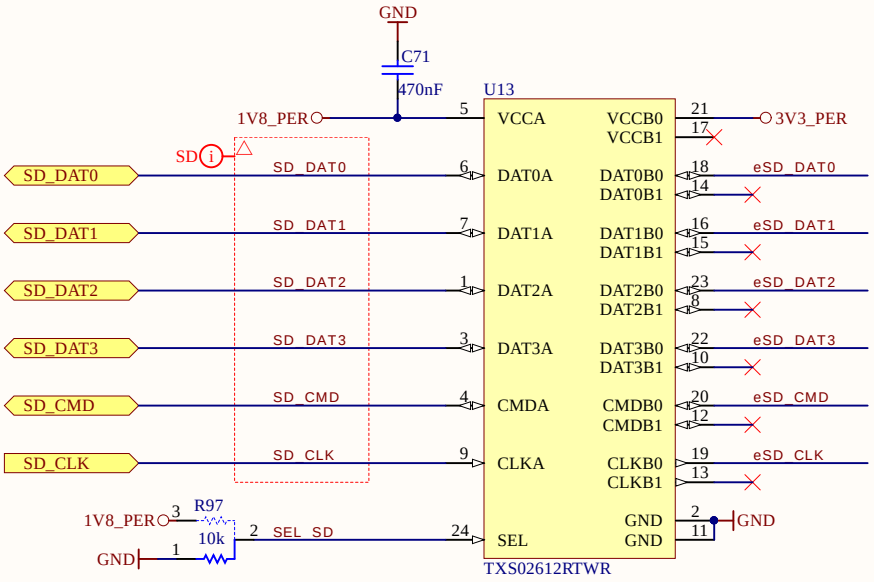


Title LevelShiftingExtGPIO.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:33	Sheet 11 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			



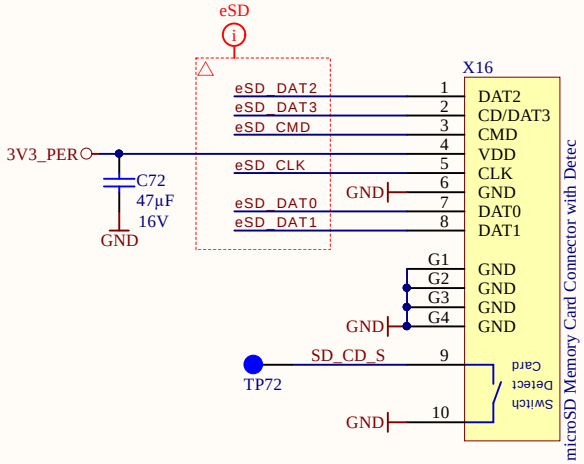
Title ETH-PHY.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm*	
Size: A4	Revision: 3v00	*Wassertorstr. 10*	
		90489 Nürnberg	
Date: 17.06.2020	Time: 23:24:33	*GERMANY*	
Sheet 12 of 22	Author: Andreas Geiger		
Project: UltraZOhm_CarrierBoard.PrjPcb			

Bidirectional Level Shifting 1.8V to 3.3V



SEL_SD on DGND to enable B0

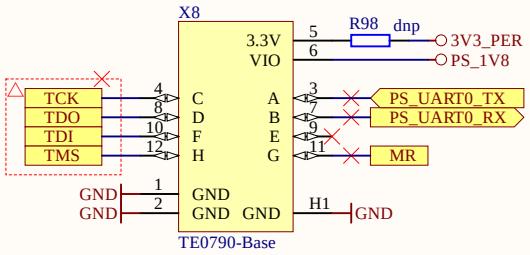
SD Card Connector



Title SD_Card.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:33	Sheet 13 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			

JTAG-Interface

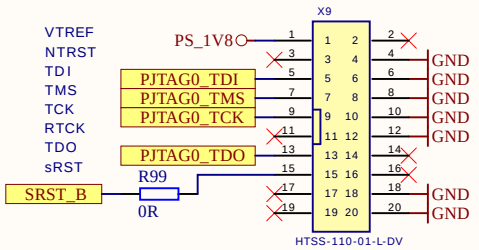
JTAG/UART header ('XMOD FTDI JTAG Adapter'-compatible) for access to MPSoC module



XMOD-FT2232H header: JTAG and UART

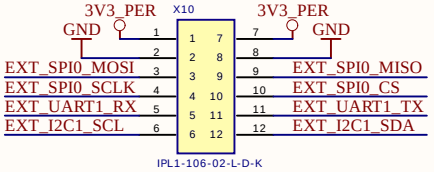
PJTAG-Interface (optional)

ARM JTAG

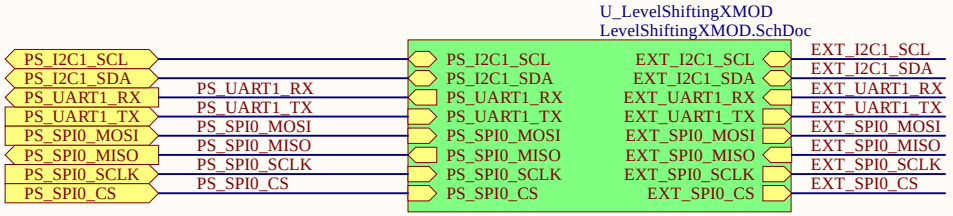


SPI, UART, I2C-Interface (from Processor System)

SPI, UART and I2C Connector @ 3.3V level

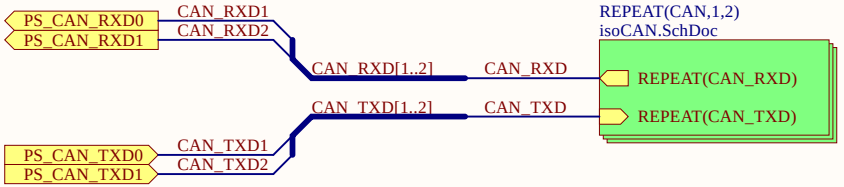


Bidirectional Level Shifting 1.8V to 3.3V

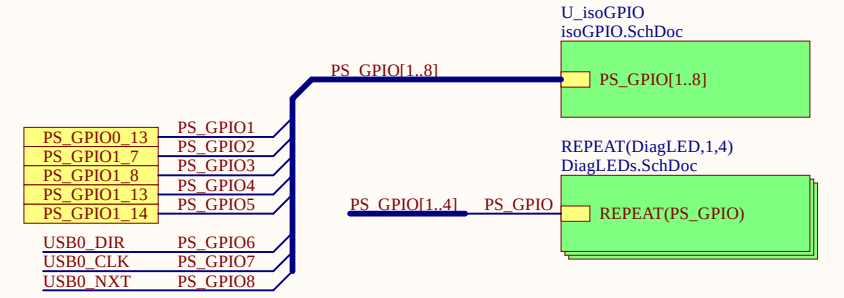


2x Isolated CAN-Interface

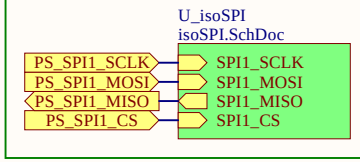
(renamed numbering, because multi channel design in Altium Designer starts with index 1 instead of 0)



Isolated External GPIO Interface

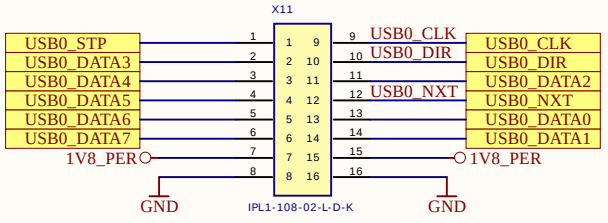


Isolated SPI-Interface

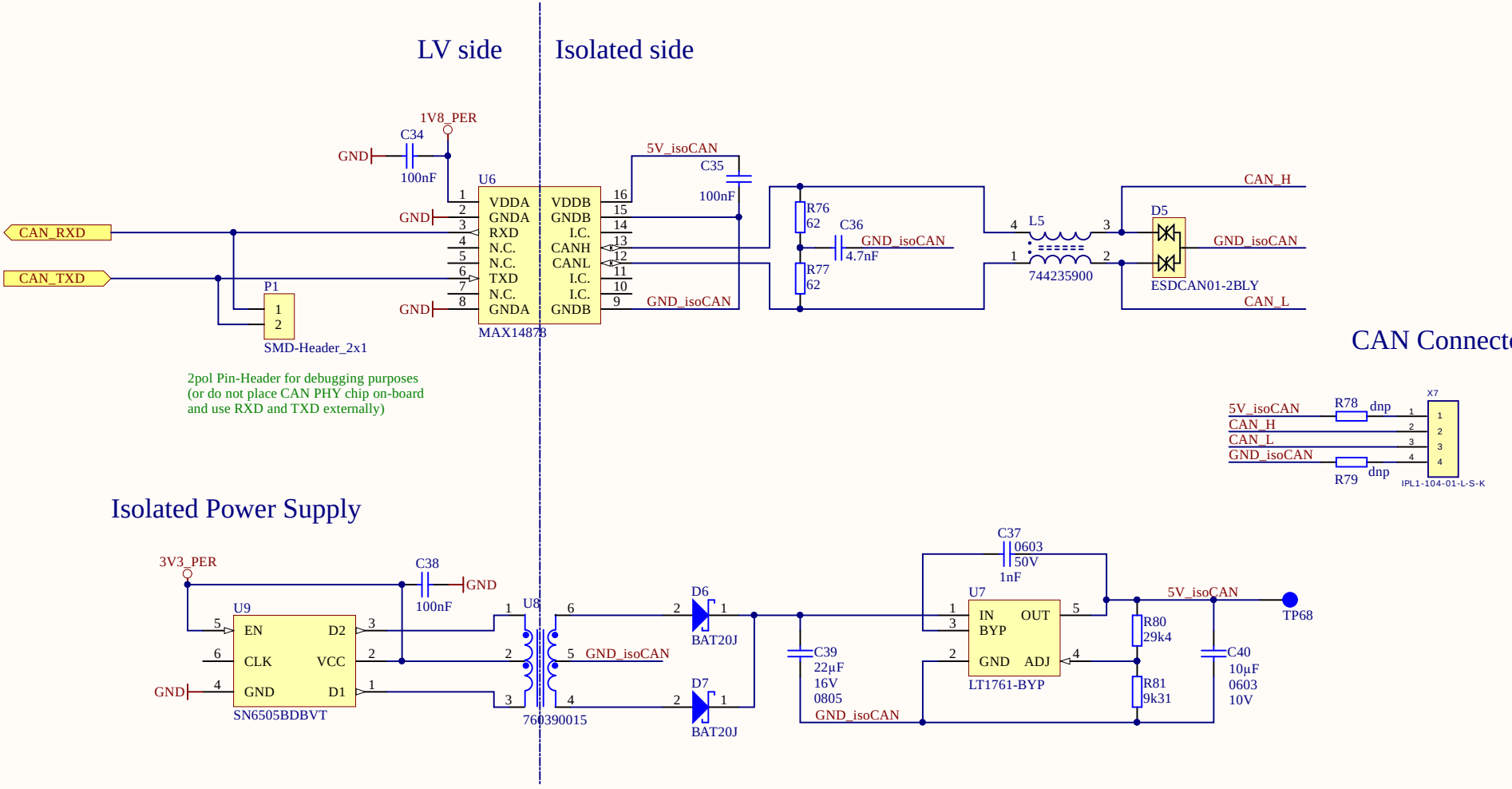


USB Pins on Header

(for use as extension port or pin use as GPIO)

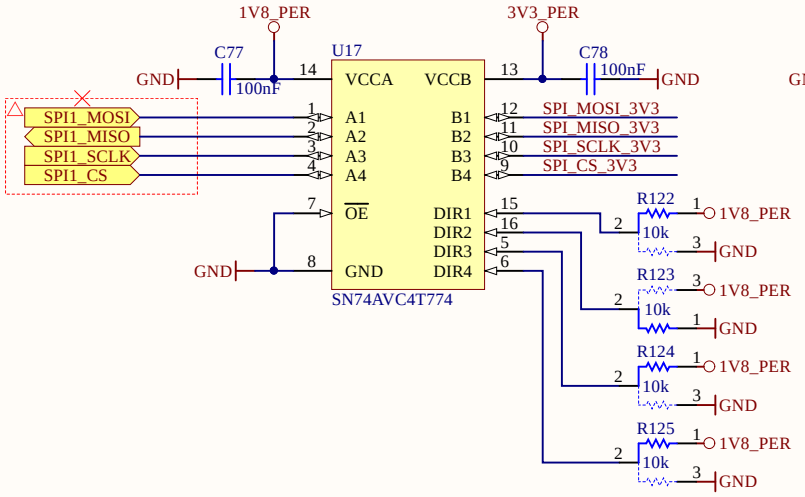


Title XMOD.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:33	Sheet 14 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			

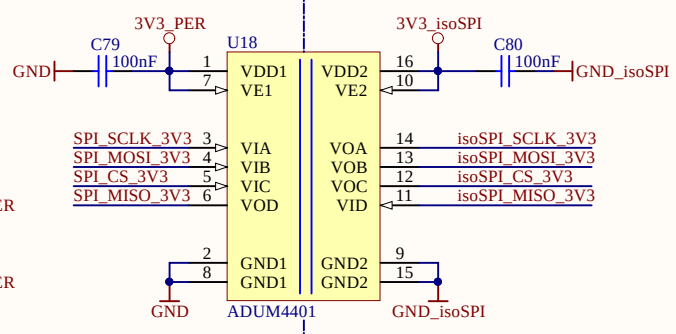


Title isoCAN.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:34	Sheet 15 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			

Level Shifting 1.8V to 3.3V



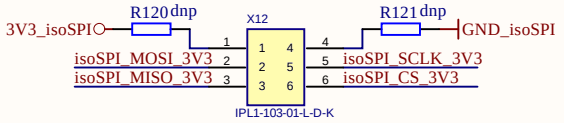
LV side / Isolated side



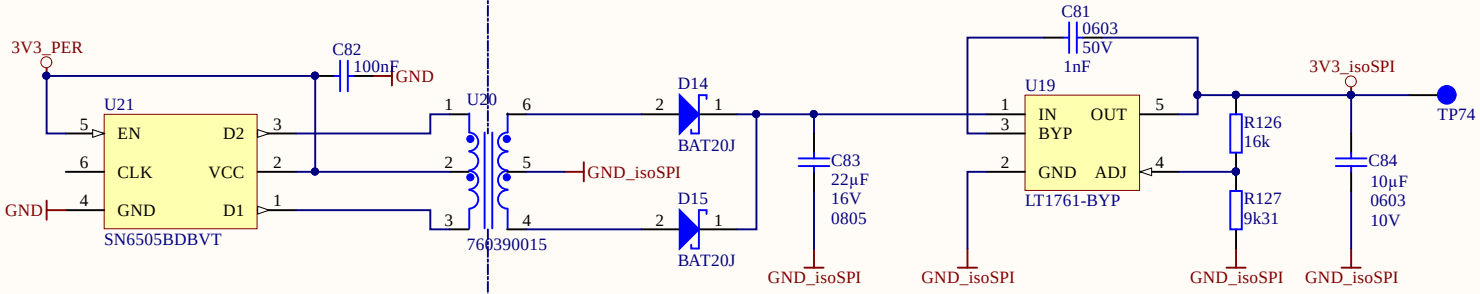
take ADUM4402 if SoC acts as SPI slave

alternative pin-compatible part: Texas Instruments ISO7741DW

SPI Connector



Isolated Power Supply



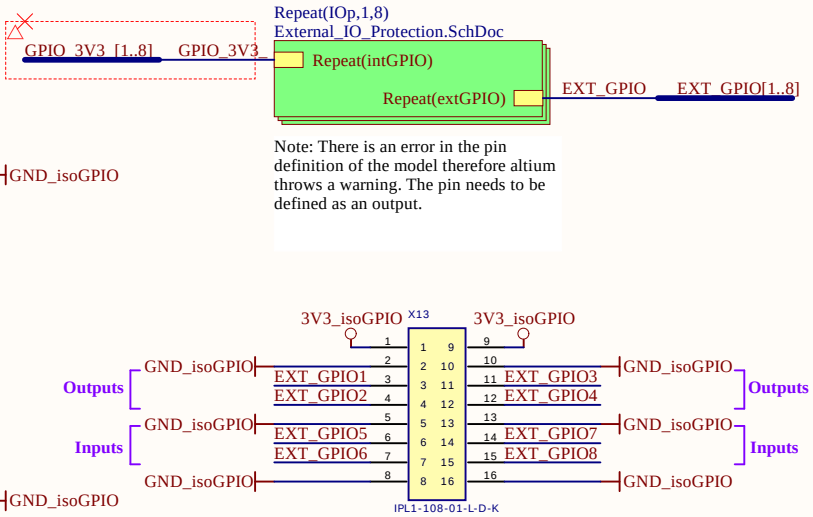
Title isoSPI.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:34	Sheet 16 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			

Bidirectional Level Shifting 1.8V to 3.3V

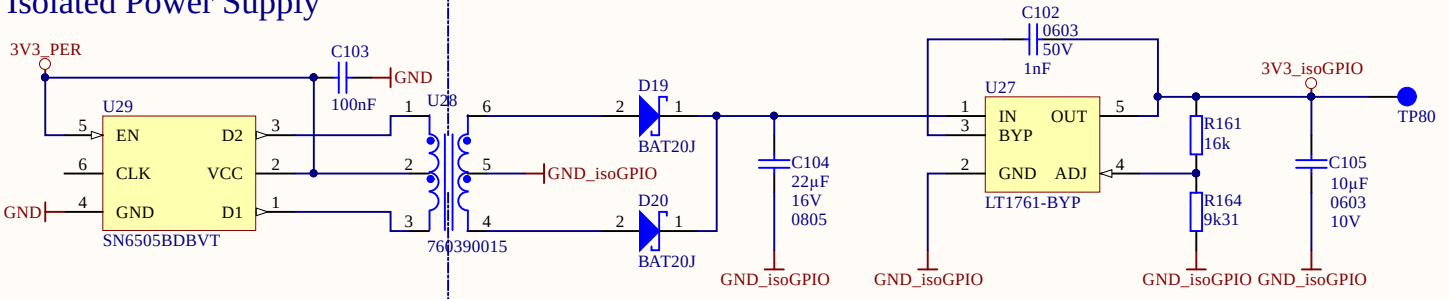
LV side

Isolated side

IO Protection with TVS-Diode and PTC-Resistor



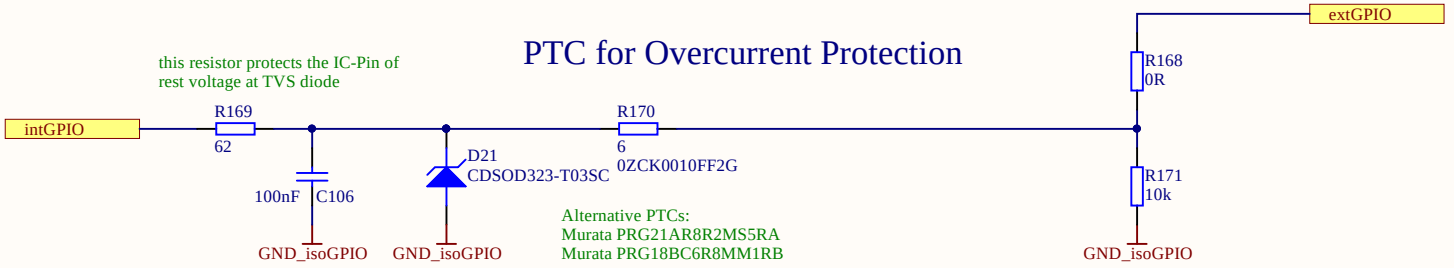
Isolated Power Supply



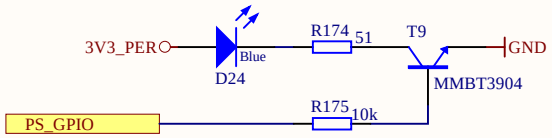
Title isoGPIO.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:34	Sheet 17 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			

Voltage Divider

PTC for Overcurrent Protection

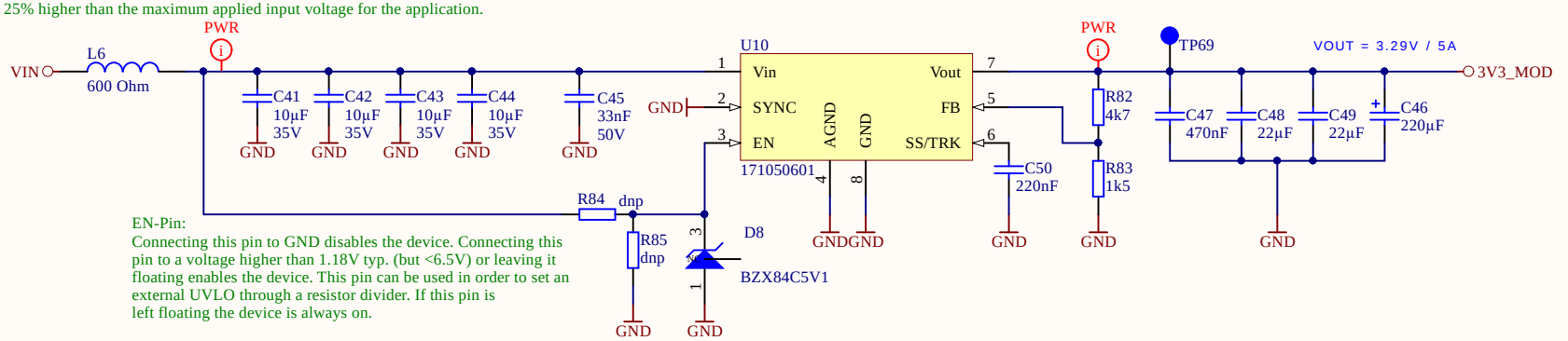


Title External_IO_Protection.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:34	Sheet 18 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			



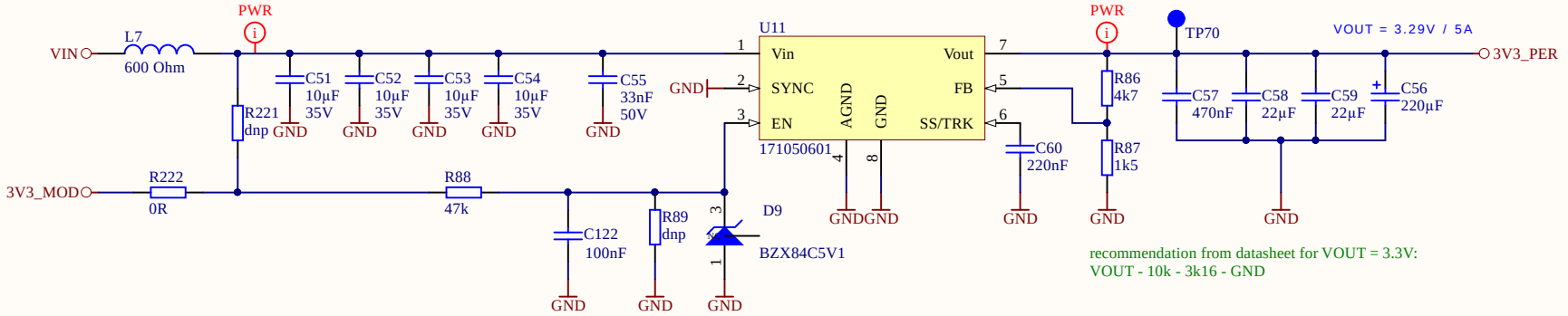
Title DiagLEDs.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020 Time: 23:24:34		Sheet 19 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			

Notes: preferred to use 2x 22µF/50V capacitors at Vin, but this design uses 35V caps due to worse availability at distributors.
Datasheet: recommended minimum input capacitance is 22 µF (including derating) ceramic with voltage rating
at least 25% higher than the maximum applied input voltage for the application.



EN-Pin:
Connecting this pin to GND disables the device. Connecting this pin to a voltage higher than 1.18V typ. (but <6.5V) or leaving it floating enables the device. This pin can be used in order to set an external UVLO through a resistor divider. If this pin is left floating the device is always on.

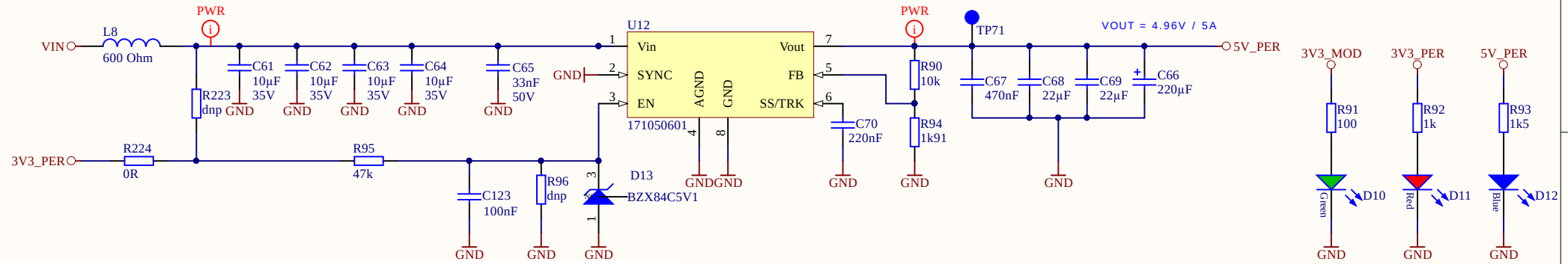
power supply for:
- Trenz module (PL_1V8, PS_1V8, ...)



power supply for:
- digital and analog sockets
- SD-Card
- Ethernet
- CAN

power supply for:
- digital and analog sockets

recommendation from datasheet for VOUT = 3.3V:
VOUT - 10k - 3k16 - GND



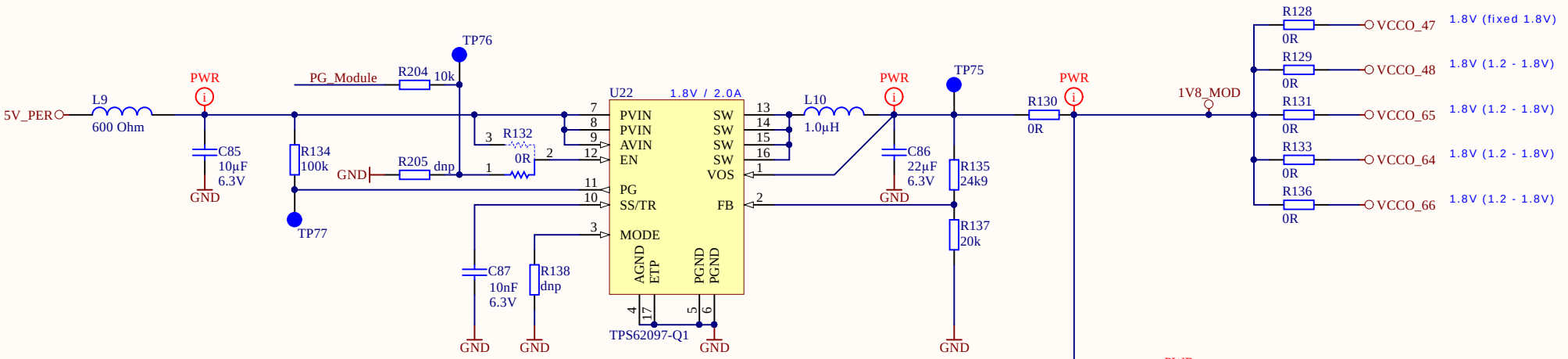
The delay time between the power supplies U10 U11 and U12 is determined by R88 C122 R95 and C123.
The delay time can be estimated as follows: t_on = -tau * ln(1-(U_en/U_max))
tau = R*C
U_en = 1,27V
U_max = output voltage of prior stage (e.g. 3V3)
Since the input current of the EN pin is about 21µA the real dealy time is a bit longer than the calculated value. With the values above there is a delay of about 5ms,

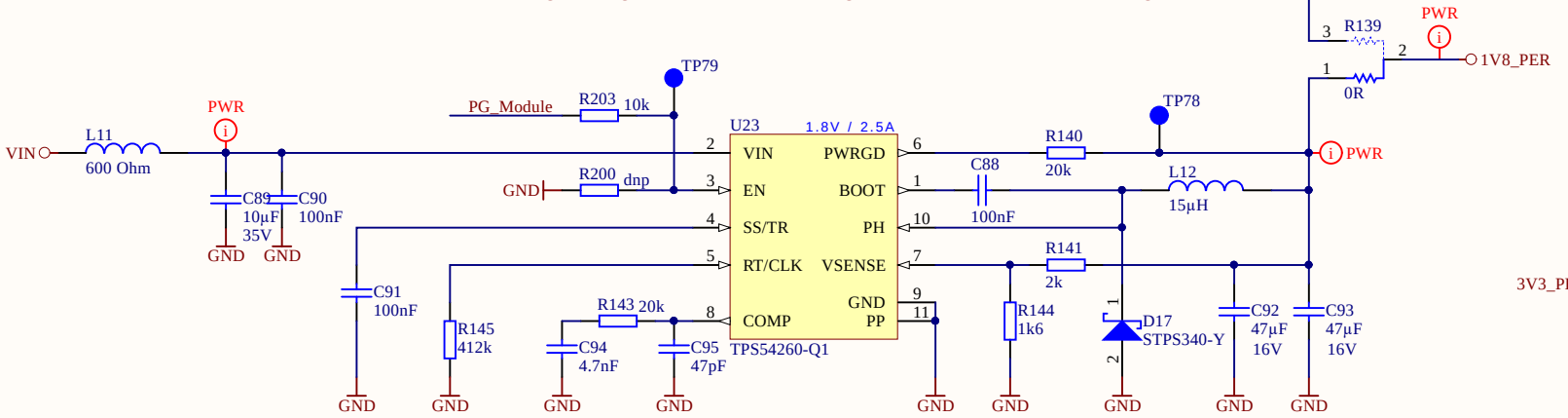
Title Power_Supply_1.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm*	
Size: A4	Revision: 3v00	*Wassertorstr. 10*	
		90489 Nürnberg	
Date: 17.06.2020	Time: 23:24:34	*GERMANY*	
Sheet 20 of 22		Author: Andreas Geiger	
Project: UltraZOhm_CarrierBoard.PrjPcb			

PG_Module

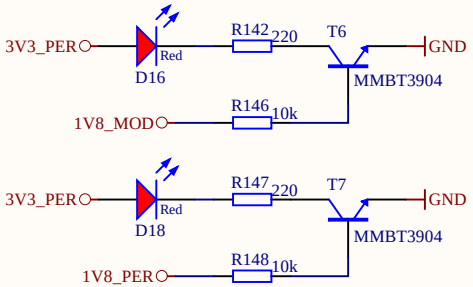
power good signal from Trenz module
to enable banks and peripherals after
module is supplied sufficiently

bank power supply with jumper selectable
(place near to Trenz module!)





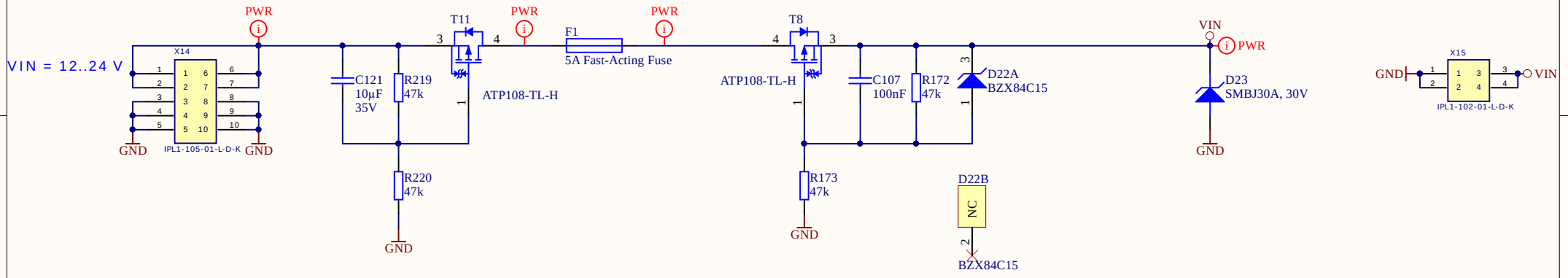
power supply for:
- CPLD Banks
- I2C Level Shifter
- Ethernet
- SD-Card Level Shifter
- JTAG Programmer
- CAN Transceiver
- SPI, UART, I2C-Interface Level Shifter
- Isolated SPI Level Shifter
- Isolated GPIO Level Shifter



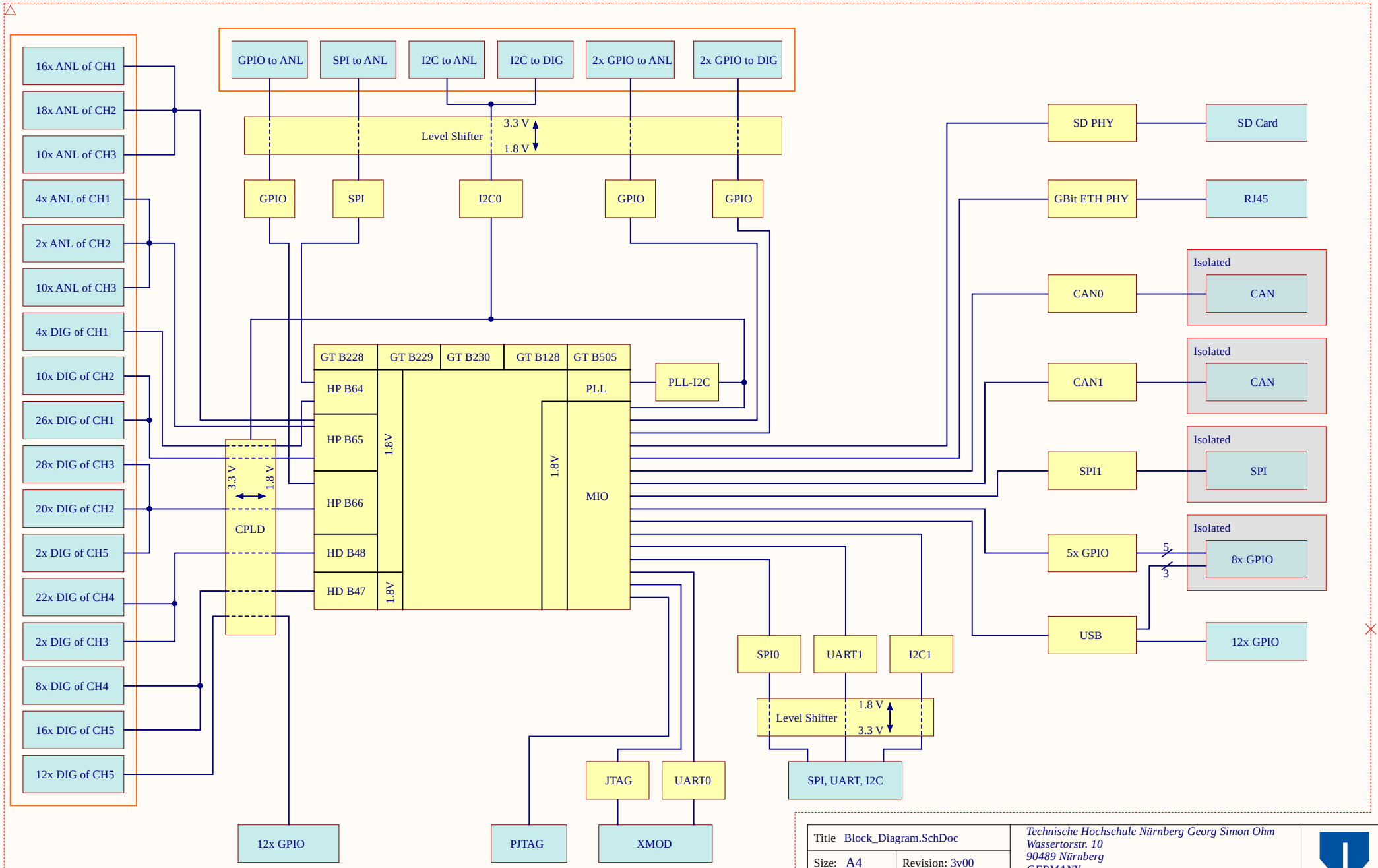
Reference Design: TE0728

Reference Design: TPS82085SIL (TE0808/POWER.SchDoc) not in stock at distributors...

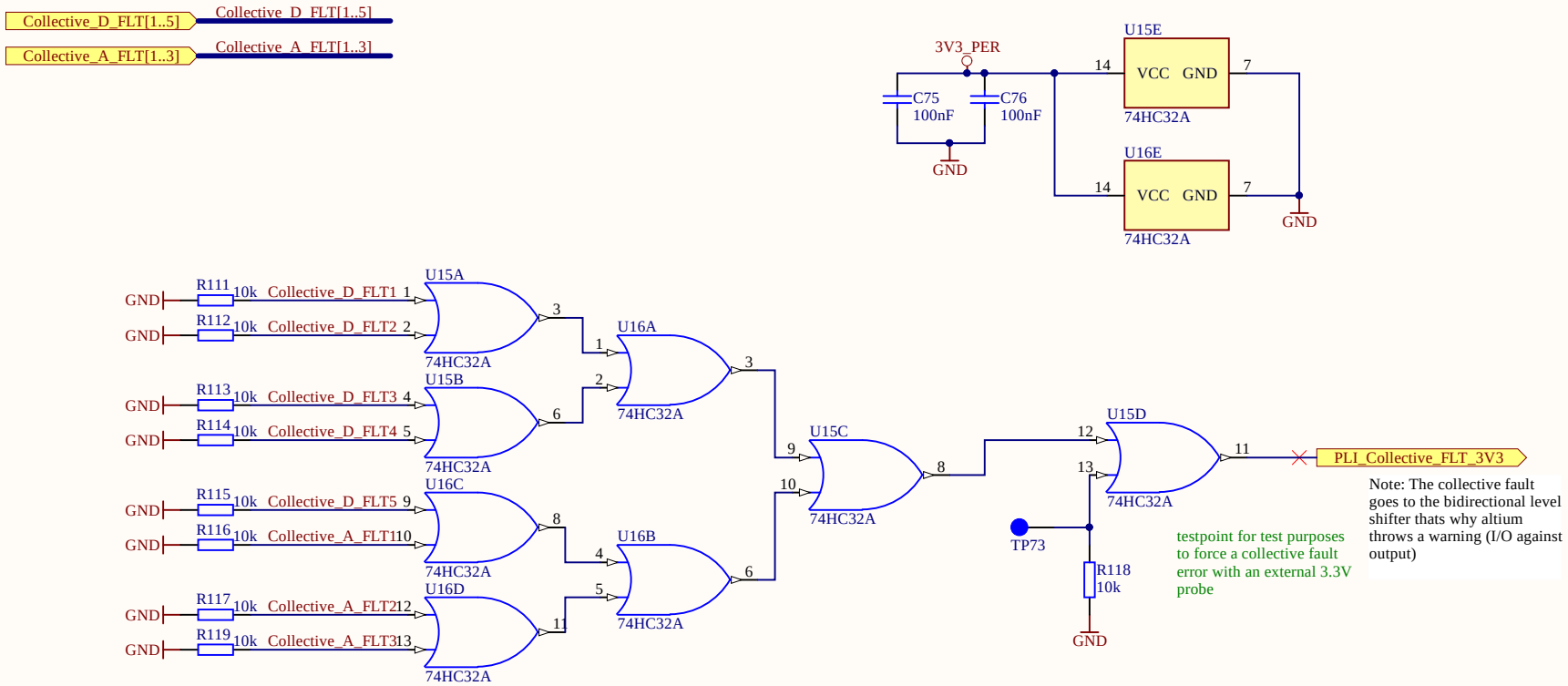
Title Power_Supply_2.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*
Size: A4	Revision: 3v00	
Date: 17.06.2020	Time: 23:24:34	Sheet 21 of 22 — Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb		



Title Power_Supply_Input.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:34	Sheet 22 of 22	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			



Title Block_Diagram.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Wassertorstr. 10* *90489 Nürnberg* *GERMANY*
Size: A4	Revision: 3v00	
Date: 17.06.2020 Time: 23:24:34	Sheet of	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb		



Title: Collective_FAULT_logic.SchDoc		*Technische Hochschule Nürnberg Georg Simon Ohm* *Fürther Straße 250* *90429 Nürnberg* *GERMANY*	
Size: A4	Revision: 3v00		
Date: 17.06.2020	Time: 23:24:34	Sheet of	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			