

Place UZ Logo from Library

Revision

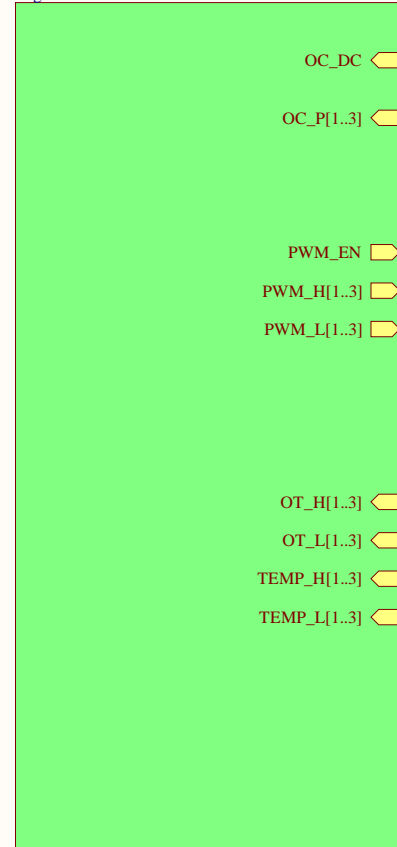
Rev03

Serial

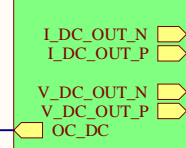
Serial #

DC-link-Caps

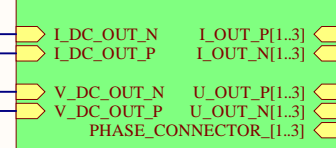
X1
DigitalCarrierJack



DC-link

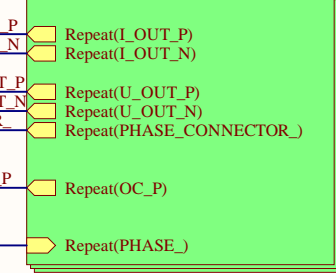


Connectors



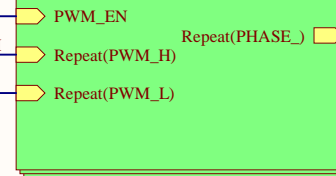
Phase_Measurements

Repeat(PhaseMeasurements,1,3)



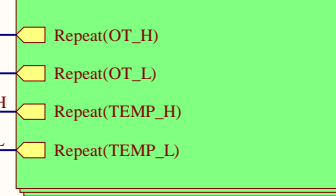
Halfbridges

Repeat(Halfbridge,1,3)



Temp_Measurements

Repeat(TempMeasurements,1,3)



INFO

Project
ProjectRevision
AuthorParam
ProjectDate

Design Information

LOGO1



UZ Logo

Title TopSheet.SchDoc

Revision: Rev03

Design Engineer: D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

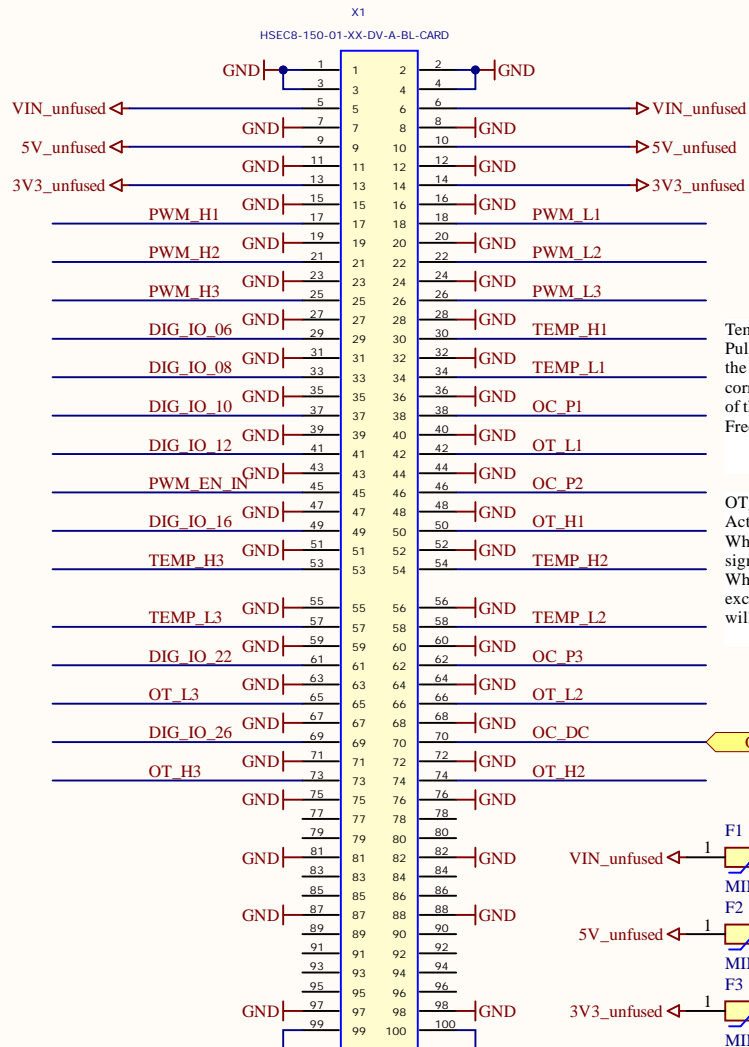
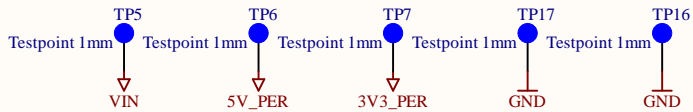
UltraZohm

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Date: 04.05.2023

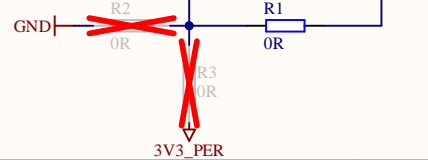
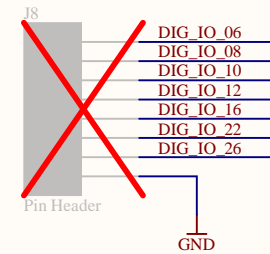
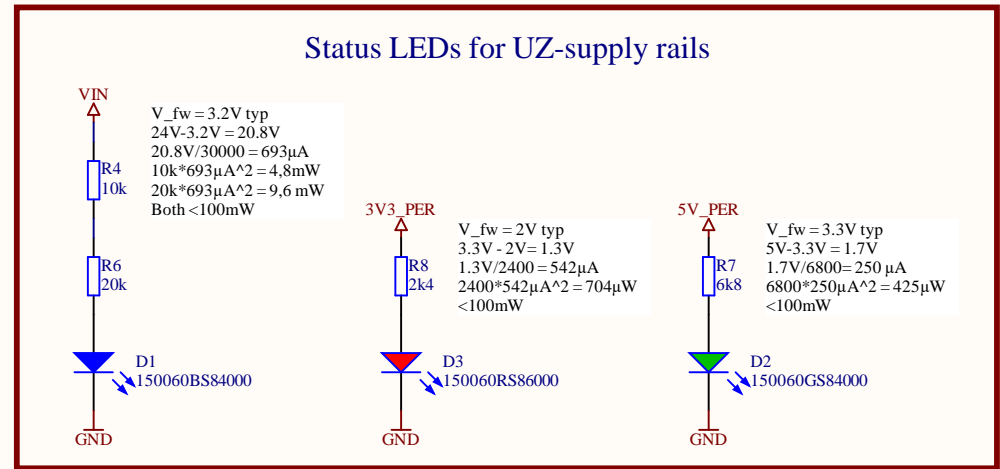
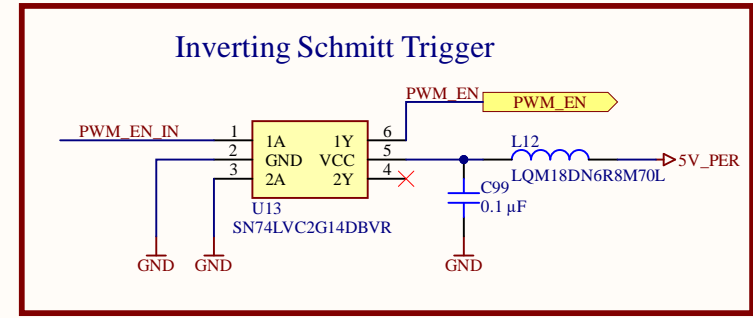
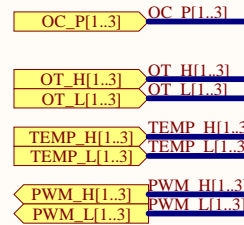
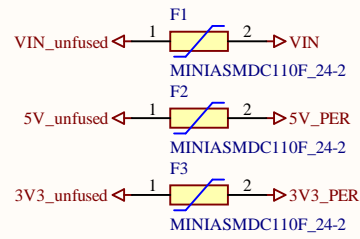
Sheet 1 of 14





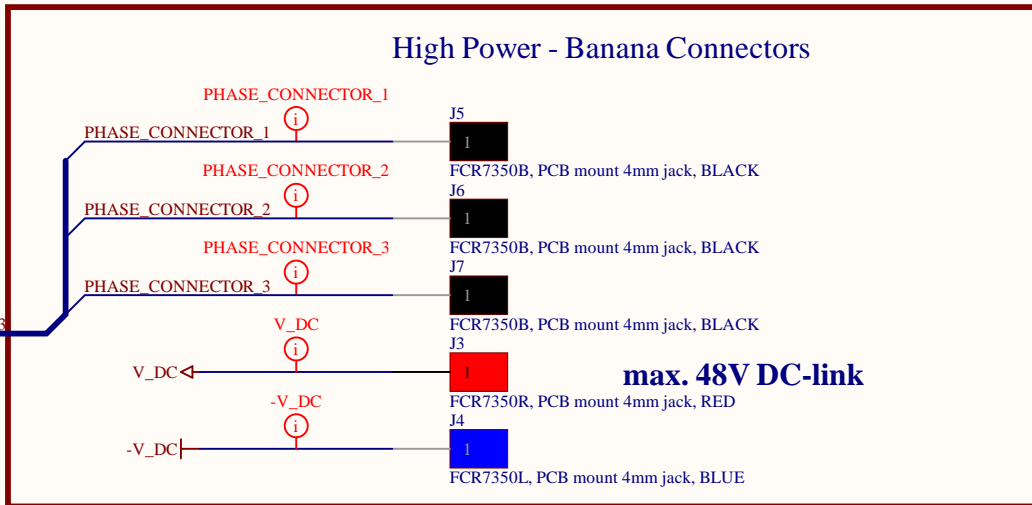
Temp_H/L signals:
Pulswidth modulated signal to the SoC. Pulswidth linear correlated to the temperature of the Mosfets
Frequency 11kHz

OT_H/L signals:
Active low signal.
When in normal operation, signal is 3V3.
When the measured temp exceeds 105°C, the OT signal will be set to LOW.

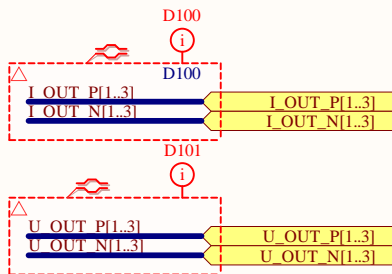


Title DigitalCarrierJack.SchDoc		
Revision: Rev03	Design Engineer: D. Hufnagel	
Project: UZ_D_Inverter.PrjPCB		www.ultrazohm.com Date: 04.05.2023 Sheet 2 of 14

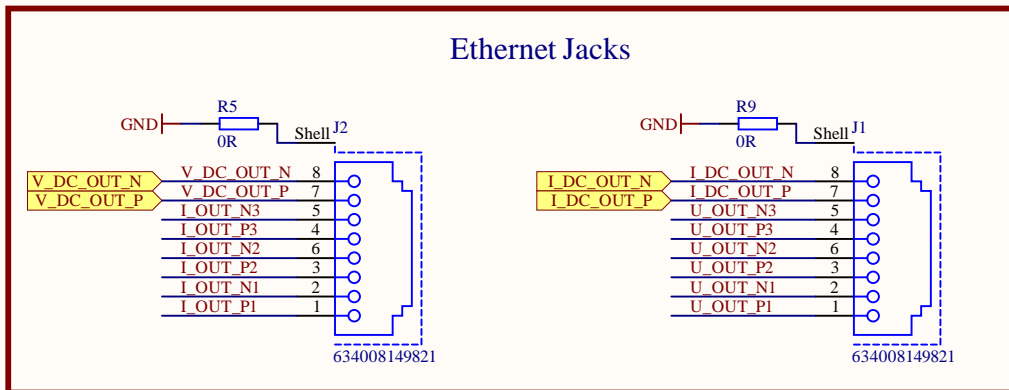
High Power - Banana Connectors



PHASE_CONNECTOR [1..3] PHASE_CONNECTOR [1..3]



Ethernet Jacks



Title Connectors.SchDoc

Revision: Rev03

Design Engineer: D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

UltraZohm

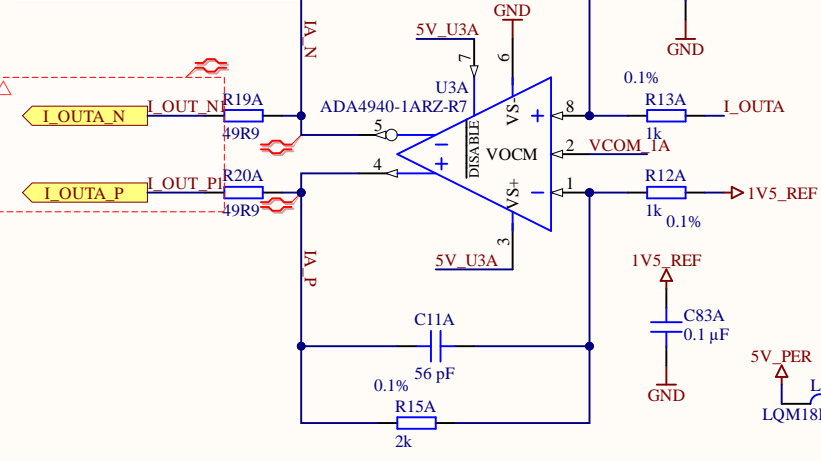
www.ultrazohm.com

Date: 04.05.2023

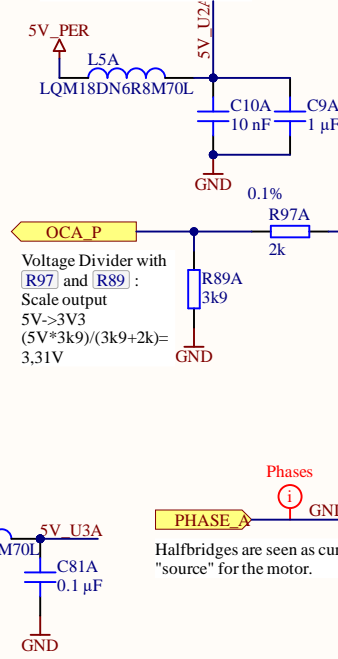
Sheet 3 of 14



With 0.3-2.7V bipolar single-ended input at 1.5Vref ->
Gain=2 would lead to a differential signal with 2.5V VCOM:
Out_N/Out_P:
3.7V/1.3V at -30A
1.3V/3.7V at 30A

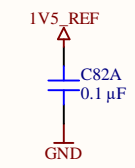


Place close to U2 OPAMP

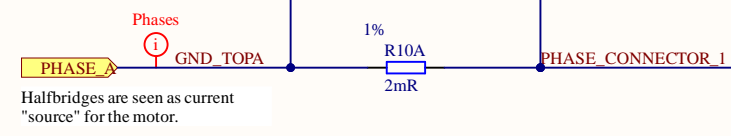


Phase Current Measurement + Single->Diff OPAMP

30A max @ 2mOhm = 60mV
With fixed 20V/V Gain and 1.5V ref ->
0.3 - 2.7V bipolar single-ended



CIP sets the trigger voltage for OCP. If OUT > (VDD-CIP) || OUT < (CIP) the OCP triggers. In an OCP event, COP is set to low. With voltage divider [R94] and [R127]
CIP=1k/(1k+3k9) * 1.5V = 0.306V
-> This translates to 29.847A



Halfbridges are seen as current "source" for the motor.

A

A

B

B

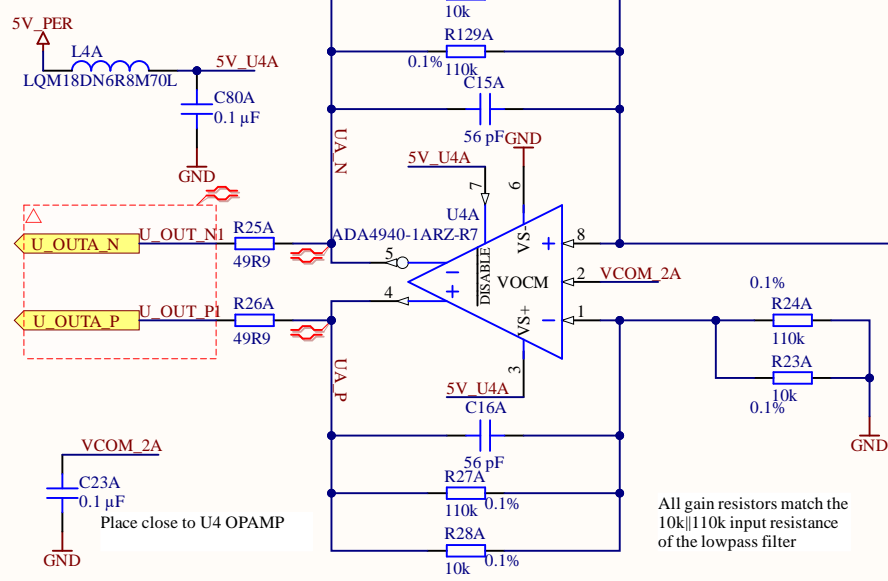
C

C

D

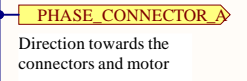
D

Phase Voltage Measurement + Single->Diff OPAMP




Voltage measurement scaled with voltage divider [R22] and [R21]:
Max 48V (LowPass max 60V as buffer)
10k||110k->
48V*10k/(10k+110k)=4V
48V/(10k||110k)=5.2mA

Max operation 60V:
60V*10k/(10k+110k)=5V
60V/(10k||110k)=6.5mA



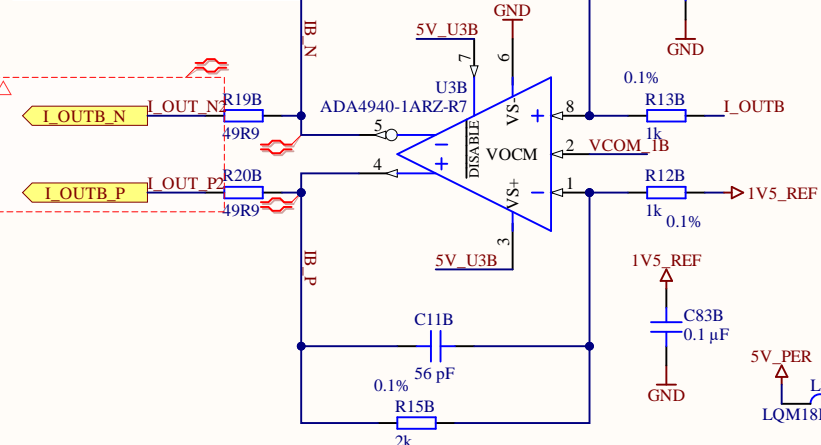
LowPass Filter:
Max Target:
6000rpm at 20 pole pairs
->fg=2000Hz
With R=10k||110k ->C=8.68nF:
Closes values:
3.3nF and 4.7nF ->2170 Hz=fg

All gain resistors match the 10k||110k input resistance of the lowpass filter

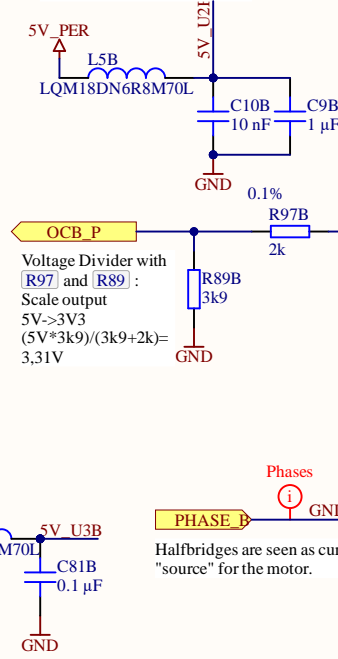
Title Phase_Measurements.SchDoc		
Revision: Rev03	Design Engineer: D. Hufnagel	
Project: UZ_D_Inverter.PrjPCB		

www.ultrazohm.com Date: 04.05.2023 Sheet 4.1 of 14

With 0.3-2.7V bipolar single-ended input at 1.5Vref ->
 Gain=2 would lead to a differential signal with 2.5V VCOM:
 Out_N/Out_P:
 3.7V/1.3V at -30A
 1.3V/3.7V at 30A

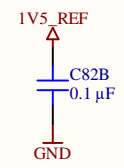
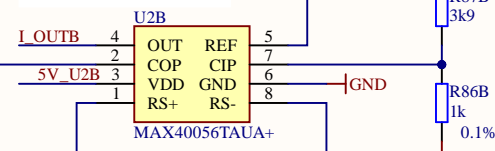


Place close to U2 OPAMP

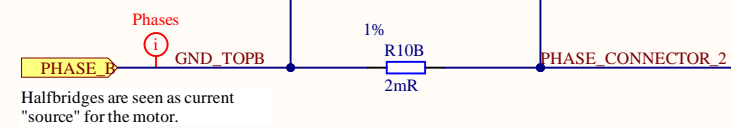


Phase Current Measurement + Single->Diff OPAMP

30A max @ 2mOhm = 60mV
 With fixed 20V/V Gain and 1.5V ref ->
 0.3 - 2.7V bipolar single-ended



CIP sets the trigger voltage for OCP. If OUT > (VDD-CIP) || OUT < (CIP) the OCP triggers. In an OCP event, COP is set to low. With voltage divider [R94] and [R127]
 $CIP = 1k / (1k + 3k9) * 1.5V = 0.306V$
 -> This translates to 29.847A



Halfbridges are seen as current "source" for the motor.

A

A

B

B

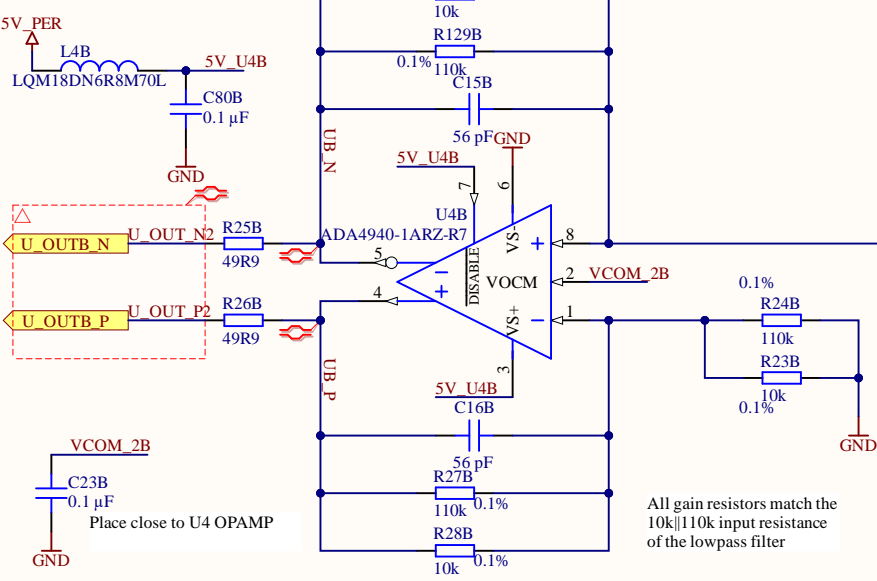
C

C

D

D

Phase Voltage Measurement + Single->Diff OPAMP




Voltage measurement scaled with voltage divider [R22] and [R21]:
 Max 48V (LowPass max 60V as buffer)
 $10k || 110k >>$
 $48V * 10k / (10k + 110k) = 4V$
 $48V / (10k || 110k) = 5.2mA$
 Max operation 60V:
 $60V * 10k / (10k + 110k) = 5V$
 $60V / (10k || 110k) = 6.5mA$

PHASE_CONNECTOR_B
 Direction towards the connectors and motor

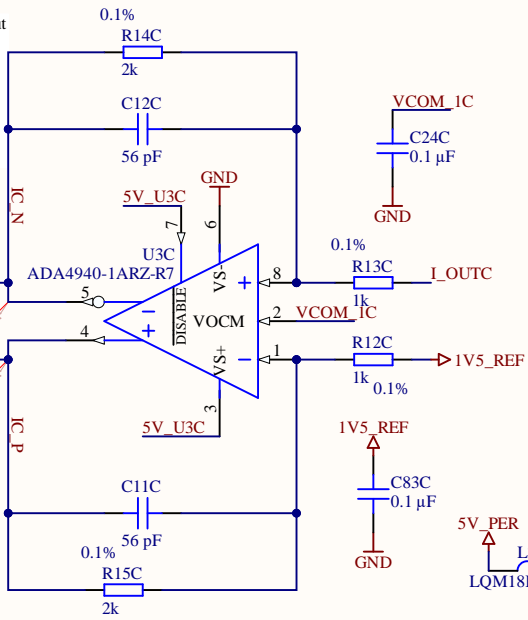
LowPass Filter:
 Max Target:
 6000rpm at 20 pole pairs
 -> $f_g = 2000Hz$
 With $R = 10k || 110k >> C = 8.68nF$:
 Closes values:
 3.3nF and 4.7nF -> 2170 Hz = f_g

All gain resistors match the $10k || 110k$ input resistance of the lowpass filter

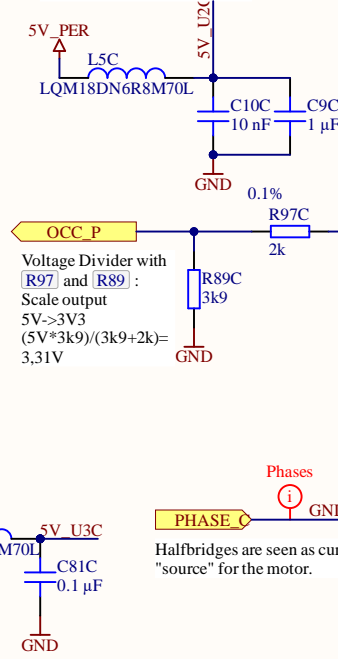
Title Phase_Measurements.SchDoc		
Revision: Rev03	Design Engineer: D. Hufnagel	
Project: UZ_D_Inverter.PrjPCB	Date: 04.05.2023	

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 Date: 04.05.2023
 Sheet 4.2 of 14

With 0.3-2.7V bipolar single-ended input at 1.5Vref ->
 Gain=2 would lead to a differential signal with 2.5V VCOM:
 Out_N/Out_P:
 3.7V/1.3V at -30A
 1.3V/3.7V at 30A

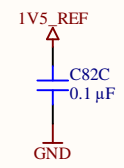


Place close to U2 OPAMP

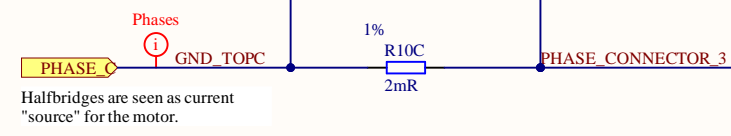


Phase Current Measurement + Single->Diff OPAMP

30A max @ 2mOhm = 60mV
 With fixed 20V/V Gain and 1.5V ref ->
 0.3 - 2.7V bipolar single-ended



CIP sets the trigger voltage for OCP. If OUT > (VDD-CIP) || OUT < (CIP) the OCP triggers. In an OCP event, COP is set to low. With voltage divider R94 and R127
 $CIP = 1k / (1k + 3k9) * 1.5V = 0.306V$
 -> This translates to 29.847A



A

A

B

B

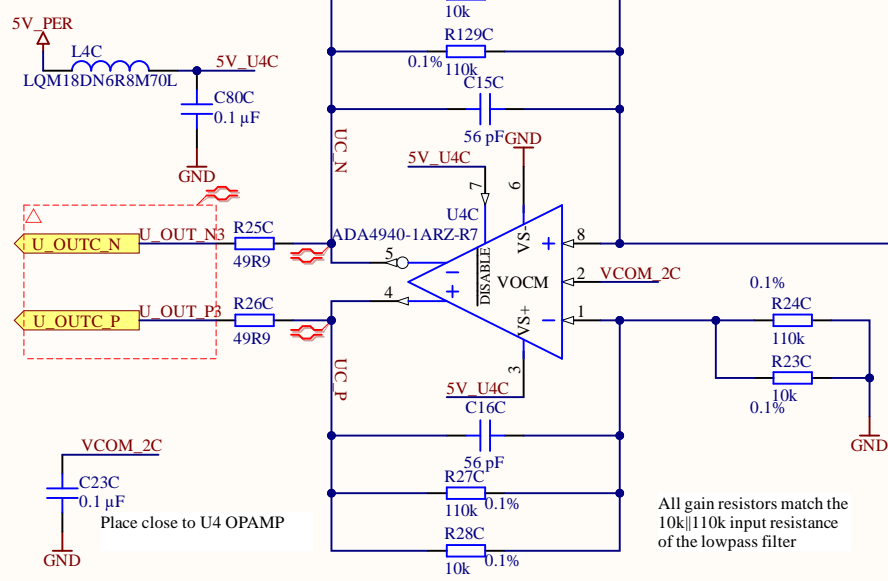
C

C

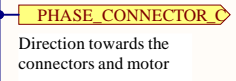
D

D

Phase Voltage Measurement + Single->Diff OPAMP




Voltage measurement scaled with voltage divider R22 and R21:
 Max 48V (LowPass max 60V as buffer)
 $10k || 110k >$
 $48V * 10k / (10k + 110k) = 4V$
 $48V / (10k || 110k) = 5.2mA$
 Max operation 60V:
 $60V * 10k / (10k + 110k) = 5V$
 $60V / (10k || 110k) = 6.5mA$



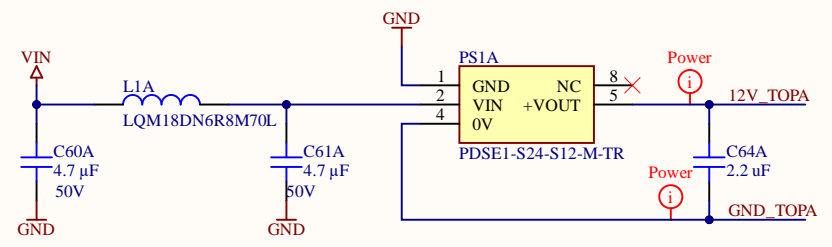
LowPass Filter:
 Max Target:
 6000rpm at 20 pole pairs
 -> fg=2000Hz
 With R=10k||110k -> C=8.68nF:
 Closes values:
 3.3nF and 4.7nF -> 2170 Hz=fg

All gain resistors match the 10k||110k input resistance of the lowpass filter

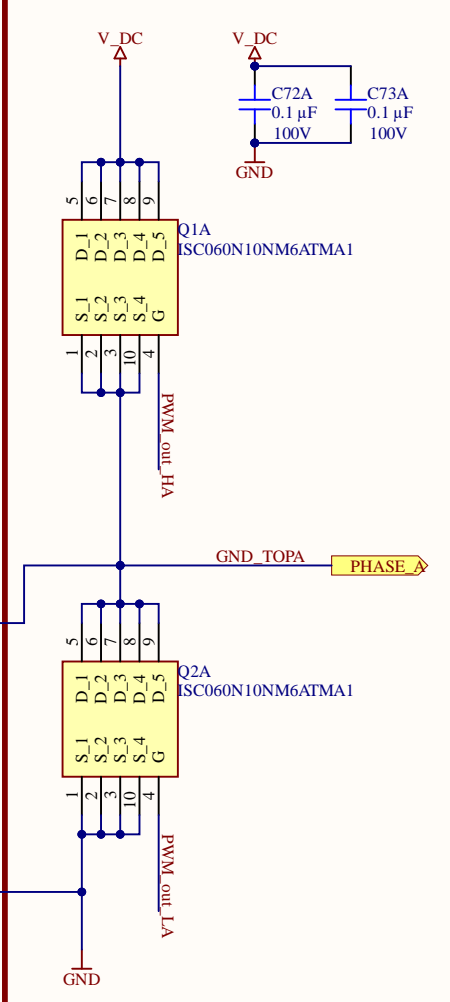
Title Phase_Measurements.SchDoc		
Revision: Rev03	Design Engineer: D. Hufnagel	
Project: UZ_D_Inverter.PrjPCB	Date: 04.05.2023	

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 Date: 04.05.2023
 Sheet 4.3 of 14

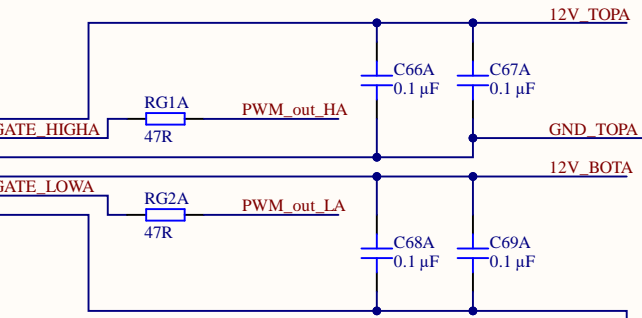
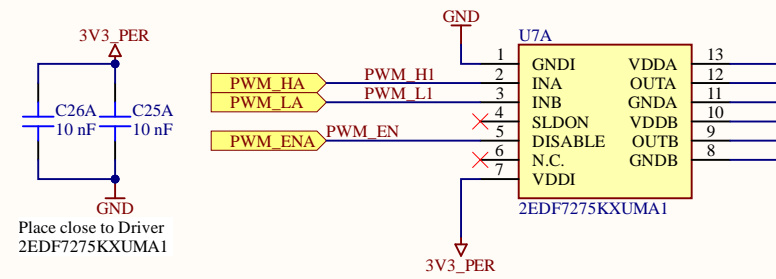
Isolated Top Side Gate Supply



MOSFETS



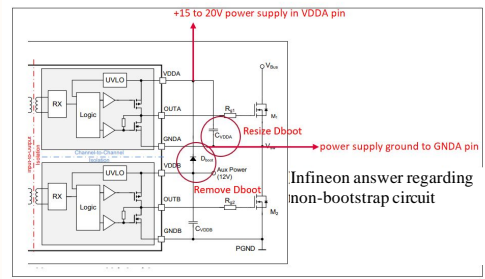
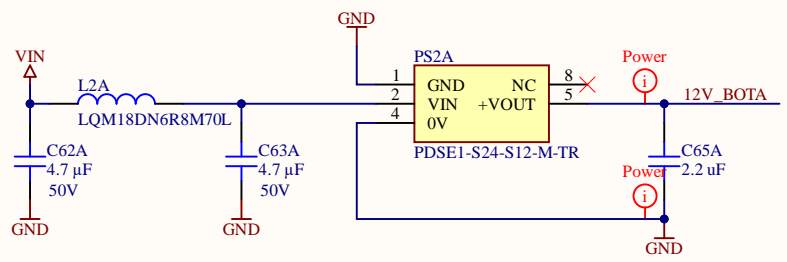
Gate Driver




IG_charging_peak <4A
 IG_discharging_peak <8A
 ->Max currents:
 IG_charging = 12V/(47+0.42)Ohm = 253mA
 IG_discharging = 12V/(47 + 0.18)Ohm = 254mA

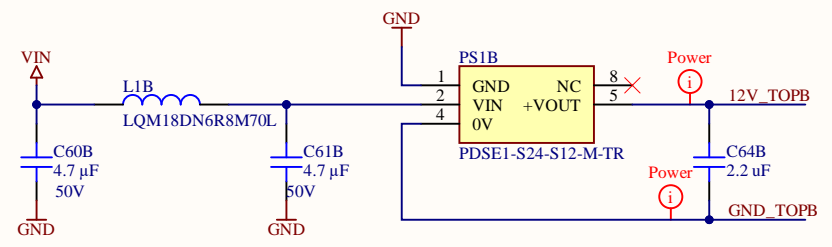
Datasheet said minimum
 20x CISS for
 output-caps:
 2x100nF > 20x2.5nF

Isolated Bottom Side Gate Supply

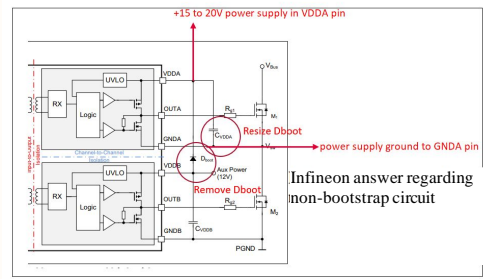
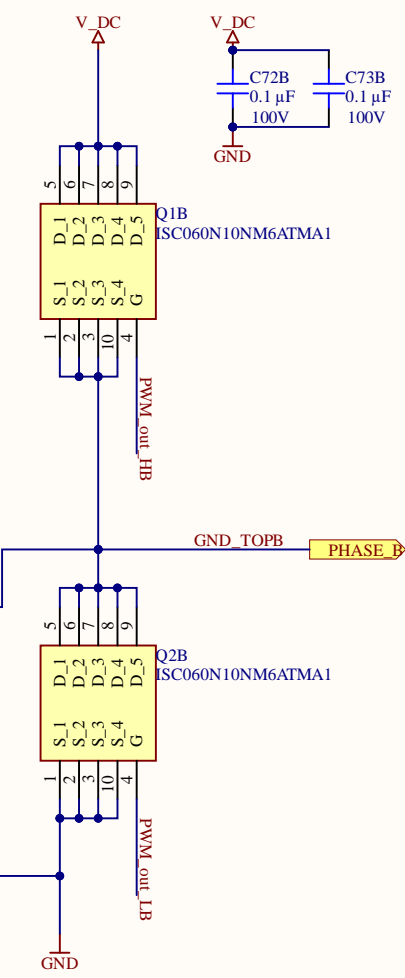


Title Halfbridges.SchDoc		
Revision: Rev03	Design Engineer: D. Hufnagel	
Project: UZ_D_Inverter.PrbPCB		
		www.ultrazohm.com Date: 04.05.2023 Sheet 5.1 of 14

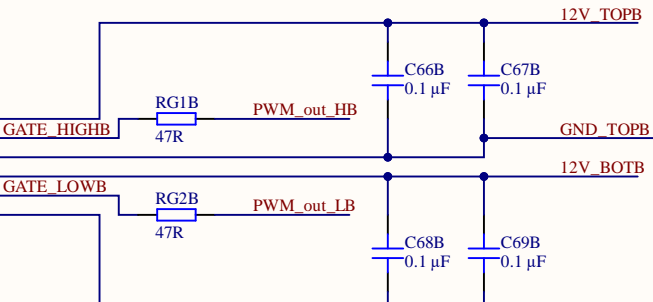
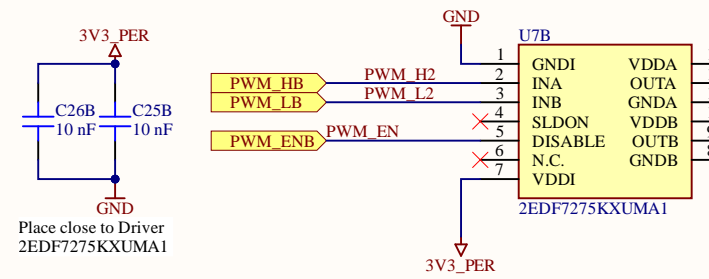
Isolated Top Side Gate Supply



MOSFETS



Gate Driver

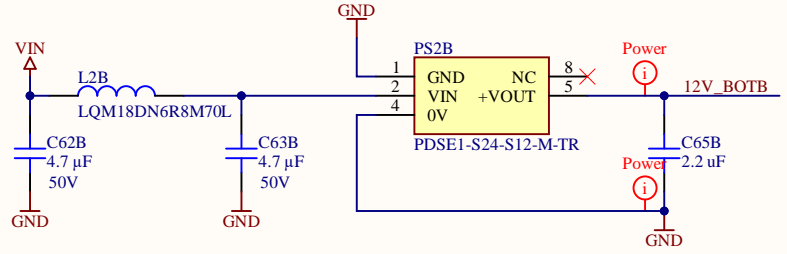



IG_charging_peak <4A
 IG_discharging_peak <8A

->Max currents:
 IG_charging = 12V/(47+0.42)Ohm = 253mA
 IG_discharging = 12V/(47 + 0.18)Ohm = 254mA

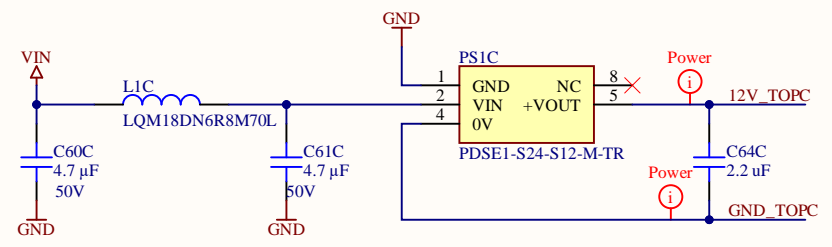
Datasheet said minimum
 20x CISS for
 output-caps:
 2x100nF > 20x2.5nF

Isolated Bottom Side Gate Supply

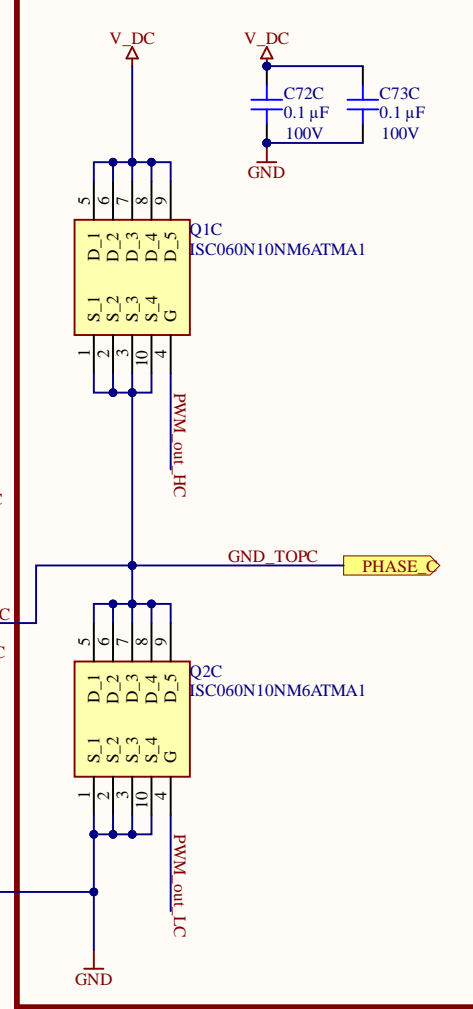


Title Halfbridges.SchDoc		
Revision: Rev03	Design Engineer: D. Hufnagel	
Project: UZ_D_Inverter.PrjPCB		
Date: 04.05.2023		Sheet 5.2 of 14

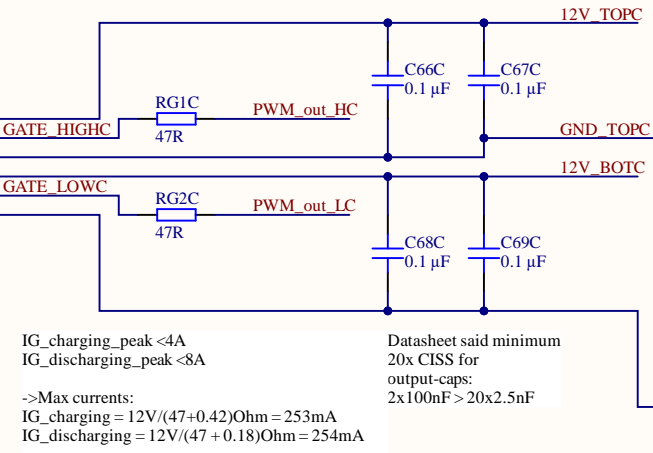
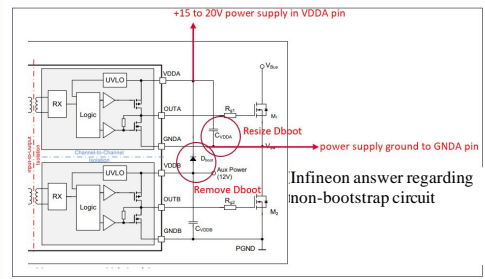
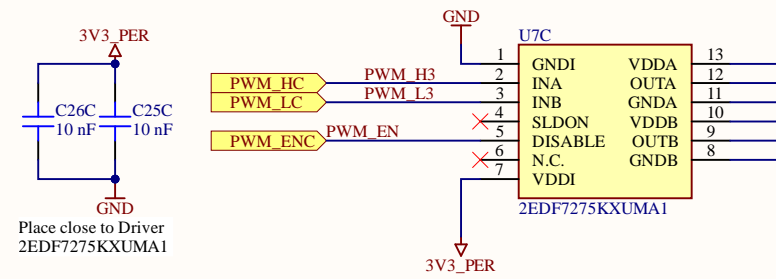
Isolated Top Side Gate Supply



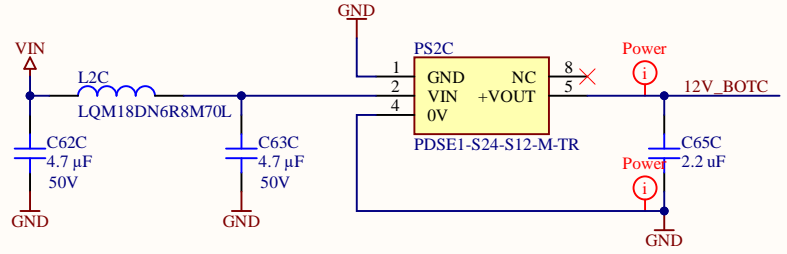
MOSFETS




Gate Driver



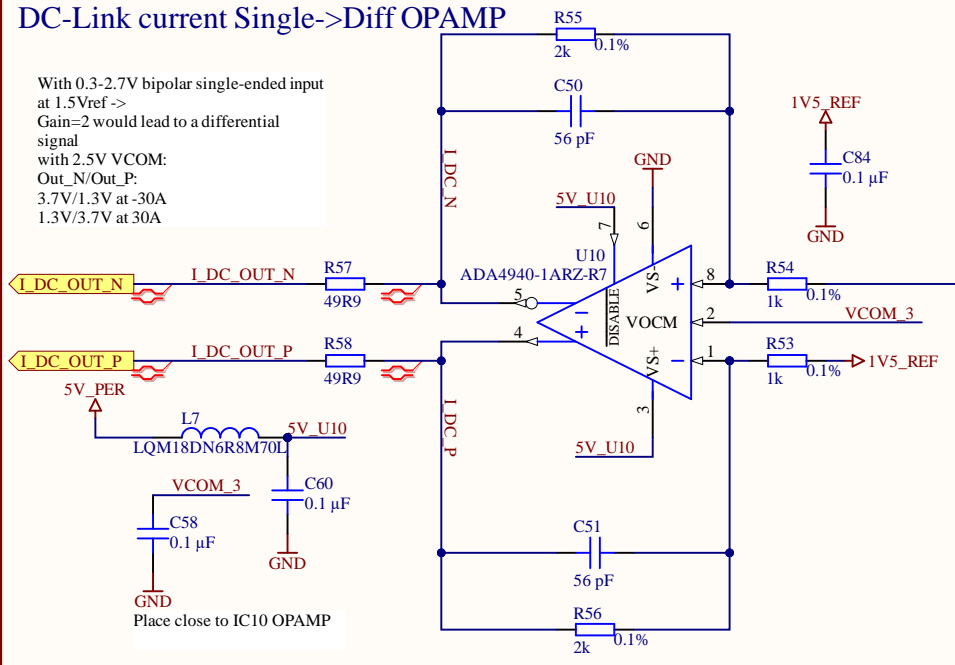
Isolated Bottom Side Gate Supply



Title Halfbridges.SchDoc		
Revision: Rev03	Design Engineer: D. Hufnagel	
Project: UZ_D_Inverter.PrjPCB		
Date: 04.05.2023		Sheet 5.3 of 14

DC-Link current Single->Diff OPAMP

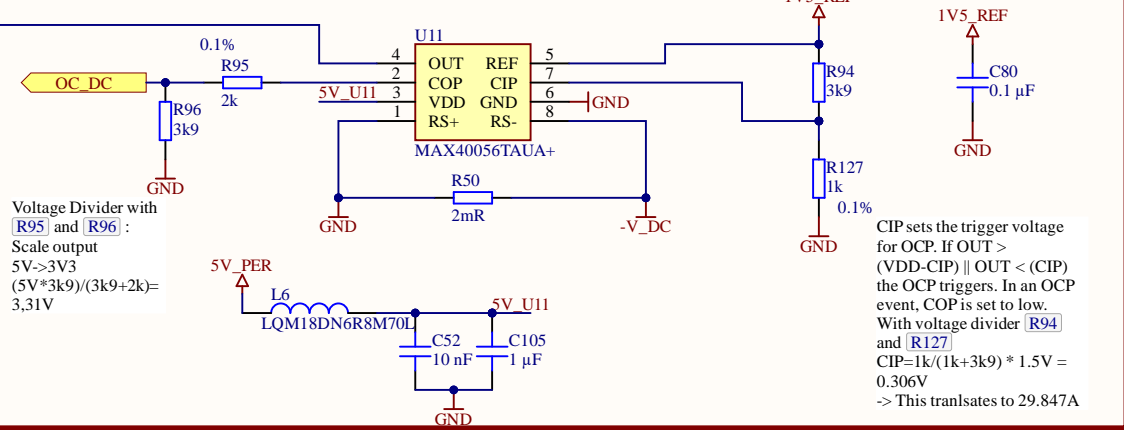
With 0.3-2.7V bipolar single-ended input at 1.5Vref ->
 Gain=2 would lead to a differential signal with 2.5V VCOM:
 Out_N/Out_P:
 3.7V/1.3V at -30A
 1.3V/3.7V at 30A



Place close to IC10 OPAMP

30A max @2mOhm = 60mV
 With fixed 20V/V Gain and 1.5V ref ->
 0.3 - 2.7V bipolar single-ended

DC-Link current measurement

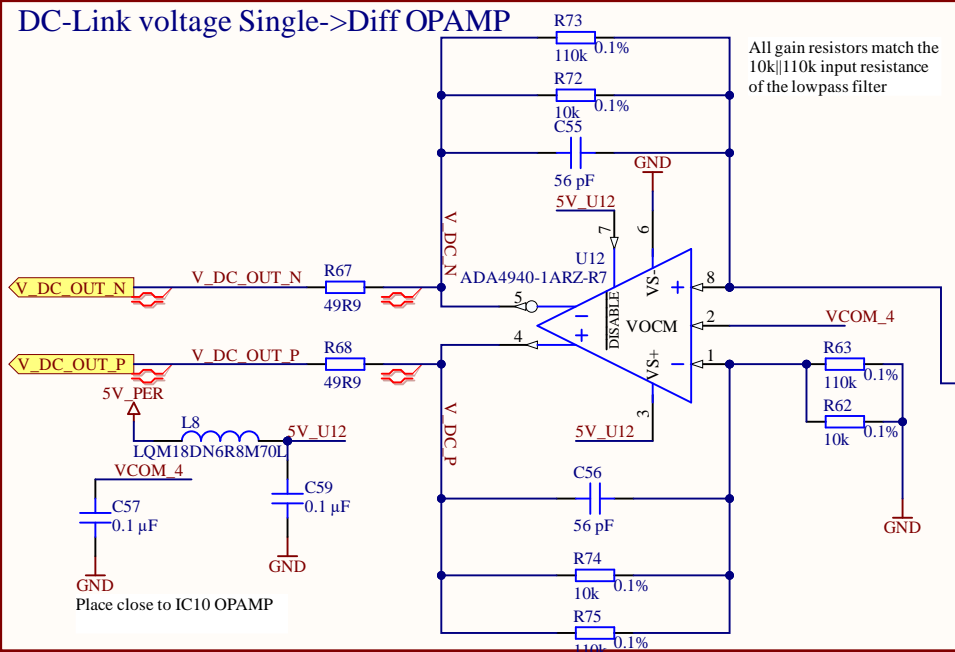


Voltage Divider with [R95] and [R96] :
 Scale output 5V->3V3
 $(5V * 3k9) / (3k9 + 2k) = 3,31V$

CIP sets the trigger voltage for OCP. If $OUT > (VDD - CIP) \parallel OUT < (CIP - VDD)$ the OCP triggers. In an OCP event, COP is set to low. With voltage divider [R94] and [R127] $CIP = 1k / (1k + 3k9) * 1.5V = 0,306V$
 -> This translates to 29.847A

DC-Link voltage Single->Diff OPAMP

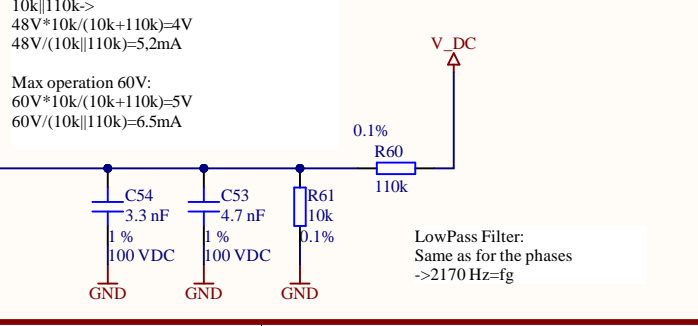
All gain resistors match the 10k||110k input resistance of the lowpass filter



Place close to IC10 OPAMP

Voltage measurement scaled with voltage divider [R60] and [R61] :
 Max 48V (LowPass max 60V as buffer)
 $10k \parallel 110k >$
 $48V * 10k / (10k + 110k) = 4V$
 $48V / (10k \parallel 110k) = 5,2mA$

DC-Link Voltage lowpass



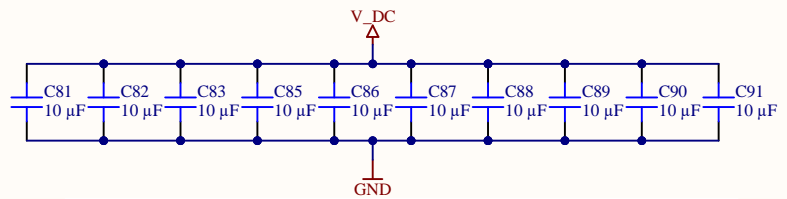
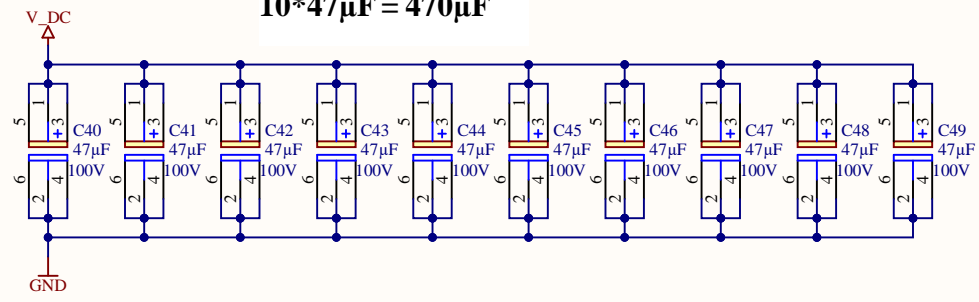
LowPass Filter:
 Same as for the phases
 -> 2170 Hz = fg

Title DC-link.SchDoc	
Revision: Rev03	Design Engineer: D. Hufnagel
Project: UZ_D_Inverter.PrjPCB	

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 Sheet 6 of 14




10*47µF = 470µF

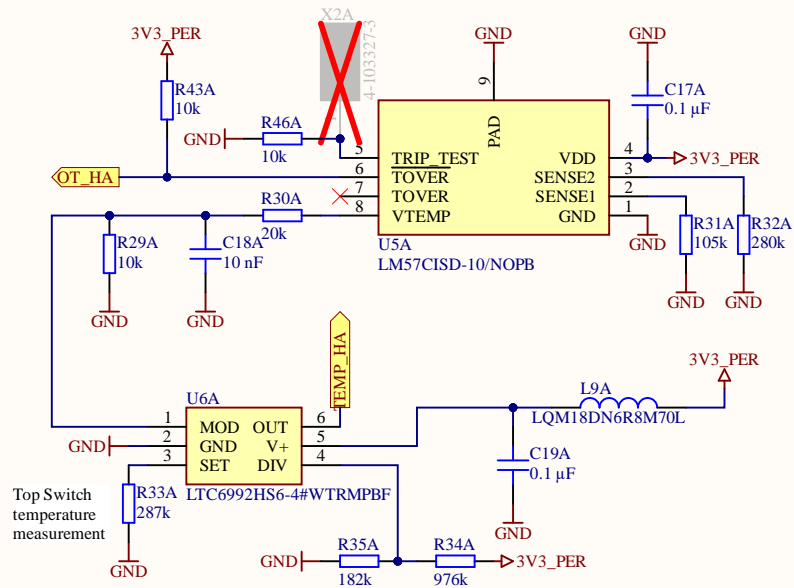


Additional MLCC caps with low internal R
10*10µF = 100µF

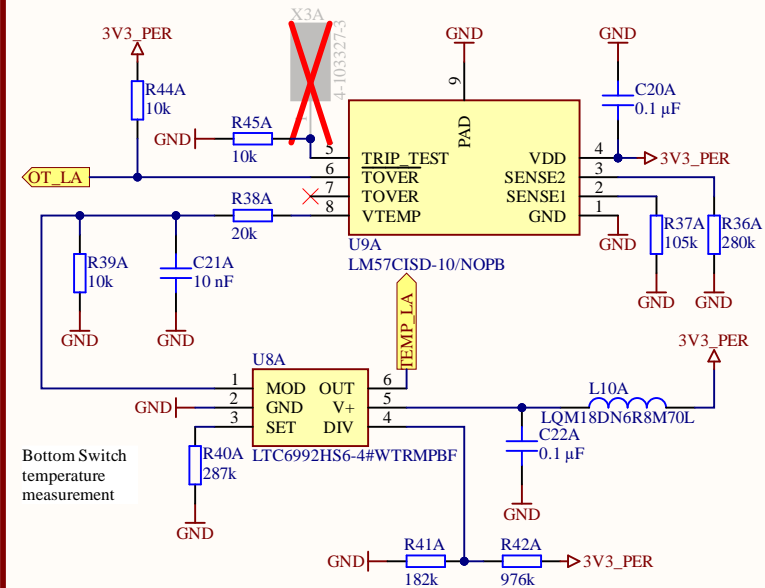
Total DC-Link capacitance
470µF + 100µF = 570 µF

Title DC-Link-Caps.SchDoc		
Revision: Rev03	Design Engineer: D. Hufnagel	
Date: 04.05.2023		
Project: UZ_D_Inverter.PrjPCB		Sheet 7 of 14

Top MOSFET Temp Measurement



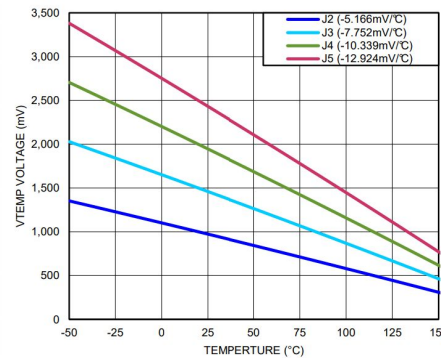
Bottom MOSFET Temp Measurement



$R_SENSE1 = \left(\frac{R31}{R37} \right) = 105k$
 $R_SENSE2 = \left(\frac{R32}{R36} \right) = 280k$
 is Gain
 ->J4 ->Leads to:
 1.11V@105°C
 2.00V@20°C

VTEMP has voltage divider with 20k/10k:
 MOD input voltages->
 $1.11V * 10 / (10+20) = 0.37V @ 105^\circ C$
 $2.00V * 10 / (10+20) = 0.67V @ 20^\circ C$

MOD input should be between 0.14V and 0.9V



Title Temp_Measurements.SchDoc

Revision: Rev03 Design Engineer: D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

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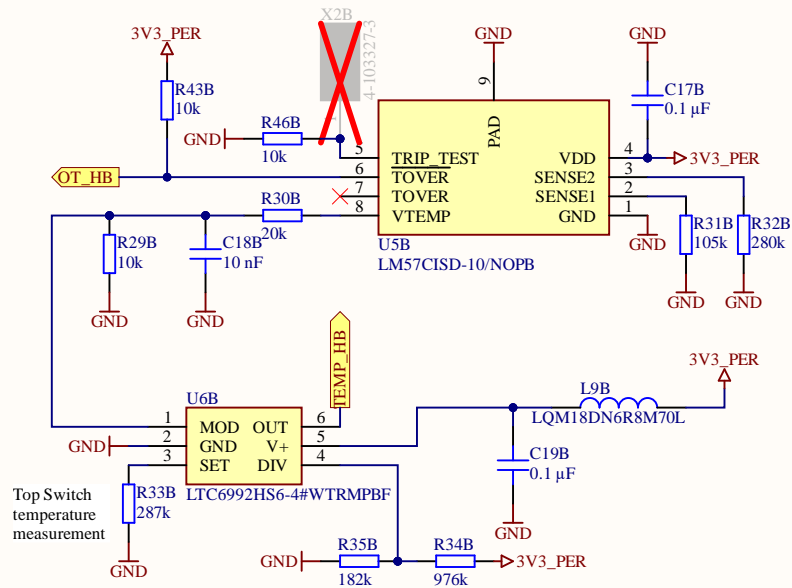
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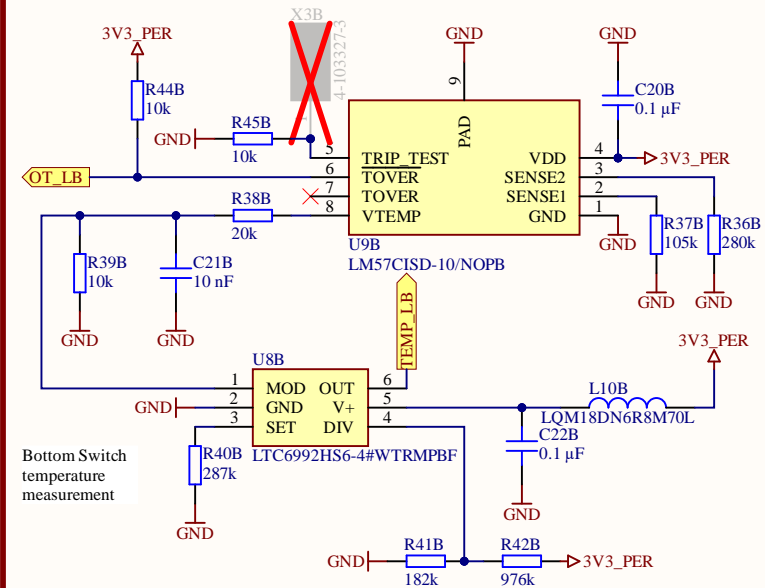
Sheet 8.1 of 14



Top MOSFET Temp Measurement



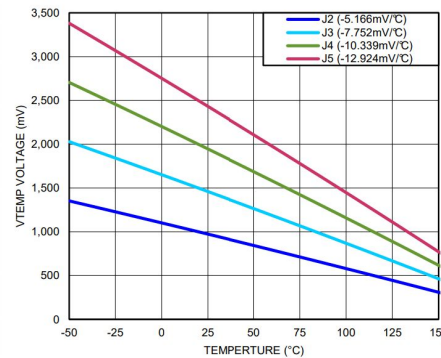
Bottom MOSFET Temp Measurement



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Title Temp_Measurements.SchDoc

Revision: Rev03 Design Engineer: D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

UltraZohm

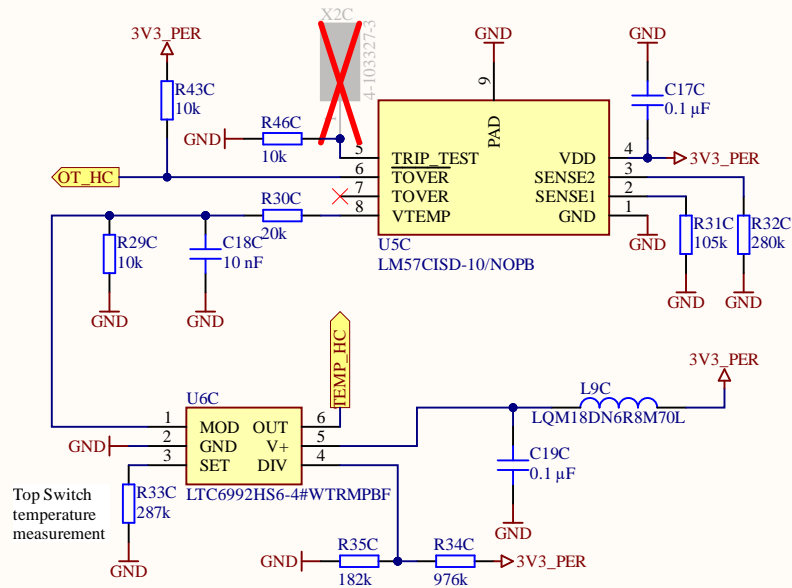
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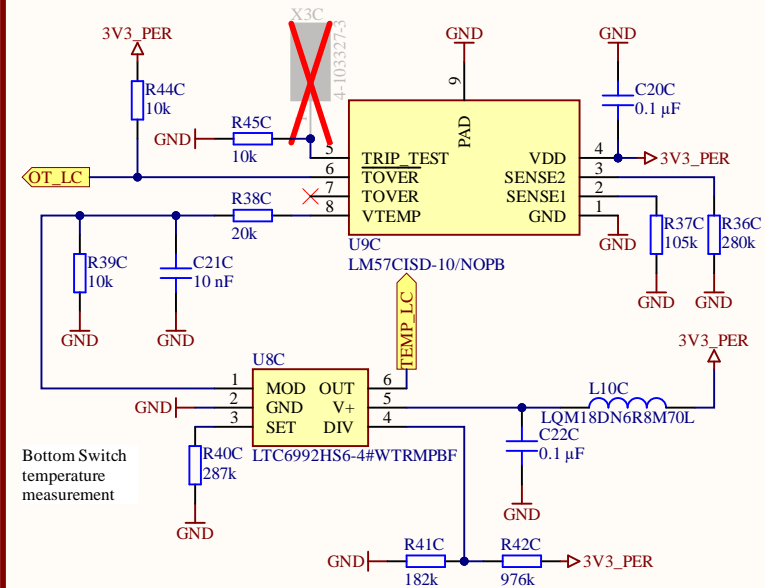
Sheet 8.2 of 14



Top MOSFET Temp Measurement



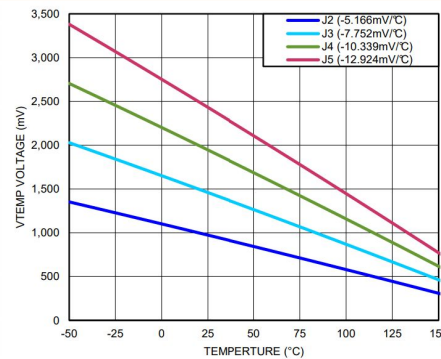
Bottom MOSFET Temp Measurement



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 $R_SENSE2 \left(\frac{R32}{R36} \right) = 280k$
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MOD input should be between 0.14V and 0.9V



Title Temp_Measurements.SchDoc

Revision: Rev03 Design Engineer: D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

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Sheet 8.3 of 14

