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Interfacing a Two-Level Silicon Carbide Inverter to a Rapid Control Prototyping Platform

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Interfacing a Two-Level Silicon Carbide Inverter to a Rapid Control Prototyping Platform

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Declaration

The work in this thesis is based on research carried out at the Chair of High-Power Converter Systems, Technical University of Munich (TUM), supervised by M.Sc. Eyke Aufderheide. No part of this thesis has been submitted elsewhere for any other academic degree or qualification, and it is all my own work unless referenced to the contrary in the text.

Place, Date, Signature

Abstract

With the rapid electrification of industries and the drive towards renewable energy integration, power converters have increasingly begun to play an important role, specifically in sectors such as transportation, energy, and industrial automation. Recent trends in the power electronics industry indicate a clear shift toward higher energy efficiency, more compact designs, and the implementation of advanced control algorithms. Due to this, control systems with increased computational capacity are needed for the implementation of predictive data-driven control methods such as Model Predictive Control (MPC) or integrating machine learning.

This thesis involves the design and testing of an interface board to connect the Wolfspeed CRD25DA12N-FMC 25 kW three-phase inverter with the high-performance real-time control platform UltraZohm.

The design process involves the schematic circuit analysis of the Wolfspeed inverter, analog and digital signal circuit path design, power supply design, and PCB layout optimization. An RJ45 Ethernet connector is used to transfer analog signals, and digital optical transmitters and receivers are used for digital signal transmission. Through a thorough and systematic testing procedure, the design and layout of the board are validated and integrated with the Wolfspeed inverter, producing sinusoidal three-phase output currents until a DC-link input power of approximately 10 kW.

The interface board allows users of UltraZohm to interface the Wolfspeed CRD25DA12N-FMC 25 kW three-phase inverter directly to the system for testing. The open-source hardware design files are hosted on Bitbucket [1], with supporting material available on the UltraZohm project documentation page at docs.ultrazohm.com.

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CHAPTER 1

Introduction and Background

1.1 Motivation

With the rapid electrification of industries and the drive towards renewable energy integration, power converters have increasingly begun to play an important role, specifically in sectors such as transportation, energy, and industrial automation. Recent trends in the power electronics industry indicate a clear shift toward higher energy efficiency, more compact designs, and the implementation of advanced control algorithms [2].

A fundamental component in power electronics is the inverter, which converts direct current (DC) input into alternating current (AC) output, enabling the operation of AC loads and devices. Specifically, a three-phase inverter delivers power across three phases using six switching devices arranged in a three-leg bridge topology. To meet the growing demand for higher switching frequencies, improved efficiency, and increased power density, the industry has turned to advanced semiconductor materials - notably silicon carbide (SiC).

In response to these trends, Wolfspeed has developed a 25 kW three-phase inverter targeting the automotive and renewable energy industries. To keep pace with the growing need for advanced control strategies, Wolfspeed partnered with the Chair of High-Power Converter Systems at the Technical University of Munich to design an interface board that enables the inverter to be connected to the external real time rapid prototyping platform UltraZohm [3], which is a modular system with significantly enhanced computational flexibility for developers.

This collaboration strengthens Wolfspeed's development capabilities and benefits the UltraZohm user community by providing access to a commercially available inverter platform that can be readily integrated into testing and development workflows.

1.2 Project Objective and Scope

This section aims to provide a brief overview of the objectives and scope of the project.

1.2.1 Project Objective

The main goal of this thesis is to design and test a Printed Circuit Board (PCB) interface that can connect the Wolfspeed CRD25DA12N-FMC 25 kW three-phase inverter [4] with UltraZohm. The inverter is designed to be compatible with a Texas Instruments TMDSCNCD280039C control card [5], and the interface board will be integrated in its place. Digital signals will be transmitted through digital optical cables and analog signals through Ethernet between the inverter and UltraZohm platforms. The PCB design is done using Altium Designer, and the boards are ordered at JLCPCB.

The important aspects of the interface design are listed below in no particular order:

- Schematic-level analysis of Wolfspeed inverter
- Analog sensing signal circuit path design
- Digital signal circuit path design
- Power supply design
- PCB layout optimization

The testing of the board is conducted in the following order:

1. Board bring-up
2. Validation of analog sensing and digital transmitter/receiver signal path designs
3. Digital gate signal transmission test from UltraZohm to the Wolfspeed inverter
4. Testing of DC-link voltage and output phase current sensing
5. Running inverter with RL-load and power

1.2.2 Scope

This project is exclusively covering the design and testing of an interface board that can be used in place of the TI TMDSCNCD280039C to connect the Wolfspeed inverter to UltraZohm. Systematic procedures are followed to validate the board design and verify its performance once integrated into the inverter. Testing of the inverter and UltraZohm systems only occurs to test the interface board itself; specific control methods are not evaluated in the scope of this thesis.

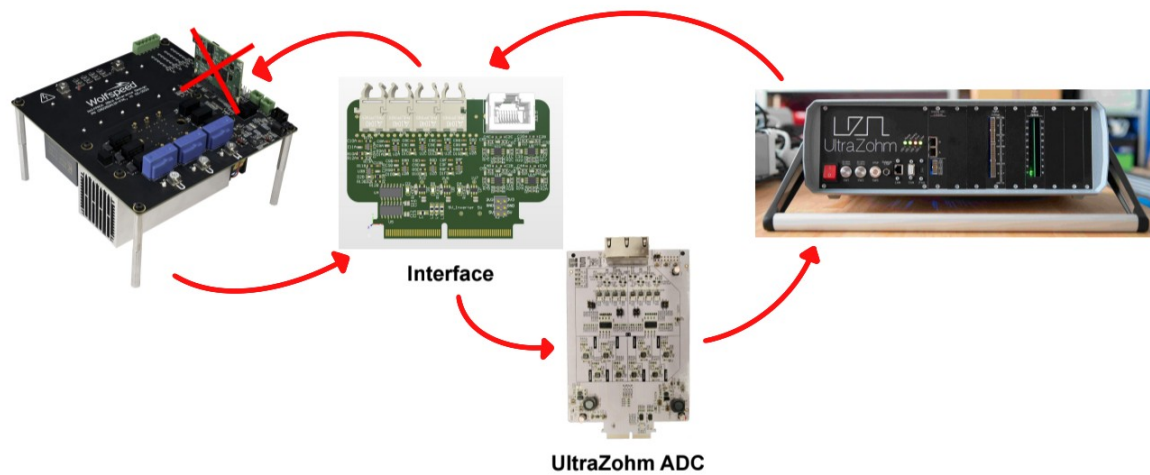


Figure 1.1: Overview of the goal of this thesis

CHAPTER 2

State of the Art

This chapter presents the theoretical foundations and technical background of all the key systems utilized in this project. It begins with an overview of power transistors, focusing on the metal-oxide-semiconductor field-effect transistor (MOSFET), insulated-gate bipolar transistor (IGBT), and silicon carbide MOSFET (SiC MOSFET). Secondly, there will be an introduction to inverters, looking at different topologies and pulse width modulation (PWM). Lastly, the specific hardware platforms used in this project are introduced: the Wolfspeed 25kW 3-phase inverter and the UltraZohm real-time control platform.

2.1 Introduction to Power Transistors

Power transistors are fundamental components in modern power electronic systems. They serve as the primary switching elements that enable the conversion of the DC input power to an AC output. Power transistors are designed for use under high currents and voltages while maintaining fast switching speeds and thermal stability. The type of transistor used in a power converter directly influences its efficiency, switching frequency, and thermal capabilities. The two most widely used types of power transistors are MOSFETs and IGBTs. More recently, wide-bandgap devices such as SiC MOSFETs have gained prominence due to their superior switching performance and high-voltage capabilities. This section provides only a brief overview of power transistors; for a more comprehensive treatment, the reader is referred to [6].

2.1.1 MOSFETs

A MOSFET is a type of transistor widely used in power modules of power converters for switching. It is a three-terminal device, consisting of a gate, source, and drain. The key operating principle of a MOSFET is that conduction between the source and drain terminals is controlled by the gate signal. When a voltage is applied to the gate, an electric field is generated across

an oxide layer that insulates the gate terminal from the channel substrate. This changes the conductivity of the channel between the source and drain terminals. The gate terminal itself draws very little current, and it is isolated from the channel by an oxide layer, thus acting like a capacitor. Therefore, to stop the conduction between the source and the drain, the gate charges must be discharged.

A MOSFET has 2 types of operating modes:

- **Enhancement-Mode MOSFETs:** the default state is not conducting. A gate voltage must be applied for a conductive channel to be formed between the source and drain terminals in order for the MOSFET to conduct.
- **Depletion-Mode MOSFETs:** the default state is conducting. A gate voltage is applied to cut off the conduction.

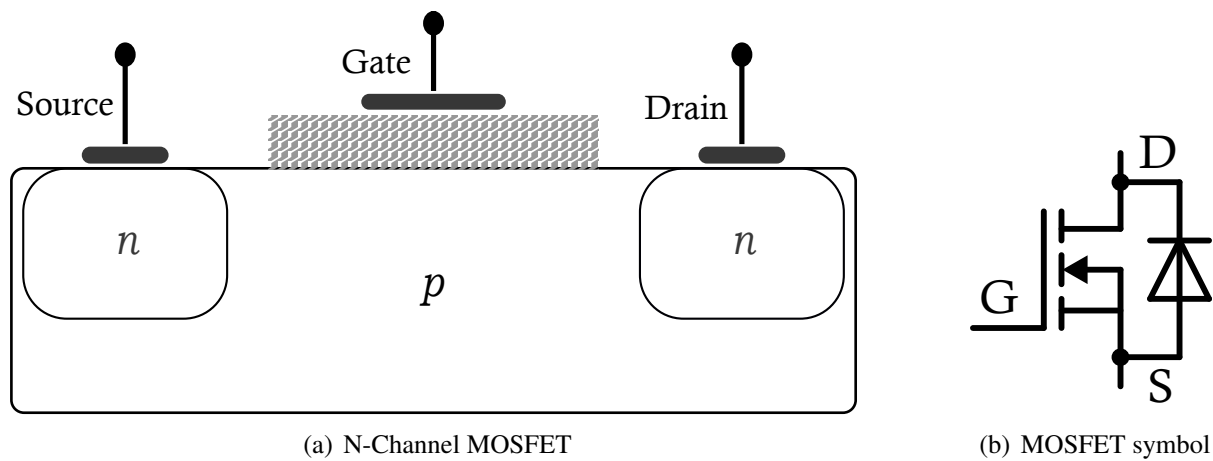


Figure 2.1: N-Channel MOSFET and the corresponding circuit symbol

Figure 2.1 shows the configuration of a typical MOSFET and its corresponding circuit symbol. When talking about the chemical composition of MOSFETs, it is important to understand n-doped and p-doped semiconductors. For silicon-based MOSFETs, doping with an element that has one more valence electron than silicon, such as phosphorus, produces n-type (negative-type) silicon with free electrons as charge carriers. Doping with an element that has one fewer valence electron, such as boron, results in p-type silicon, where holes are the majority carriers.

MOSFETs can be classified according to the type of semiconductor doping used in their channel region: n-channel and p-channel. In an n-channel MOSFET, the base layer (or substrate) is typically p-type silicon, whereas the regions below the source and drain are heavily n-doped. In a p-channel MOSFET, the base layer (or substrate) is typically n-type silicon, and the regions below the source and drain are heavily p-doped. The majority of power MOSFETs are of the n-channel type. Due to its physical structure, a MOSFET inherently includes a body diode between the drain and source terminals. This diode is formed by the pn-junction between the body (p-type) and the drain (n-type), and it allows current to flow from drain to source when the MOSFET is turned off.

For enhancement-mode n-channel MOSFETs, if there is no gate voltage, the oppositely doped regions form a pn-junction, thus a depletion layer where they meet, preventing any conduction. When there is a positive voltage at the gate, the gate region acts like a capacitor,

attracting electrons to the area, building a channel of negatively charged electrons connecting the source to the drain. Depletion-mode MOSFETs are not further discussed as they are rarely used in power electronics. [7] [6]

2.1.2 IGBTs

Like MOSFETs, the IGBT is a three-terminal device, consisting of emitter, collector, and gate terminals. In the context of this thesis, we will only discuss n-channel IGBTs as p-channel IGBTs are not commercially used in power electronics due to their performance drawbacks [7]. The basic structure of an IGBT and its corresponding symbol is shown in Figure 2.2.

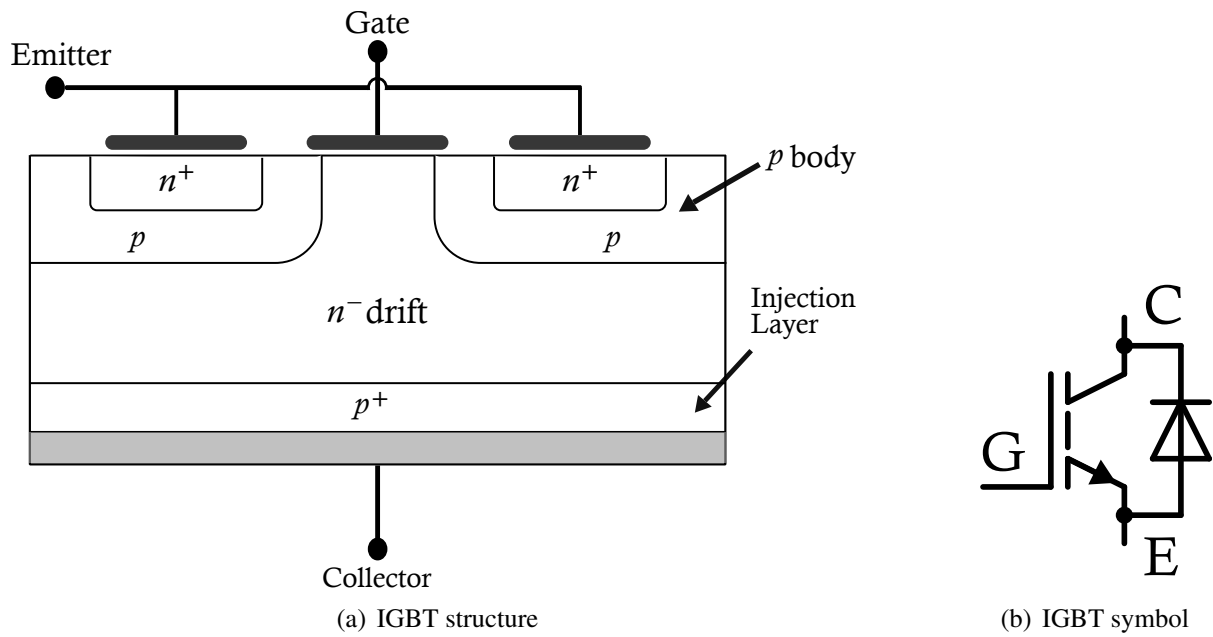


Figure 2.2: IGBT structure and corresponding circuit symbol, based on [8]

The total structure of an IGBT is developed on an n-doped substrate with two p-doped regions formed at the top. Inside the p-doped regions, right underneath the emitter terminals, are also two n+ (highly n-doped) wells. The n- (lightly n-doped) region is called the drift layer, below which is a p+ (highly p-doped) injection layer, connected to the collector terminal. When a positive voltage is applied to the gate, just like a MOSFET, an n-channel is formed between the two emitter terminals. When the n-channel is formed, electrons can flow from the emitter into the drift layer. To maintain charge balance, holes from the injection layer are injected into the n- drift layer, and a conduction channel between the emitter and collector terminals is formed.

2.1.3 SiC MOSFETs

Traditional Silicone (Si)-based MOSFETs and IGBTs are limited by the physical properties of silicon, especially when operating at high voltages and temperatures. Silicon carbide (SiC), a wide bandgap (WBG) semiconductor material, has a breakdown field strength approximately

ten times higher than that of silicon. As a result, SiC transistors show superior performance at high voltage levels, with lower conduction losses and improved thermal stability [9].

Just like traditional MOSFETs, both n and p-channel configurations exist, and we can further classify them into enhanced-mode and depletion-mode depending on the default conduction mode. Unlike a traditional MOSFET, typical power MOSFETs, including ones based on SiC substrates, tend to have differently doped layers stacked vertically, similar to the structure of an IGBT.

In Figure 2.3, the structure of an n-channel enhanced SiC power MOSFET is shown. In this vertical structure, the drain is moved to the bottom so the current conducts vertically through the structure. When the gate terminal sees a positive voltage, an electric field gradient is formed, attracting carrier electrons to the region, creating a channel between the N+ regions. This allows the carrier electrons to enter the drift region so that conduction between the source and drain terminals can occur.

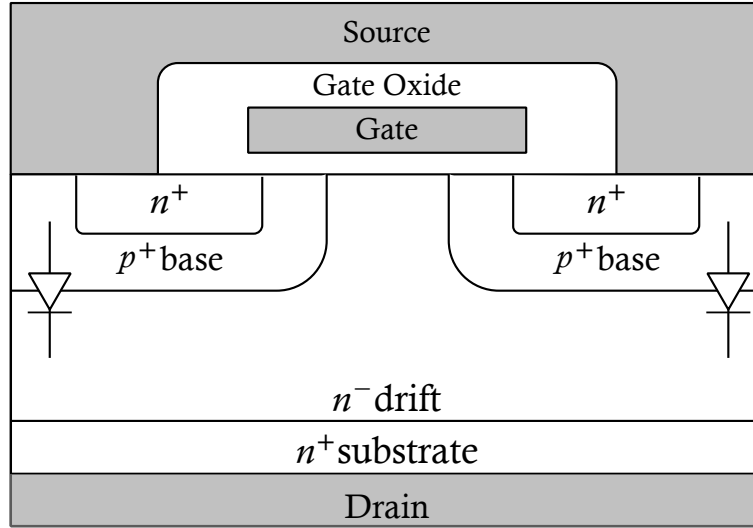


Figure 2.3: SiC MOSFET structure, taken and drawn from figure 1 of [10]

Compared to silicon, silicon carbide possesses several advantageous properties that make it better suited for high-voltage power electronics applications. First of all, power transistors must be able to withstand large drain-source voltages without breaking down and entering uncontrolled conduction. One way to increase the breakdown voltage is to increase the distance between the source and drain terminals by extending the drift layer. However, this increases the on-state source to drain resistance, leading to higher conduction losses. SiC has a breakdown field strength that is approximately ten times larger than silicon [9]. This allows SiC MOSFETs to be designed with shorter distances between the source and drain terminals for the same breakdown voltage, resulting in smaller device dimensions and lower on-state resistance. For example, a 900V SiC MOSFET with the same on-state resistance can be 35 times smaller than a standard Si MOSFET [11]. Furthermore, SiC's wide bandgap (3.25eV) results in only small amounts of electrons escaping from the valence band to the conduction band at high temperatures, resulting in negligible leakage currents up to 500°C [12]. This, along with SiC having higher thermal conductivity than Si, means that SiC MOSFETs have a larger operating temperature range than their Si counterparts. Lastly, SiC has lower power loss and is able to handle

higher switching frequencies when compared to Si-MOSFETs and IGBTs [13]. On the other side, SiC devices currently cost more to produce, and due to the high switching frequencies problems related to electromagnetic interference (EMI) often arise [14].

2.2 Introduction to Inverters

Inverters are essential components in power electronics, responsible for converting a DC voltage or current source into an AC output. This conversion is crucial in any application where AC power is required but only a DC source is available, such as a battery Electric Vehicle (EV) powertrain or photovoltaic systems.

The basic principle of an inverter involves switching power transistor devices such as MOSFETs or IGBTs in a specific manner to produce the required AC output waveform. By switching the transistors on and off in a certain pattern, a DC link input can be converted into AC output power with variable amplitude and frequency. Pulse Width Modulation (PWM) is a very commonly used switching method and will be explained in the coming sections. Inverters can be classified based on their transistor topology – in the context of this thesis, single and three-phase half-bridge topologies are discussed.

2.2.1 Half-bridge Configuration

The half-bridge inverter is a fundamental building block of power electronics and consists of two active switching devices (MOSFETs or IGBTs) connected in series across a DC supply. Figure 2.4 shows a single-phase half-bridge configuration. Two free-wheeling diodes are connected in parallel to the switches, and the load is connected in series to the midpoint between the two switches. For SiC devices, the body diodes act as internal free-wheeling diodes. The two capacitors C_1 and C_2 split the input DC link into equal halves charged $\frac{V_{DC}}{2}$. Through the two capacitors, a fictitious ground point is created between them.

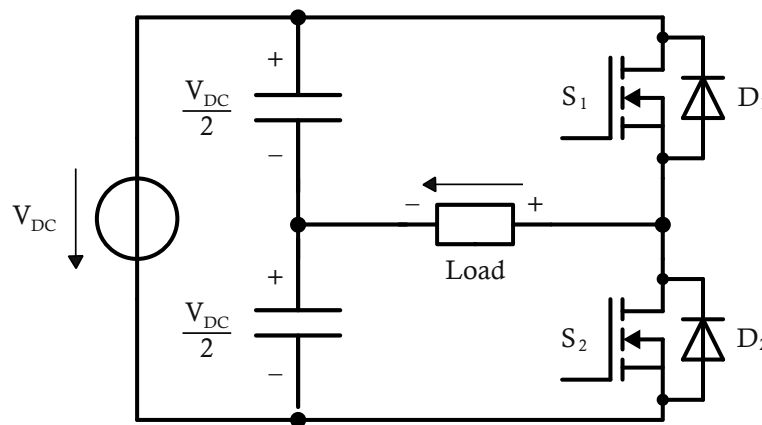


Figure 2.4: Single-phase half-bridge inverter

The inverter operates by using a microcontroller or Field Programmable Gate Array (FPGA)-based controllers to alternately switch S_1 and S_2 . When switch S_1 is conducting, the load sees a positive voltage, and when switch S_2 is conducting, the load sees a negative voltage. For

half-bridge topologies, the high-side switch (S1) and low-side switch (S2) are always driven complementarily, with a small dead-time in between where both switches are not conducting, to avoid shoot-through.

A device with the half-bridge topology can operate in 5 distinct states:

1. State 1: S1 is conducting and S2 is not conducting. The voltage on the load is equal to $+\frac{V_{in}}{2}$ and $i_{Load} > 0$
2. State 2: S2 is conducting and S1 is not conducting. The voltage on the load is equal to $-\frac{V_{in}}{2}$ and $i_{Load} < 0$
3. State 3: Only D1 is conducting. The voltage on the load is equal to $+\frac{V_{in}}{2}$ and $i_{Load} < 0$
4. State 4: Only D2 is conducting. The voltage on the load is equal to $-\frac{V_{in}}{2}$ and $i_{Load} > 0$
5. State 5: Both S1 and S2 are not conducting. The voltage and current on the load is zero

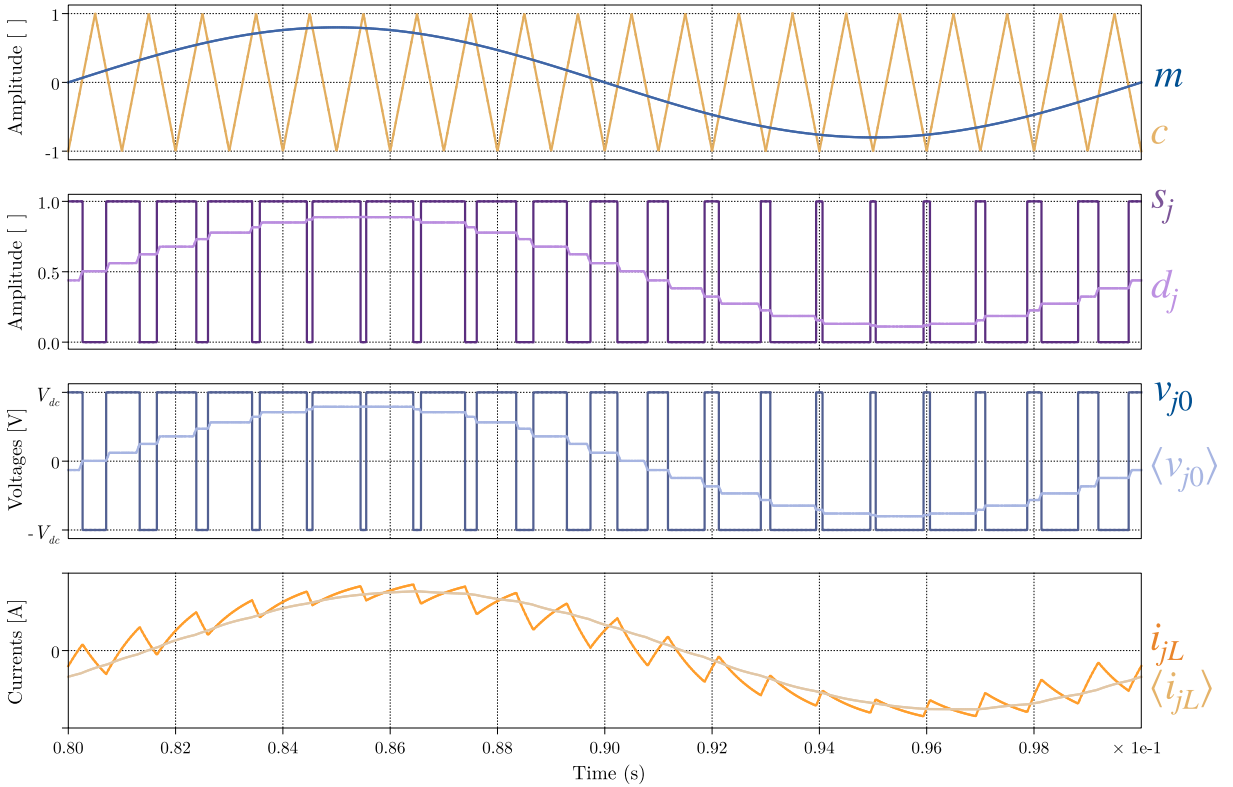


Figure 2.5: Carrier and reference signal as well as the resulting PWM signal for a half-bridge inverter with the respective load voltage and current curves [15]

2.2.2 Three-phase Inverter

A three-phase inverter is constructed by connecting three half-bridge legs in parallel. This is illustrated in Figure 2.6. In this configuration, a total of six transistors and six free-wheeling

diodes are required. The output three-phase voltages and currents must have the same frequencies and magnitude and have a phase difference of 120° . These parameters are controlled by the specific PWM signals that each leg of the inverter receives.

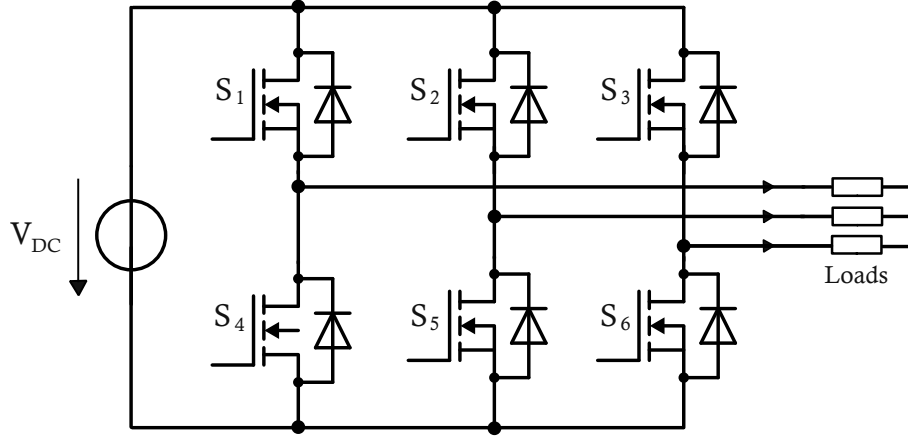


Figure 2.6: Three-phase half-bridge inverter

2.2.3 Pulse Width Modulation

PWM is the primary switching method for regulating the average power delivered by modern power converters. A high frequency carrier waveform – typically a triangular or saw-tooth signal with constant period $T_s = \frac{1}{f_s}$ is continuously compared with a reference waveform that represents the desired output (here a sinusoid for each phase). Whenever the reference exceeds the carrier, the comparator outputs a logic-high and otherwise a logic-low. The resulting rectangular pulses drive the gate drivers of the power transistors. Figure 2.5 shows in the first plot the carrier and reference waveforms which produce the PWM signal in the second subplot.

The high-side switches are turned on when the rectangular pulses are high, and the low-side switches are turned on when the rectangular pulses are low.

The key control variable is the duty cycle.

$$D = \frac{t_{\text{on}}}{T_s}$$

This is the fraction of each switching period where the pulse is high. The duty cycle ranges from 0 (always off) to 1 (always on) $D \in [0, 1] \subseteq \mathbb{R}$. For an ideal single-phase half-bridge inverter, the average value of the output voltage is given by

$$\langle V_{\text{load}} \rangle = D \cdot V_{\text{DC}}$$

Therefore, increasing the duty cycle increases the average output voltage and, therefore, the delivered power proportionally.

2.3 Wolfspeed Inverter

For this thesis, the Wolfspeed CRD25DA12N-FMC 25 kW three-phase inverter is interfaced to the UltraZohm control platform. It is built around the CCB021M12FM3T Wolfpack module [5] (1200 V, 21 mOhm six-pack SiC MOSFET module), which contains the three half-bridges for a three-phase inverter topology. The inverter is designed for lab evaluation and not industrial use or production development, but offers flexibility for use in motor drives, power supplies, renewable energy systems, and EV charging applications [4].

2.3.1 Technical Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
P_{OUT}	Output Power	—	—	25	kW
V_{DC}	DC Bus Voltage	—	800	1000	V
V_{AUX}	Low-Power Auxiliary Voltage	10.8	12	13.2	V
I_{AUX}	Low-Power Auxiliary Current	—	—	5	A
I_{OUT}	Output Phase Current	—	—	30	A _{RMS}
f_s	Switching Frequency ¹	—	20	100	kHz
$R_{th,ja}$	Thermal Resistance, Junction-to-Ambient ¹	—	1.571	—	°C/W

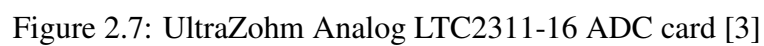
Table 2.1: CRD25DA12N-FMC Inverter Ratings [4]

Table 2.1 contains all the important parameters for inverter operation. Integrated components include gate drivers with separate turn-on/off resistors, hall-effect current sensors, voltage sensing (three-phases and the DC link), resolver feedback for position sensing, Negative Temperature Coefficient (NTC) temperature monitoring, and isolated Controller Area Network (CAN) communication [4].

2.4 UltraZohm

The UltraZohm is a real-time control platform with high-performance capabilities based on a system-on-chip FPGA. It is a modular system that is designed to be used to test more complex control algorithms, such as Model Predictive Control (MPC) or artificial intelligence-based methods. It is an ongoing project funded by the Federal Ministry of Education and Research within the research project KI-Power. Integrating the UltraZohm with the Wolfpack inverter provides engineers with a versatile setup for implementing and evaluating complex control strategies in real-world applications.

On UltraZohm, the Analog LTC2311-16 Analog Digital Converter (ADC) card [3] is used to convert and interpret the DC-link voltage and output phase current sensing signals. It contains RJ45 Ethernet connectors and four ADCs that support fully differential measurements. Furthermore, the Digital Optical 14Tx4Rx card [3] is used to transmit and receive digital optical signals from the inverter. It contains up to 14 transmitters and four receivers. The interface board uses the same transmitter and receiver logic as defined on this board. Figures 2.7 and 2.8 show the analog ADC and digital optical cards used in UltraZohm.



CHAPTER 3

Design and Development

This chapter presents the design and development process of the interface board, outlining key considerations related to analog and digital signal components, power supply constraints, and component layout. First, all transmitted signals are summarized using a system-level block diagram. This is followed by a discussion of the analog schematic design, which includes current and DC voltage conditioning circuits with differential signalling, implemented using a fully differential operational amplifier. LTSpice simulations are used to verify circuit behavior. Furthermore, the schematics of the digital components and the power supply design are covered. Finally, practical aspects such as component placement and additional mechanical features integrated into the design are discussed.

3.1 Block Diagram of Interface Board

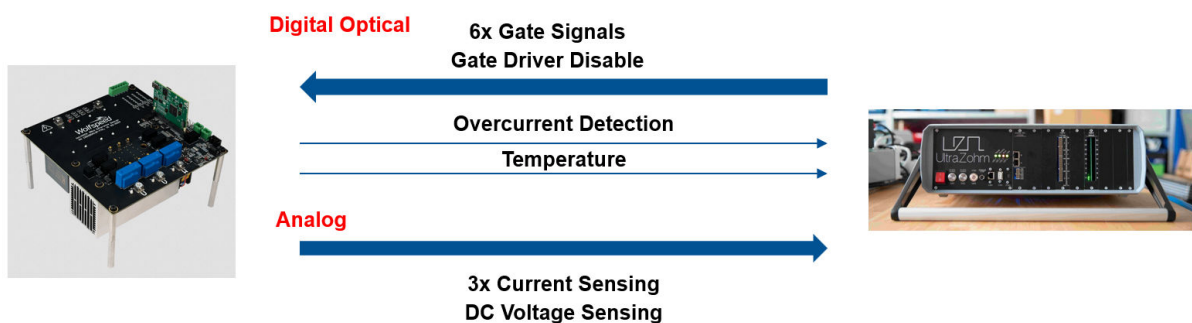


Figure 3.1: Digital optical and analog signal interface between the Wolfspeed inverter (left) and UltraZohm real-time controller (right)

Figure 3.1 shows an overview of the signal interface between the Wolfspeed inverter and

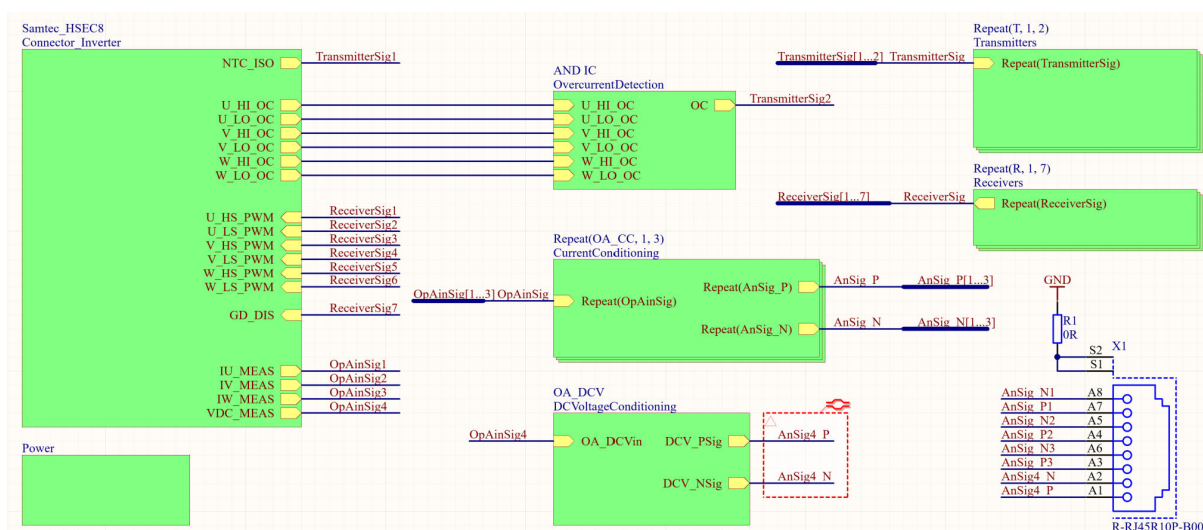


Figure 3.3: Top sheet of interface board

3.2 Circuit Design

The schematic design of the interface board is based on both analog and digital signal requirements, which were derived through an analysis of the incoming and outgoing signals between the Wolfspeed inverter and the interface. The design process begins with an investigation of the analog signal paths to define proper biasing, voltage levels, and signal conditioning. Following this, the digital signal schematics were developed. Finally, the power supply section was designed based on the voltage and current demands of all the integrated components. Figure 3.3 shows the top sheet of the schematics.

3.2.1 Analog Current Sensing

Three output current sensing signals are transmitted from the inverter to UltraZohm.

3.2.1.1 Inverter Circuitry

Figure 3.4 shows the path of the output current sensing signal path in the Wolfspeed inverter for one phase.

To begin, the LAH 50-P Hall effect current transducer from LEM, which is connected in series to an output phase, outputs a current. The current transducer has a turns ratio of 1 : 2000 with a primary current measuring range of 0 to ± 110 A [17]. It has a primary and secondary nominal Root Mean Square (RMS) current of 50 A and 25 mA respectively. Therefore, the current transducer translates the current down by a factor of 2000.

Afterwards, there is a current-to-voltage conversion with the parallel resistor R90 through the equation 3.1.

$$I_U R_{90} = 0.025 \text{ A} \cdot 100 \Omega = 2.5 \text{ V} \quad (3.1)$$

and then a voltage divider formed by R93 and R164 scales the voltage down to around 2/3 of its original value through the equation 3.2.

$$2.5 \text{ V} \cdot \frac{R_{164}}{R_{93} + R_{164}} = 2.5 \text{ V} \cdot \frac{4.02 \text{ k}\Omega}{4.02 \text{ k}\Omega + 2 \text{ k}\Omega} = 1.669 \text{ V} \quad (3.2)$$

The resulting IU_FILT signal has a bias voltage of 1.68 V applied through the +3.3 V source. This bias voltage is derived from the 3.3 V source via a voltage divider composed of R154 as the upper resistor and R90, R93, and R164 together forming the lower resistor as shown in equation 3.3.

$$\begin{aligned} & \left(\frac{1}{\frac{1}{R_{93}+R_{90}} + \frac{1}{R_{164}}} \right) \bigg/ \left(R_{154} + \frac{1}{\frac{1}{R_{93}+R_{90}} + \frac{1}{R_{164}}} \right) \cdot 3.3 \text{ V} \\ & \approx \frac{1.379}{1.379 + 1.33} \cdot 3.3 \text{ V} \approx 1.68 \text{ V} \end{aligned} \quad (3.3)$$

Then, the signal goes through an op-amp configured as a voltage follower, which acts as a buffer. The resulting single-ended IU_MEAS signal then enters the interface board.

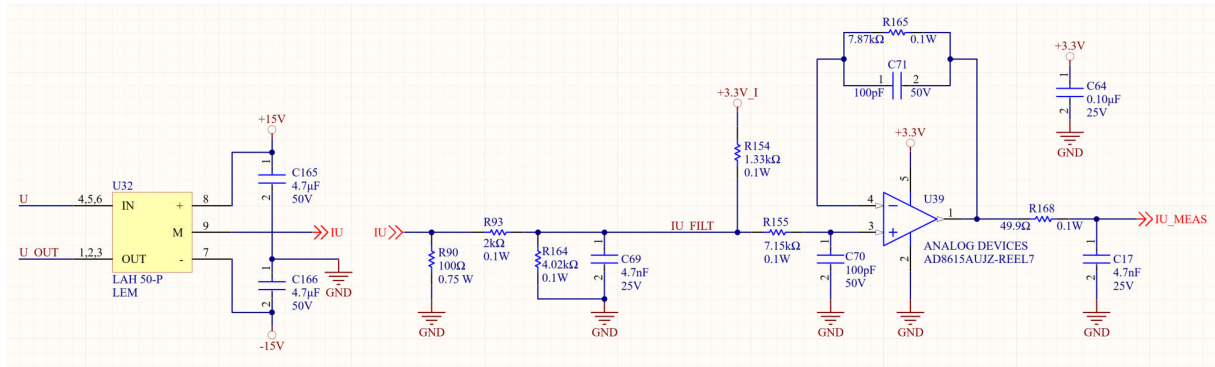


Figure 3.4: Current sensing signal pathway in inverter [16]

3.2.1.2 Interface Board Circuitry

The single-ended signal is converted into a differential signal to increase signal integrity by reducing susceptibility to noise interference, which allows for more reliable transmission over longer distances. To convert the single-ended signal into a differential signal, the TI THS4561 low-power, 60 MHz fully differential amplifier is used. This specific op-amp is also used in UltraZohm ADC cards. In addition to generating a differential output, the op-amp also removes the 1.68 V DC bias voltage and applies a gain of 1.515 V to match the input range of the UltraZohm's ADC, which operates at 5 V, while the inverter signal has a nominal level of 3.3 V.

Figure 3.5 shows the fully differential op-amp schematic design. As a 1.68 V voltage reference is not commonly available, a 1.7 V reference is used instead, connected to the inverting input terminal of the op-amp.

The gain of a fully differential op-amp can be calculated using the equation 3.4.

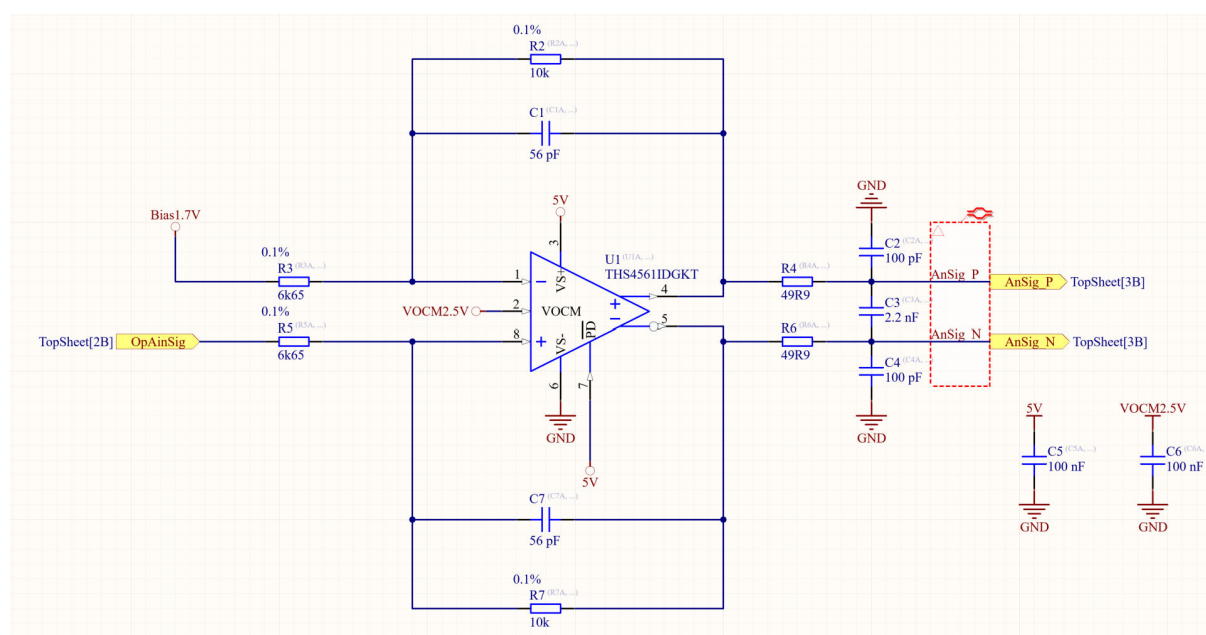


Figure 3.5: Fully differential op-amp for current sensing

$$\text{Gain} = \frac{R_7}{R_5} \quad (3.4)$$

R_2 is the feedback resistor and R_1 is the gain resistor [18]. For the current sensing signal op-amp, a 10kOhm feedback resistor and 6.65 kOhm gain resistor are used so that the output differential signal has a gain of 1.504.

A quick example calculation is done for the case where 1 A is flowing through one output phase. To begin, the current is translated down by a factor of 2000, converted into voltage by multiplying with the 100 Ohm resistor R90, and translated by a factor of 2/3 by the voltage divider. Afterwards, a bias voltage of 1.68 V is added, and the voltage follower has a gain of 1. Lastly, now coming into the interface board, the bias is corrected back down by 1.7 V, and the fully differential op-amp has a gain of 1.504. Therefore, when the primary side current 1 A is conducted in one output phase, the sensed value is expected to be around 0.0201. The current is then sensed in the UltraZohm LTC2311-16 ADC card and translated to the actual current value in the system.

$$\text{Gain}_{\text{Output Phase Current Sense}} = \left(\left(1 \text{ A} \cdot \frac{1}{2000} \cdot 100 \text{ Ohm} \cdot \frac{201}{301} \right) + 1.68 \text{ V} - 1.7 \text{ V} \right) \cdot 1.504 \approx 0.0201 \quad (3.5)$$

3.2.1.3 LTspice Simulation

To validate the fully differential op-amp feedback design and make sure the inverter circuitry is understood correctly, the total circuit is simulated using LTSpice.

Figure 3.6 shows the circuit schematics under a transient simulation with an AC source that inputs a sine wave with an amplitude of 0.01, frequency of 50 Hz, and no DC offset. Several

voltage measurements are taken and displayed throughout the circuit. The simulation confirms the theoretical calculation of the 1.68 V bias due to the +3.3 V source before the AD8615 op-amp follower in the inverter.

Figure 3.7 illustrates the differential output signal from the THS4561 op-amp, centered around a common-mode voltage of 2.5 V. By applying a 1.7 V reference to the inverting input, the op-amp effectively removes the input bias and generates a differential output compatible with the 5 V input range of the UltraZohm ADCs.

Looking at the Bode plot of the differential output signal in Figure 3.8, it is evident that the circuit functions as a low-pass filter, effectively attenuating high-frequency components. This enhances signal integrity by suppressing high-frequency noise, which is beneficial for accurate current sensing in inverting control applications. In the Bode plot, the magnitude curve is plotted in black and the phase curve is plotted in red. It can be seen that the magnitude curve has a gain of around -27 dB below the cutoff frequency. This shows the gain of the circuit without the current transducer, and it should be noted that the output is not normalized over the input.

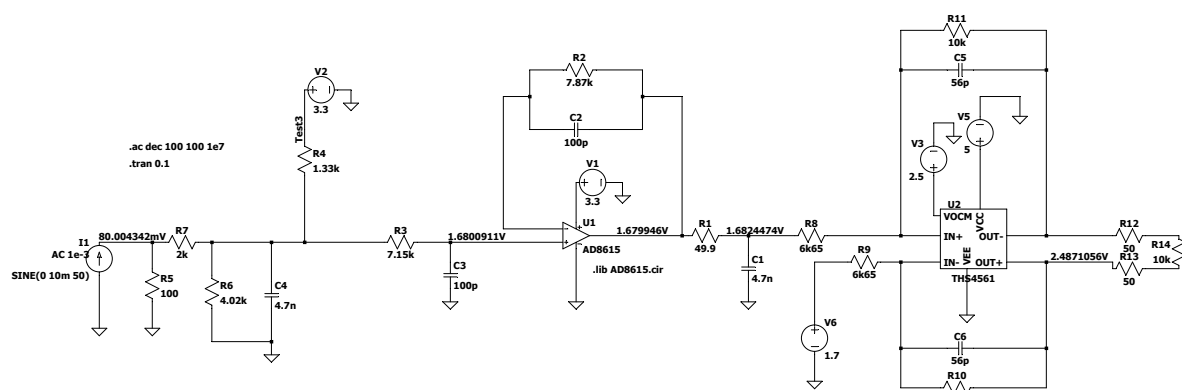


Figure 3.6: LTspice current sensing circuit simulation

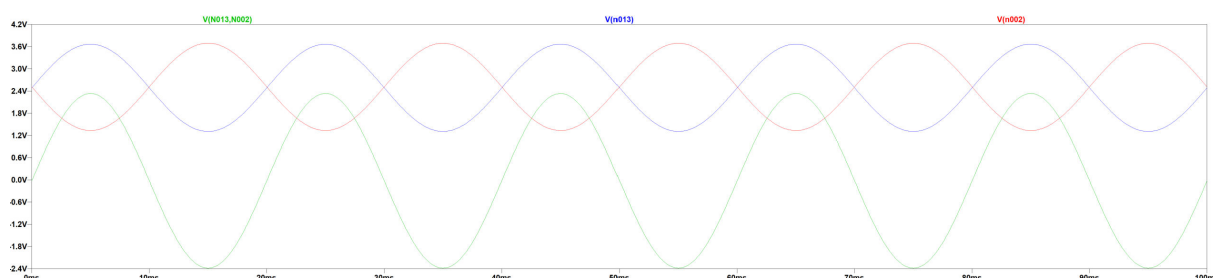


Figure 3.7: Differential output phase current sensing - the blue and red curves show the positive and negative output terminal measurements of the fully differential amplifier with a common mode around 2.5 V and the green curve is the resulting differential signal

Overall, the LTspice simulation confirmed the correct functioning of the current sensing circuit. It demonstrates that the fully differential op-amp THS4561 implemented on the interface

board successfully removes the 1.68 V bias voltage and generates a properly amplified differential signal compatible with the input range of the UltraZohm ADCs.

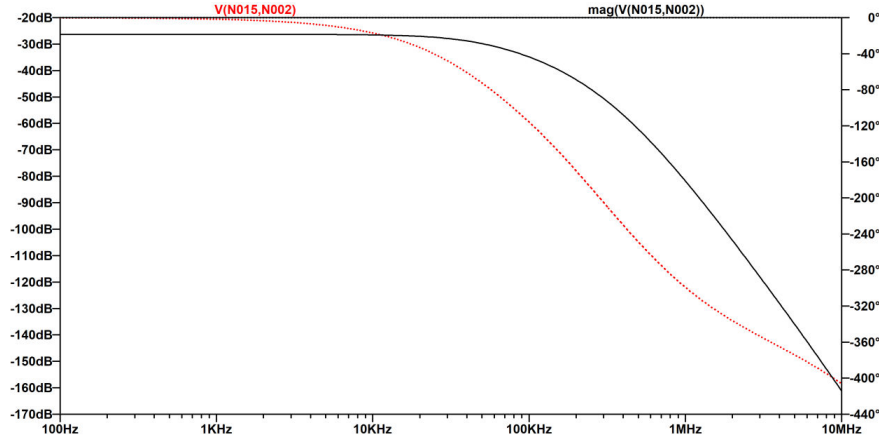


Figure 3.8: Bode plot of THS4561 differential output

3.2.2 DC-Link Voltage Sensing Analog Circuit Design

There is one analog DC link input voltage sensing signal that is transmitted from the inverter to UltraZohm.

3.2.2.1 Inverter Circuitry

Figure 3.10 shows the path of the voltage sensing signal in the Wolfsped inverter for the input DC-link. There are six 249 kOhm resistors in series with both the positive and negative DC-link inputs, creating a high impedance path for the DC-link voltage sensing path.

For the positive leg of the DC-link, there is an additional 3.74 kOhm resistor (R38) which forms a voltage divider for the input of the Analog Devices AD8615 op-amp. This forms a classic difference amplifier configuration, where the gain of the op-amp is given by the feedback resistance divided by the gain resistance, as shown in Figure 3.9 and equation 3.6 [7].

$$\text{Gain} = \frac{R_2}{R_1} \quad (3.6)$$

Therefore, the gain of this difference amplifier in the Wolfsped inverter (Figure 3.10) is given by equation 3.7

$$\text{Gain}_{\text{DC Voltage Conditioning Inverter}} = \frac{3.74 \text{ k}\Omega}{6 \cdot 249 \text{ k}\Omega} = 2.503 \cdot 10^{-3} \quad (3.7)$$

The input bias current of the op-amp is specified as 1 pA [19] and therefore the 4.99 kOhm resistors (R153 and R37) at the input terminals of the op-amp can be neglected as the input currents are negligible. They are likely remnants from an older design using legacy op-amps.

The resulting output signal from this op-amp then enters the interface board.

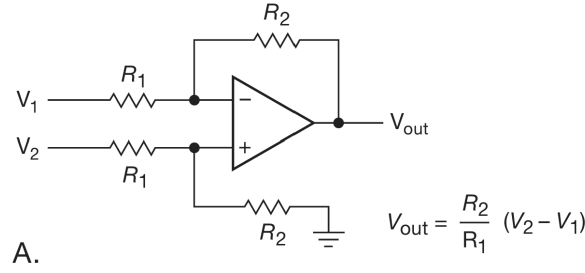


Figure 3.9: Difference amplifier gain calculation [7]

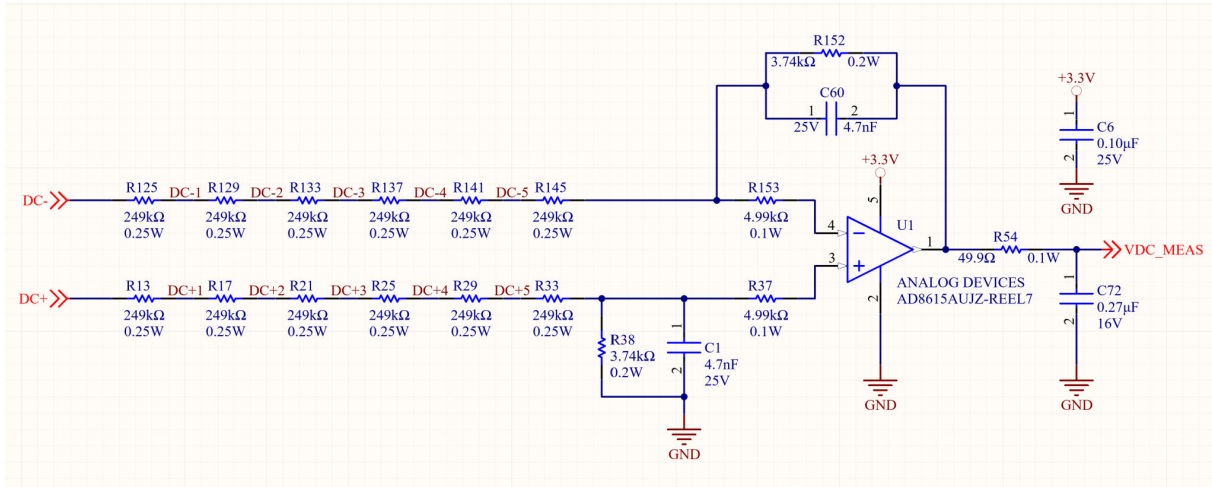


Figure 3.10: DC-link voltage sensing signal pathway in inverter [16]

3.2.2.2 Interface Board Circuitry

Like the output phase current sensing signals, to convert the single-ended DC-link voltage sensing signal into a differential signal, the THS4561 fully differential amplifier is used.

Unlike the output phase current sensing signals, the DC-link voltage sensing signal does not have a bias, as the DC-link voltage is only positive, not bipolar, as the currents are. Therefore, the inverting input of the fully differential op-amp can just be connected to ground (GND).

Figure 3.11 shows the schematic design of the fully differential amplifier on the interface board.

The values of the feedback and gain resistors are the same as for the fully differential amplifier for current sensing, with a gain of 1.504, as identical ADCs are being used in UltraZohm.

To calculate the total gain that the DC-link voltage signal has, the gain of the first difference amplifier (equation 3.7) in the inverter and the gain of our fully differential amplifier can be multiplied together. This is shown in equation 3.8 and results in a voltage sensing signal with a total gain of $3.765 \cdot 10^{-3}$ being transmitted to UltraZohm.

$$\text{Gain}_{\text{DC-link sense}} = 2.503 \cdot 10^{-3} \cdot 1.504 = 3.765 \cdot 10^{-3} \quad (3.8)$$

An example calculation is done when the DC-link is connected to +800 V and GND on the positive and negative rails, respectively. The following calculation shows the value expected at

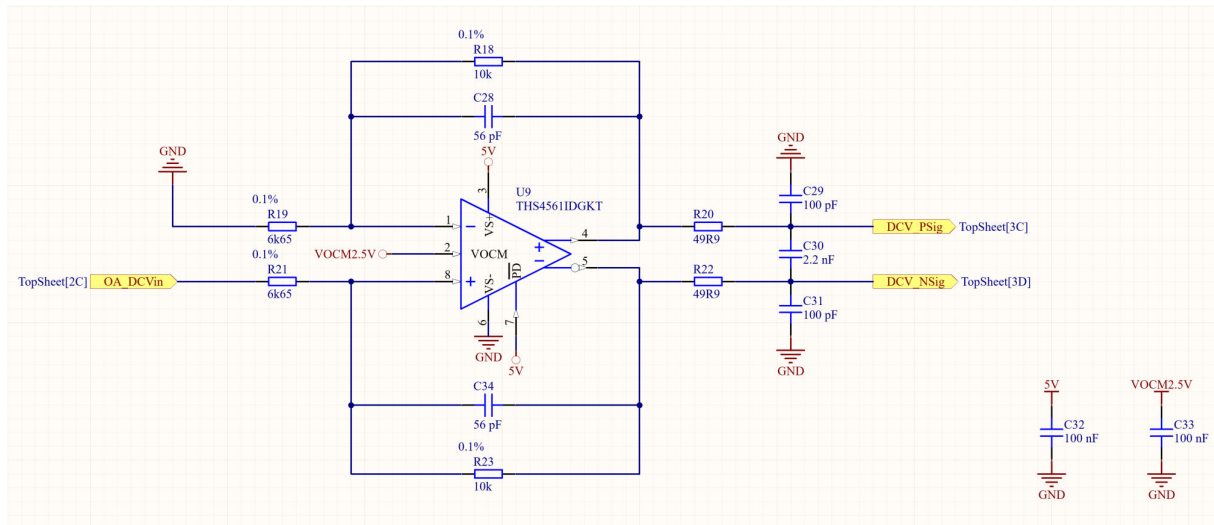


Figure 3.11: Fully differential op-amp on interface board for DC-link voltage sensing

the differential output of the op-amp on the interface board: $800 \text{ V} \times 3.765 \times 10^{-3} = 3.012 \text{ V}$

3.2.2.3 LTspice Simulation

In order to also validate the DC-link voltage sensing signal path, the total circuit was simulated using LTspice. Figure 3.12 shows the LTspice circuit schematics under a transient simulation with the positive rail of the DC-link connected to 800 VDC and the negative rail connected to GND. There are multiple voltage measurements taken and displayed throughout the circuit. The simulation confirms the gain calculations of both op-amps and outputs a differential signal with a common mode of 2.5 V. The output differential signal has a value of 3.007 V rounded to four significant figures, confirming the calculations.

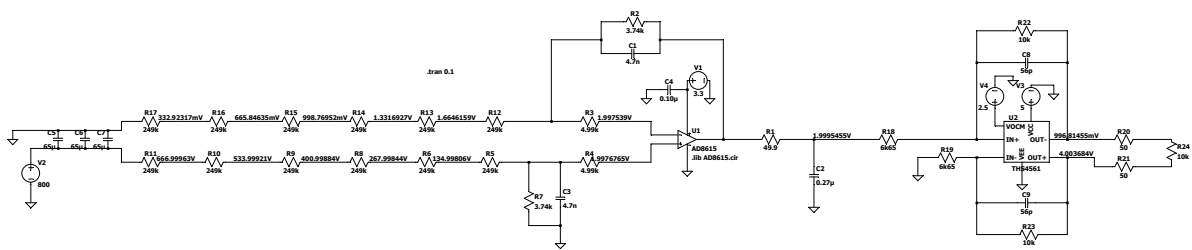


Figure 3.12: LTspice DC-link voltage sensing circuit simulation

3.2.3 Digital Signal Circuit Design

On the interface board, there are 13 digital signals consisting of six gate driver signals and one gate driver disable signal that needs to be received to the Wolfspeed inverter and six overcurrent detection signals and one NTC temperature detection signal that needs to be transmitted to UltraZohm. The six overcurrent detection signals are consolidated into one transmitted signal

using two 4-channel AND gates from TI (SN74HCS08DR). As transmitters the HFBR-1521Z and as receivers the HFBR-2521Z Broadcom versatile link fiber-optic connections are used to match the ones used in the digital optical cards of UltraZohm.

3.2.3.1 Transmitter and Receiver Schematics

The schematics for the transmitter and receivers are taken from the UltraZohm digital optical cards [3]. A dual inverter is integrated for both due to the design of the optical connections, which for the transmitter transmits light for digital low and doesn't transmit light for digital high, while for the receiver reads light input as digital low and no light input as digital high.

Figure 3.13 shows the schematic layout of the peripheral components to the transmitter and Table 3.1 shows the respective logic table.

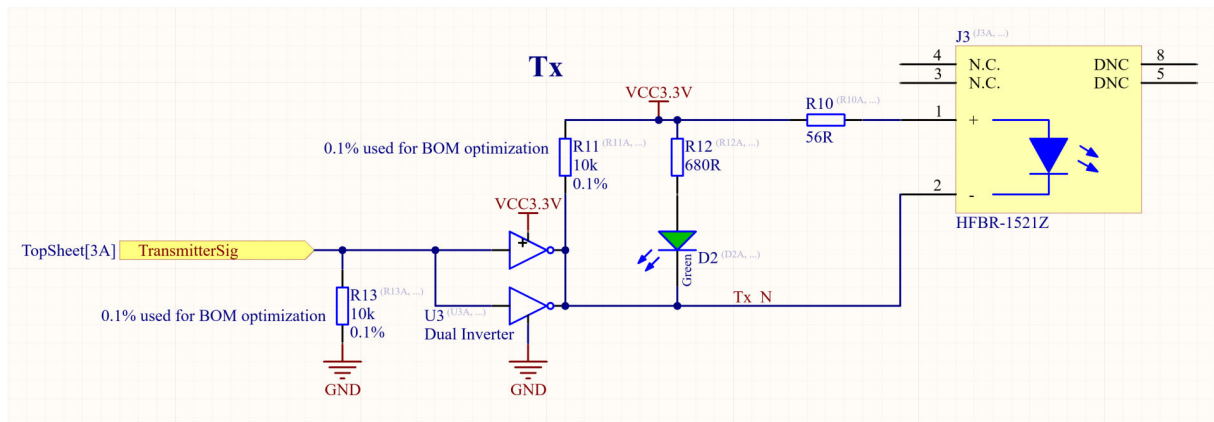


Figure 3.13: Interface board schematics of HFBR-1521Z transmitters

TransmitterSig	Node Tx_N	Transmitter LED J3	LED D2
LOW	HIGH	OFF	OFF
HIGH	LOW	ON	ON

Table 3.1: HFBR-1521Z transmitter logic table [3]

Figure 3.14 shows the schematic layout of the peripheral components to the receiver and Table 3.2 shows the respective logic table.

Receiver Diode J2	Node RxTx	ReceiverSig	LED D1
Light OFF	HIGH	LOW	OFF
Light ON	LOW	HIGH	ON

Table 3.2: HFBR-1521Z transmitter logic table [3]

3.2.3.2 Consolidation of Over- and Undercurrent Detection Signals

In order to reduce the number of digital optical transmitters required, thus reducing the size of the interface board, the six over- and undercurrent detection signals are consolidated into a

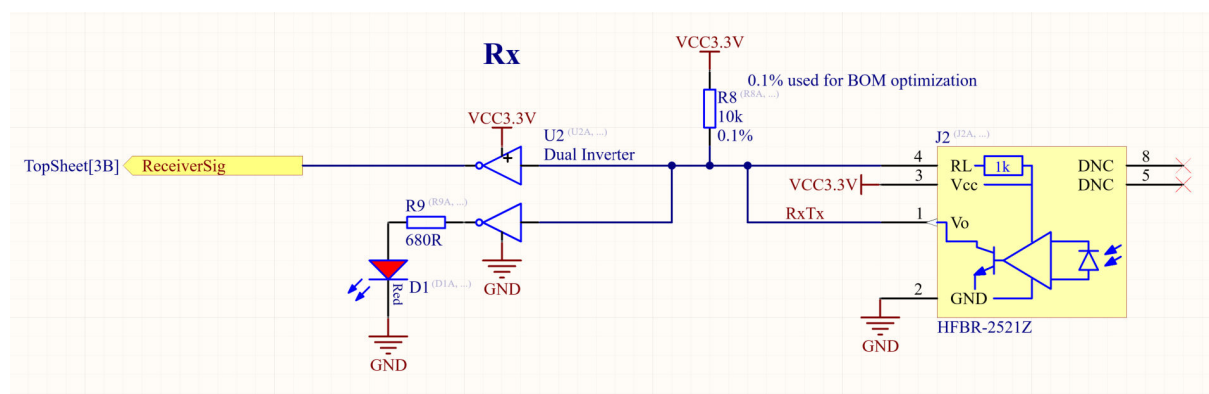


Figure 3.14: Interface board schematics of HFBR-2521Z receivers

single detection signal.

To understand how the over- and undercurrent detection signals function, it is necessary to look into the Wolfspeed inverter schematics once more. Figure 3.15 shows the TLV3502AID rail-to-rail, high-speed dual comparator used in the Wolfspeed inverter for the detection [16].

A comparator op-amp works by comparing the input voltages on the non-inverting V_+ and inverting V_- terminals. If $V_+ > V_-$, the comparator swings up and outputs the positive rail, and if $V_+ < V_-$, the comparator swings down and outputs the negative rail.

Therefore, according to the inverter schematic design, if the signal I_FILT remains within the accepted current range which is $0.3796\text{ V} < I_FILT < 2.920\text{ V}$, a logic HIGH signal will be output for both the high-side overcurrent detection and low-side undercurrent detection signals.

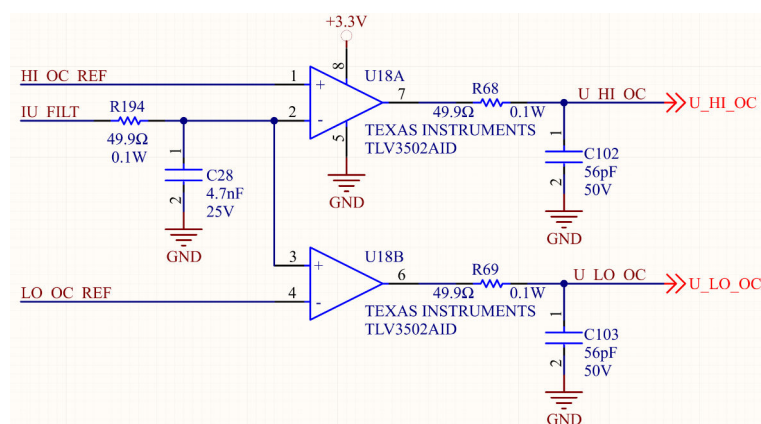


Figure 3.15: Over- and undercurrent detection circuit in Wolfspeed inverter [16]

To consolidate the six overcurrent detection signals, two 4-channel 2-input AND gates (TI SN74HCS08DR) are used, and the resulting overcurrent detection signal is transmitted to UltraZohm. The AND gates allow the detection of over- or undercurrent, as when one or more of the signals is a logic LOW, indicating the crossing of the boundaries, the AND gates will transmit a logic LOW to UltraZohm.

3.2.4 Power Section Design

The interface board requires four different power levels and receives 5 V with maximum 1 A as an input from the inverter. The 5 V input must be translated down to 3.3 V for the power supplies of the receivers, transmitters and AND gates, as well as to 2.5 V and 1.7 V for the fully differential amplifier common mode and bias voltage respectively.

An estimation of the total current demand of all voltage domains was performed to inform the selection of suitable components for the power section. A current budget of 1 A is available from the inverter input and must not be exceeded. To estimate the current demand of the interface board components, the rated current values, as well as quiescent current values, were taken into consideration.

To provide the required 2.5 V common-mode and 1.7 V bias voltages, high-precision voltage references from the TI REF35 series were selected, as they offer the necessary output voltage levels. For the 3.3 V supply rail, the TI TPS7A20 ultra-low noise low-dropout (LDO) linear regulator was chosen due to its ability to deliver up to 300 mA of output current [20], meeting the load requirements with minimal output ripple.

Additional Light Emitting Diodes (LEDs) are placed for each voltage level for easy determination of voltage level functioning. Furthermore, to be able to supply the board externally during testing, a 2x3 pin with 5 V, 3.3 V, and GND connections are designed in. Ferrite beads that can be desoldered are also placed in series with all the voltage level inputs to be able to completely power the interface board from external sources while it is mounted on the inverter.

Figure 3.16 shows the schematic design of the power sections and testing points of the voltage levels are also present.

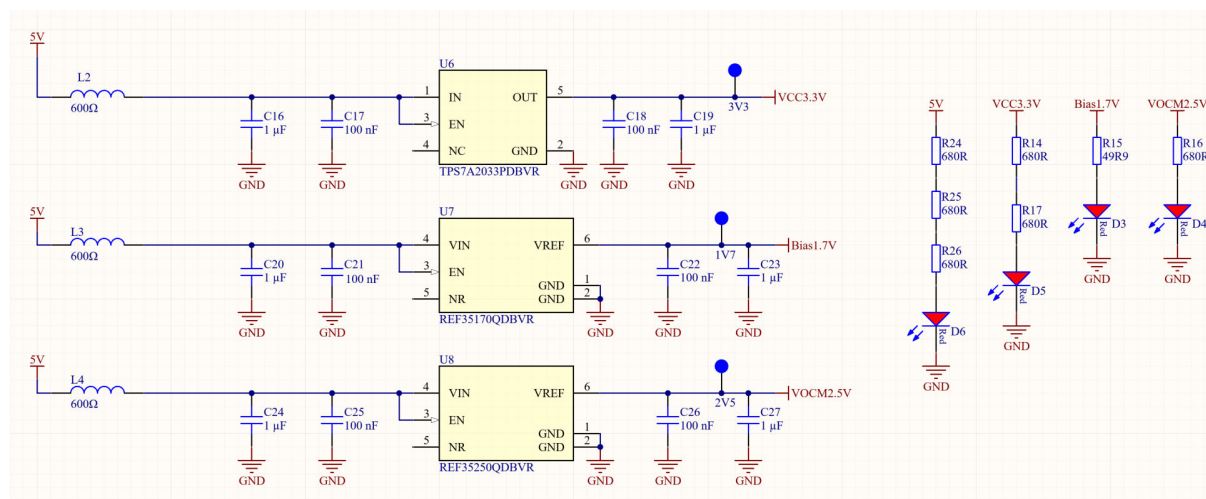


Figure 3.16: Power section schematic design

3.2.5 Interface Board Component Layout

Figure 3.17 shows a top-side view of the interface board. An important priority is keeping the interface compact for easy connection and handling. For this reason, the digital optical transmitters and receivers are stacked on both the top and bottom layers of the board, which is

shown in Figure 3.18. Furthermore, all components are placed on the top layer of the PCB for streamlined assembly and to ensure compatibility with standard surface-mount manufacturing processes. The digital components that require a supply voltage of 3.3 V are grouped together on the left side of the board below the transmitters and receivers. The fully differential amplifier for the current and DC-link voltage sensing signals requires a 5 V input and is grouped together on the right side of the board below the RJ45 connector port. The power section with the voltage references and LDO is kept close to the connector.

The edge card connector used on TI's control board is based on the HSEC8 120-pin edge card connector manufactured by Samtec. However, TI employs a proprietary pin numbering scheme that deviates from the Samtec numbering. This discrepancy should be noted in future designs utilizing the same footprint to avoid potential interface mismatches and connectivity issues.

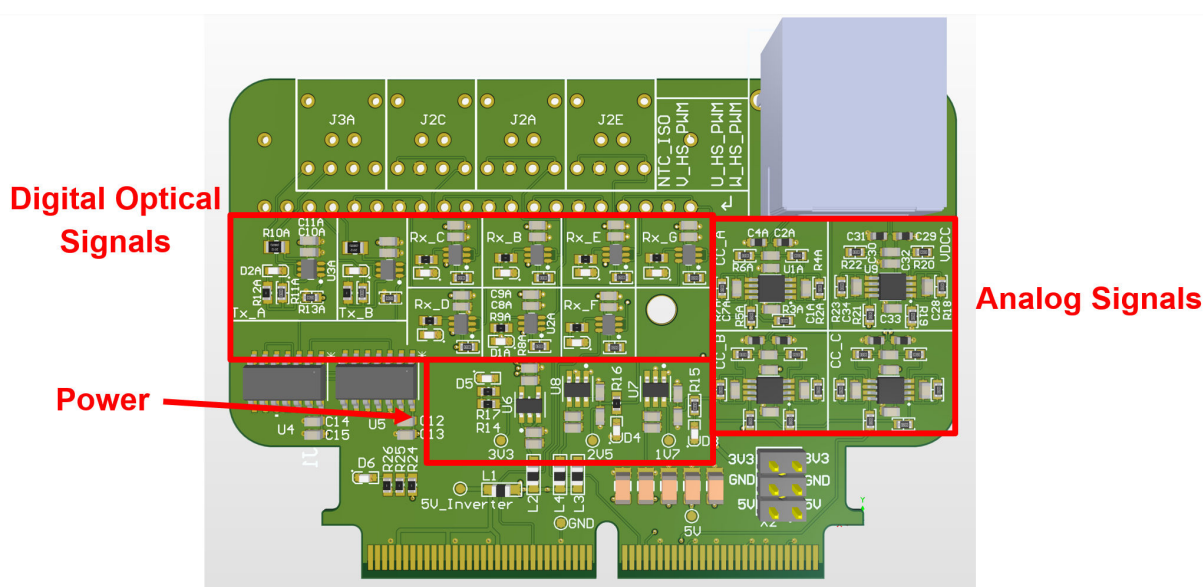


Figure 3.17: Interface board layout

As the operation frequency range of the interface board remains in the kHz range, high-frequency design considerations are not needed.

The interface board has four layers. As the 3.3 V and 5 V components are arranged separately from each other, the two supply voltage polygons can both be placed on layer 2. This leaves layer 3 to be a free GND layer, which is beneficial regarding the current return paths. The top and bottom layers of the board are also covered with GND polygons

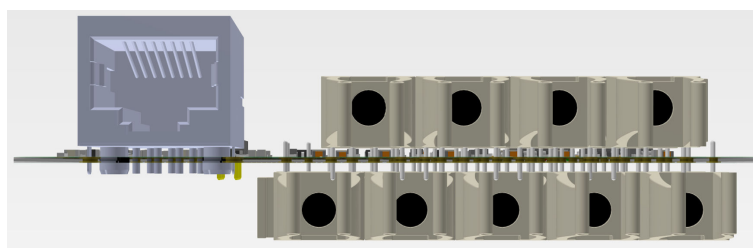


Figure 3.18: Transmitter and receiver stack on top and bottom of interface board

3.2.6 3D-Printed Stand

The Wolfspeed inverter has the edge card connector oriented such that the interface board must be inserted from above, perpendicular to the inverter's surface. This vertical connection leads to mechanical instability, causing the inserted board to wobble. In the case of the interface board, which includes multiple top-mounted cables, the risk of mechanical stress and potential damage, particularly to the edge card connector, is significantly increased. To mitigate this, a custom stand has been designed with a through-hole aligned on the interface board as a screw point. This support ensures a secure and stable connection of the interface board to the Wolfspeed inverter. Figure 3.19 shows the interface board inserted into the inverter with the 3D-printed stand in place.

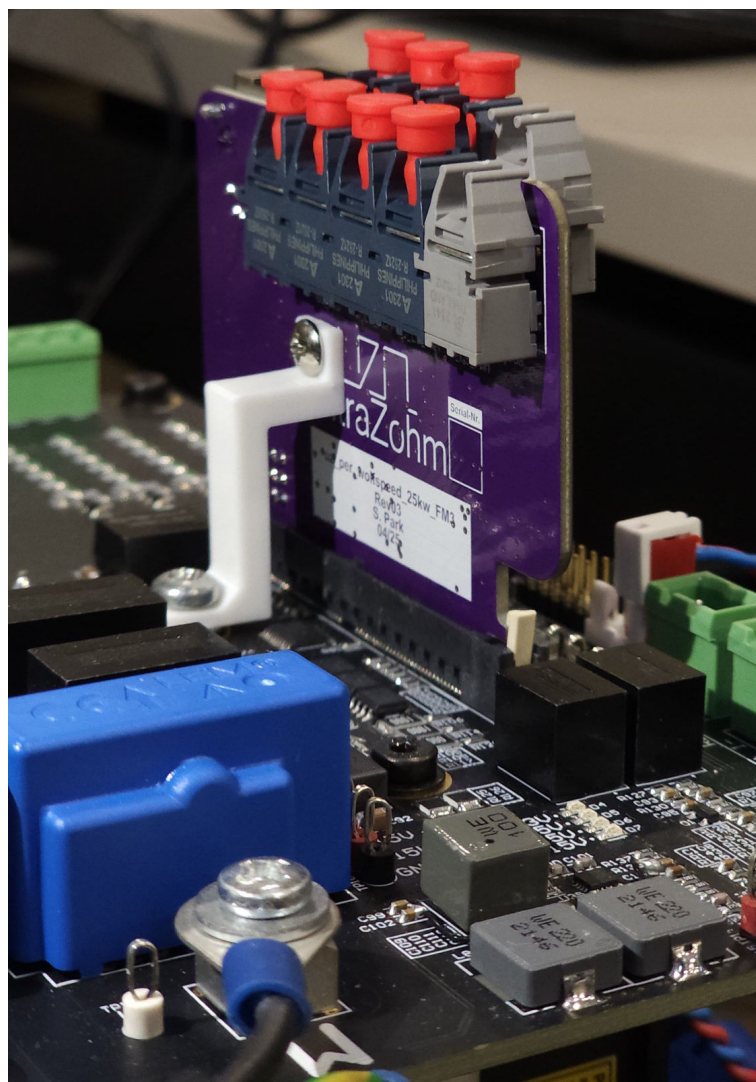


Figure 3.19: Interface board with 3D-printed stand to keep it properly mounted

CHAPTER 4

Testing and Inverter Integration

This chapter presents the testing and integration of the interface board to the Wolfspeed inverter. To ensure reliable operation, a structured and methodical testing procedure was followed.

4.1 Structure of Testing and Integration Process

The interface board was ordered from JLCPCB, and the final version was assembled with all of the surface mount components, RJ45 Ethernet port, and external 2x3-pin header. The only components not assembled during manufacturing were the nine digital optical transmitters and receivers, which had to be manually soldered due to their placement on both the top and bottom layers of the PCB. For initial verification, an unpopulated version of the board was ordered, allowing for manual assembly of selected components. This was done using the pick-and-place machine and oven in the Chair of High-Power Converter Systems (HLU) laboratory.

The testing process began with board bring-up, manually soldering and verifying individual components and signal paths, including transmitters, receivers, and analog sensing sections. Using the TI TMDSHSECDOCK HSEC180 control card baseboard docking station, a 5 V supply was connected to the board, and specific pins of the HSEC180 edge card connector could be driven to test specific signal pathways.

Following the confirmation of correct board design, the interface board was plugged in to begin tests with the Wolfspeed inverter and UltraZohm. First, the digital gate signals were tested without any voltage on the DC-link to confirm that the six PWM signals were being transmitted correctly from the UltraZohm to the Wolfspeed inverter. Afterwards, the DC-link was connected, and the analog DC-link voltage and output phase current sensing signals were tested. Finally, the input power was increased and the inverter was tested until 10 kW.

Figure 4.1 and 4.2 show the top and bottom sides of the final interface PCB used to run the tests.

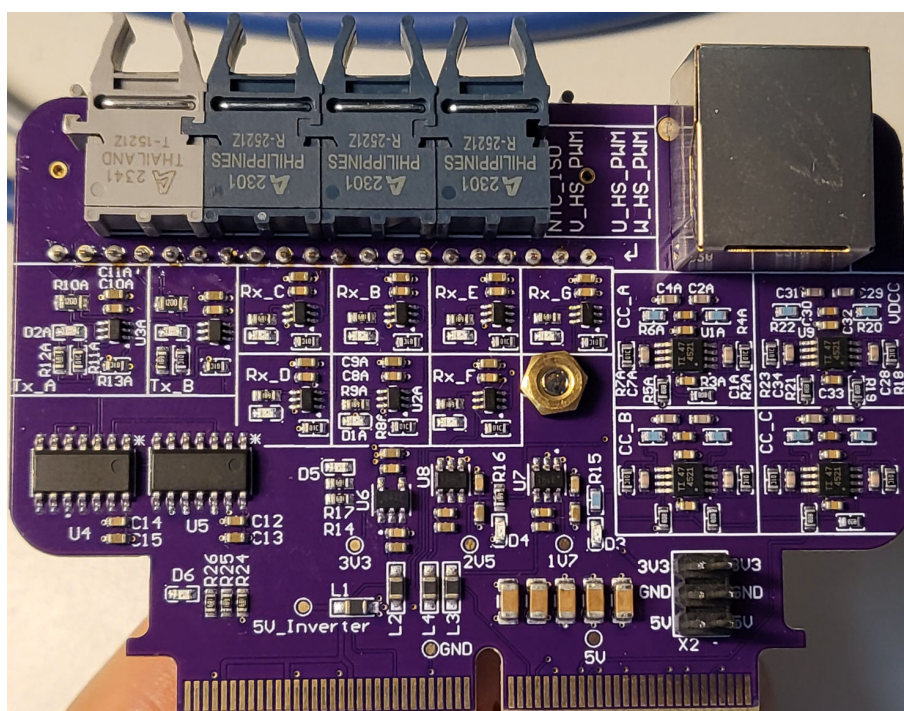


Figure 4.1: Top side of interface board

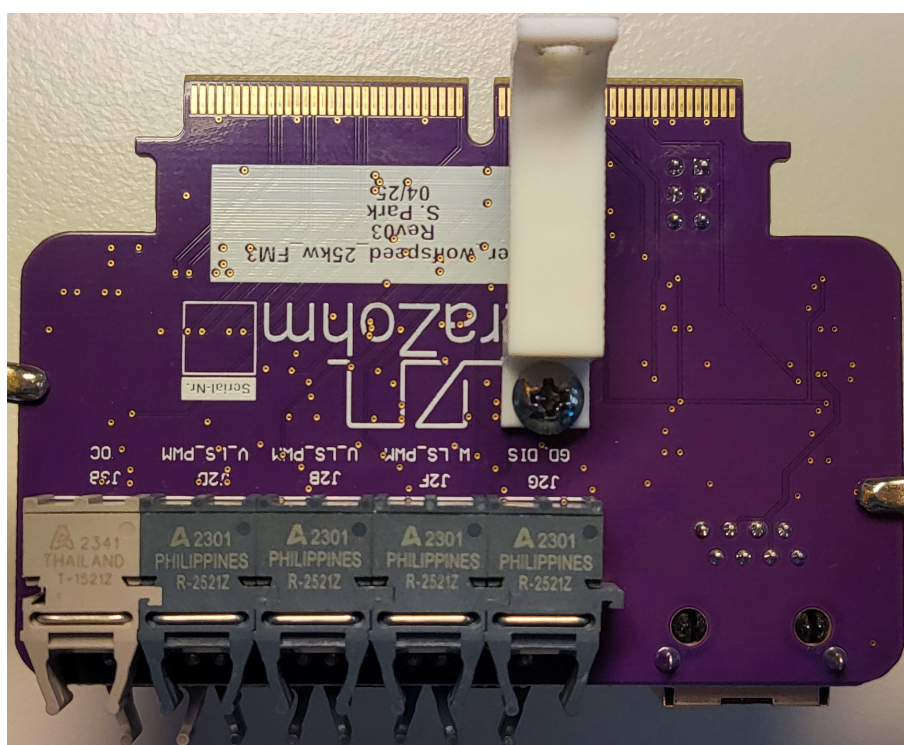


Figure 4.2: Bottom side of interface board

4.2 Board Bring-up

The board bring-up tests were conducted to ensure all signal pathways were working correctly before connecting the interface board with the Wolfpseed inverter and UltraZohm. First, 5 V was supplied to the interface board through the external pin header to ensure the power section converted and correctly referenced the different voltage levels. All of their respective LEDs lit up, indicating the correct functioning of the 3.3 V LDO and 2.5 V, 1.7 V voltage references.

Afterwards, the analog signal pathways for the DC-voltage sensing signal and the output phase current sensing signal were validated. For this test, a range of voltages was driven through the analog signal pins using the TI baseboard docking station. The output differential signals were then measured and recorded.

For this test, the following components were used:

- Texas Instruments TMDSHSECDOCK controlCARD docking station
- Ethernet adapter board
- Keysight 34461A 6.5-digit digital multimeter
- Keysight E36313A triple output programmable DC power supply

Figure 4.3 shows the setup for the board bring up tests. The Ethernet adapter board allows the output differential voltages to be measured.

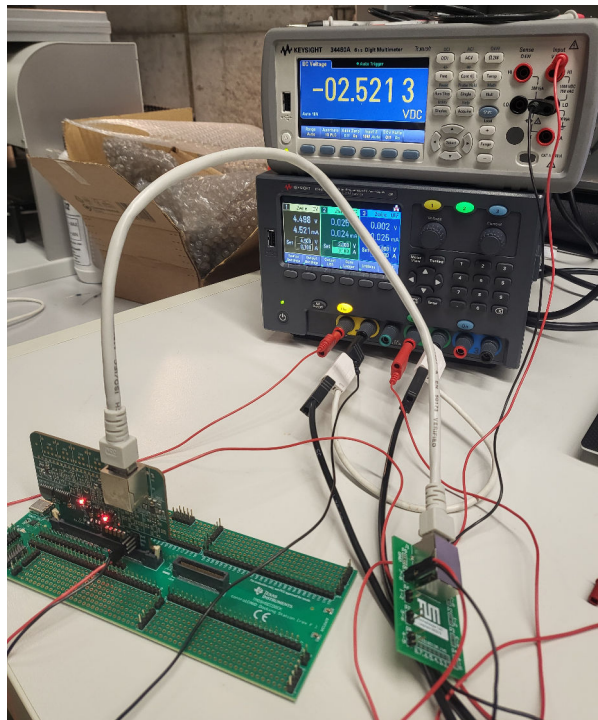


Figure 4.3: Setup for board bring up tests

4.2.1 DC-link voltage sensing pathway test

Table 4.1 shows the differential output signals and the positive and negative outputs for the analog DC-link voltage sensing signal path. When the input signal voltage is plotted against the differential output as shown in Figure 4.4, the gain can be validated through the gradient of the curve. The input signal voltage was tested up to 4.50 V. In the last three measurement points, as the differential output reaches the top 5 V rail, there is an apparent saturation with the values remaining relatively constant even with an increasing input signal.

A line of best fit for the first five points has a gradient of 1.498, which is very close to the theoretical 1.515 needed to translate the sensing signal to the 5 V range for the ADC in UltraZohm.

Input signal voltage (V)	Differential output (V)	Positive output (V)	Negative output (V)
0.00	0.025	2.513	2.489
1.00	1.510	3.256	1.746
2.00	3.014	4.008	0.995
2.50	3.765	4.384	0.619
3.00	4.516	4.759	0.243
3.50	4.923	4.952	0.029
4.00	4.922	4.951	0.029
4.50	4.921	4.951	0.030

Table 4.1: Measured input-output characteristics of the fully differential amplifier for DC-link voltage sensing

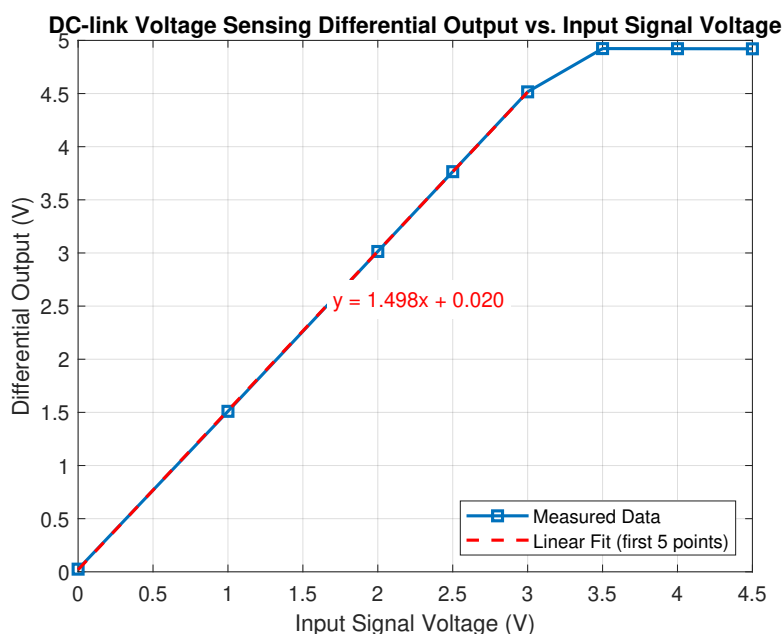


Figure 4.4: Relationship between the input signal voltage and differential output for DC-link voltage sensing path

4.2.2 Output Phase Current Sensing Path Test

Table 4.2 shows the differential output signals as well as the positive and negative outputs for an output phase current sensing signal path. For current sensing, the input signal voltage was started at 1.7 V due to the bias correction that exists on the fully differential amplifier, where the inverting input terminal V_- is connected to 1.7 V.

Input signal voltage (V)	Differential output (V)	Positive output (V)	Negative Output (V)
1.703	0.005	2.503	2.499
1.804	0.155	2.579	2.424
1.905	0.306	2.655	2.348
2.005	0.457	2.730	2.273
2.105	0.608	2.805	2.198
2.203	0.756	2.879	2.123
2.303	0.907	2.955	2.048
2.404	1.057	3.030	1.973
2.504	1.208	3.105	1.897
2.604	1.359	3.181	1.822
2.704	1.510	3.256	1.747
2.803	1.658	3.330	1.672
2.903	1.809	3.406	1.597
3.003	1.959	3.481	1.522
3.103	2.110	3.556	1.446
3.203	2.261	3.632	1.371
3.303	2.412	3.707	1.296
3.502	2.711	3.857	1.146
4.004	3.464	4.233	0.769
4.503	4.216	4.609	0.393
5.002	4.924	4.954	0.303

Table 4.2: Measured input-output characteristics of the fully differential amplifier for output phase current sensing

Figure 4.5 shows the relationship between the input signal voltage and differential output for the output current sensing path on the interface board. The input signal voltage was tested up to 5.002 V. Here a saturation is not seen because if adjusted for the 1.7 V, at an input of 5 V, the differential output is still within the 5 V rail.

A line of best fit has a gradient of 1.498 showing identical gain as for the DC-link path. A difference is the large offset from the zero point with the y-intercept being at -2.544. This occurs due to the fact that there is a bias correction of 1.7 V on the input of the fully differential amplifier. Therefore, an input signal voltage of around 1.7 V is equal to a differential output of 0 V.

4.2.3 Digital Signal Path Test

There are nine digital signal paths that need to be tested, which are for 2 transmitters and 7 receivers on the interface board. For the 2 transmitter paths, the TI docking station was used to

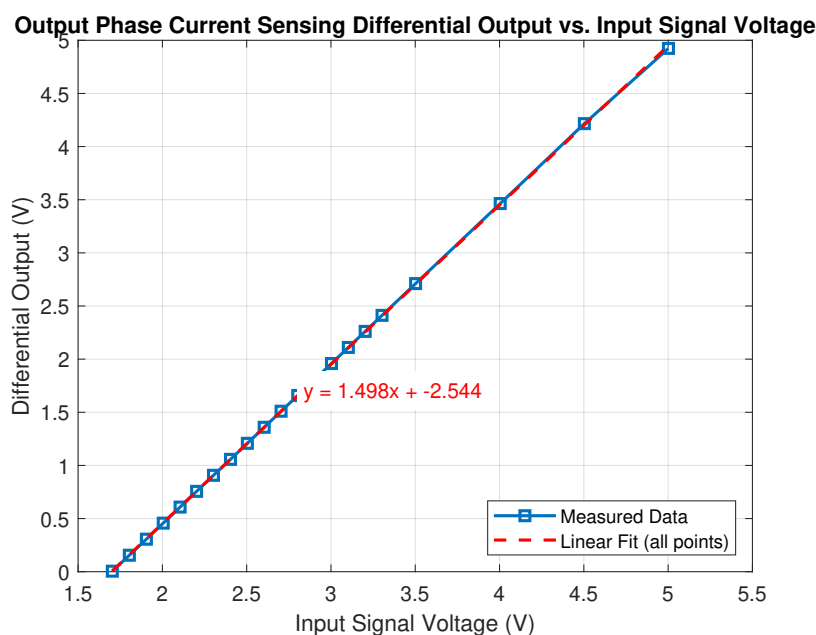


Figure 4.5: Relationship between the input signal voltage and differential output for output phase current sensing path

drive the overcurrent detection signal pins and NTC temperature pin. When this was done, the LEDs for both paths lit up, indicating signal transmission.

To test the receiver paths which consist of six gate signal and one gate driver disable signal paths, the input of the receiver footprint was physically brought down to GND, which indicated signal transmission according to the receiver logic. When this was done, LEDs for all the paths lit up, indicating signal transmission.

Figure 4.6 shows the test setup for the receiver path test. After the paths were confirmed to drive properly, one transmitter and one receiver were soldered on, to drive through the board to confirm the digital optical receiver and transmitter logic.

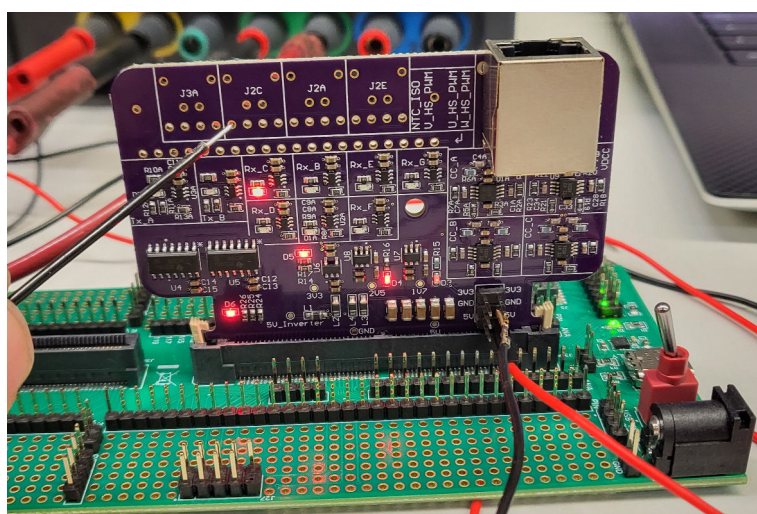


Figure 4.6: Digital receiver signal path test

4.3 Digital Gate Signal Test

After the interface board was brought up and all the signal paths were confirmed to function correctly, it was plugged into the Wolfspeed inverter. However, before connecting any DC voltage, the digital gate signals were tested to verify proper transmission from UltraZohm to the inverter.

Using the Tektronix TBS2000 series 100 MHz digital oscilloscope, the gate signals were measured on the Wolfspeed inverter. The probes needed to be hand-held as there are no hooks on the inverter to keep the probes in place. Furthermore, there is no GND connection close to the gate signal measurement points, so the GND clip was attached to the negative DC input voltage terminal.

Figure 4.7 shows the oscilloscope measurements for one gate signal. The high-side and low-side gate signals are complementary to each other, confirming correct transmission from UltraZohm. The dead-time settings were also tested and confirmed by changing the parameter on UltraZohm. The Wolfspeed inverter itself also includes input signal interlocks, which prevent the gate drivers from turning on when the high/side and low/side switch positions are commanded on simultaneously [4].

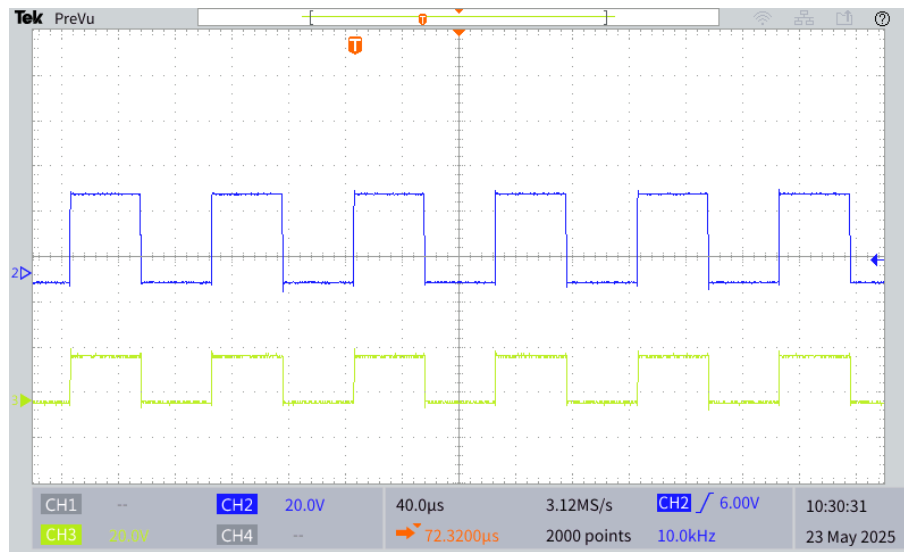


Figure 4.7: Digital gate signal oscilloscope measurement

4.4 Analog Sensing Signal Verification

After the digital gate signals were confirmed to be properly transmitting from UltraZohm to the Wolfspeed inverter, the analog sensing signals were tested and read in the UltraZohm system. For input DC-link power, the Elektro-Automatik EA-PSI 9750-06 1.5 kW and Keysight E36313A triple output DC power supply were connected in series to provide up to 800 V with a maximum of 10 A at the input.

4.4.1 DC-link Voltage Sensing

First, the DC-link was connected to the inverter using the power supplies. No gate signals were transmitted; therefore, no current was transmitted, and using the power supply, the DC-link voltage was varied from 0 V to 750 V, which is almost the full rated range of the inverter, and the voltage sensing signal on UltraZohm was recorded.

Figure 4.8 illustrates the relationship between the DC-link voltage and the corresponding sensed voltage. The slope of the linear best-fit line represents the gain from the DC-link voltage to the sensed signal. The measured gradient of 0.003744 closely matches the theoretical value of 3.765×10^{-3} derived in Section 3.2.2.2 in equation 3.8, with negligible offset at zero. This close match validates the accuracy of the DC-link voltage sensing circuit.

The inverse of the measured gain, 0.003744^{-1} was programmed into the UltraZohm for the correct translation of the sensed voltage values.

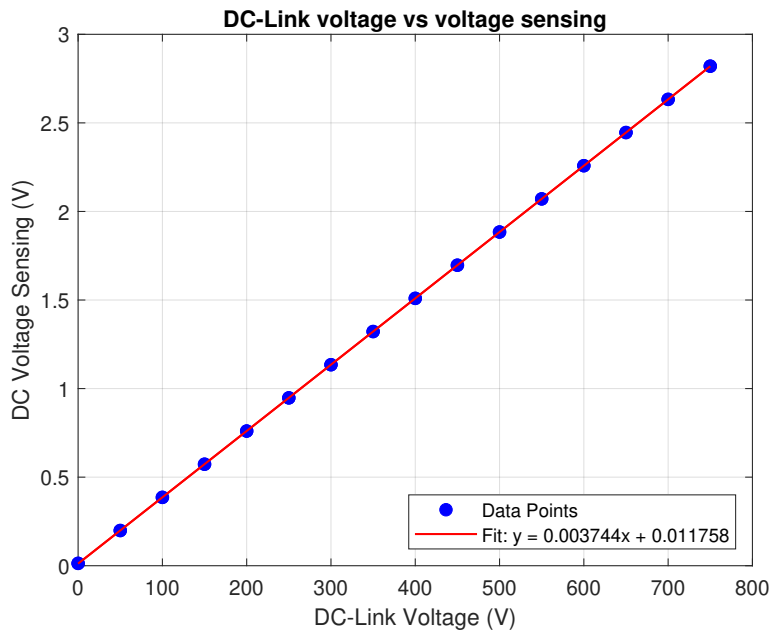


Figure 4.8: Relationship between DC-link voltage and voltage sensing value

4.4.2 Output Phase Current Sensing

To test the current sensing, two phases of the inverter were connected in series through a variable resistor. The high side switch of phase 1 and the low side switch of phase 2 were left conducting, creating a current path positively through phase 1, through the variable resistor load, and back negatively through phase 2. A schematic of this setup is shown in Figure 4.9. This was also done for phases 2 and 3 to properly test all output current paths.

The input DC-link current was varied from 0 A to 10 A due to the limits of the power supply. The inverter itself is rated for up to an output RMS phase current of 30 A.

Figure 4.10 shows the relationship between the DC-link input current and the phase current sensing value. As there is no switching involved, the DC-link input current is equal to the

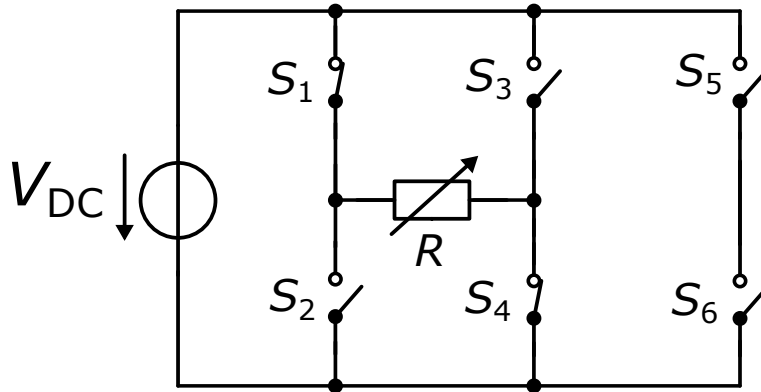


Figure 4.9: Schematic of current sensing test setup

output phase current. The gradient of the linear best-fit line represents the gain from the output phase current to the sensed signal. The measured gradient of 0.024169 is reasonably close to the calculated theoretical value of 0.0201 in equation 3.5.

The current sensing signals exhibit a general downward offset. This is due to the discrepancy between the actual bias of around 1.68 V that the Wolfspeed inverter introduces and the correction factor of 1.7 V used on the interface. To compensate for this offset, a calibration routine was implemented in the UltraZohm. Prior to operation, the system samples 100 data points, computes their average, and subtracts this baseline value from all subsequent current measurements to correct for the offset.

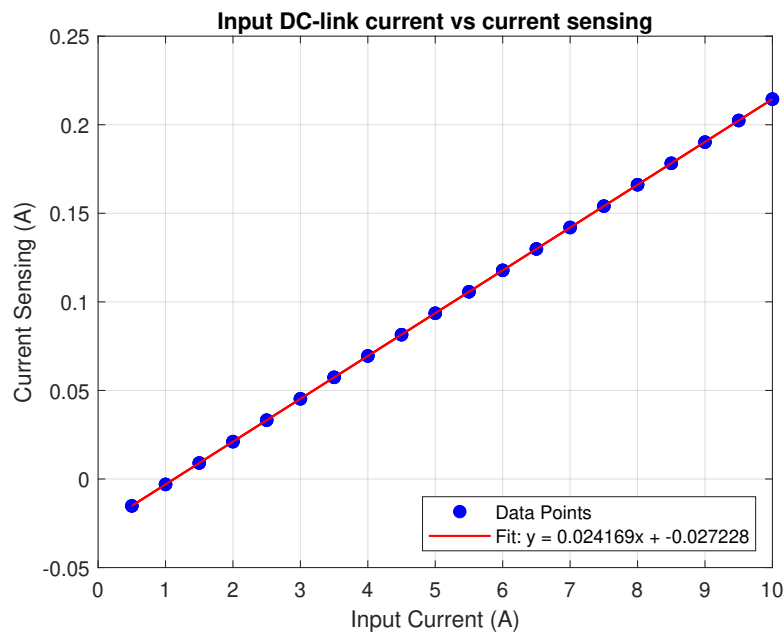


Figure 4.10: Relationship between DC-link input current and phase current sensing value

4.5 Integrated Testing

The last testing stage involved connecting loads to the outputs of the Wolfspeed inverter and evaluating its performance under switching conditions to generate sinusoidal output currents.

For the final integrated testing, the following components were used:

- Sourcetronic SBRU 10 kW/14 Ohm brake resistor
- Hammond Manufacturing 195C20 1 mH inductor
- Elektro-Automatik EA-PSI 9750-06 1.5 kW programmable power supply
- Elektro-Automatik EA-PS 81000-30 10 kW power supply
- Rohde & Schwarz MXO 5 series 2 GHz 8-channel oscilloscope

Each phase was hooked up to an RL load using 14 Ohm resistors and 1 mH inductors in series. To begin, the EA-PSI 9750-06 power supply was used to slowly increase the input power up to its 1.5 kW limit and measure the output currents and phase voltage. For the measurements, the Rohde & Schwarz MXO 5 series 2 GHz oscilloscope was used, with three current probes and one differential voltage probe to measure the output currents of each phase as well as one output phase voltage.



Figure 4.11: Integrated testing setup with resistors and inductors

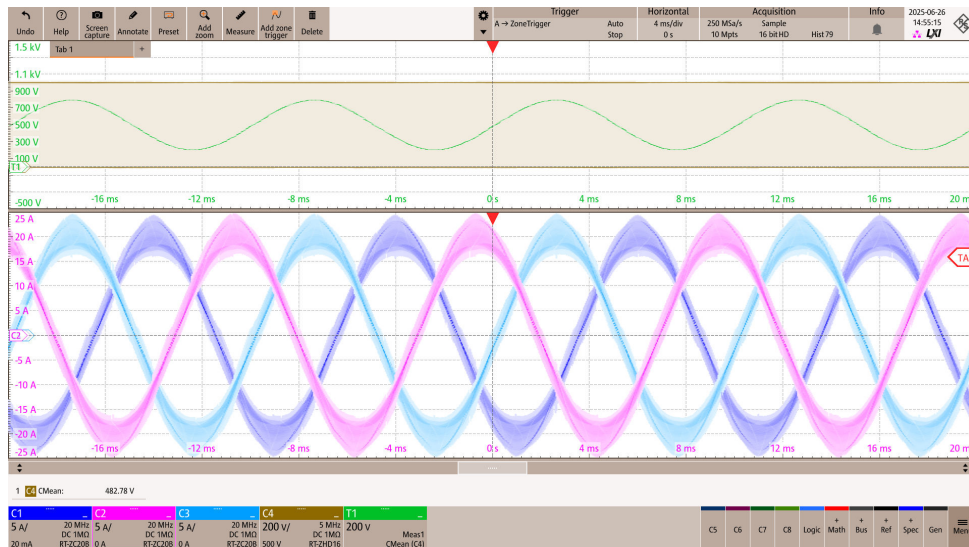
Afterwards, the inverter was tested with higher input power levels - up to approximately 10 kW - using the EA-PS 81000-30 power supply. Figure 4.12 shows the oscilloscope measurements of the inverter's output at three different switching frequencies, with a constant DC-link voltage of 999 V and a modulation index of 0.3. In each subfigure, the upper section displays

the measured output phase voltage, where the green trace represents the average of the PWM waveform. The lower section shows the corresponding three-phase output currents.

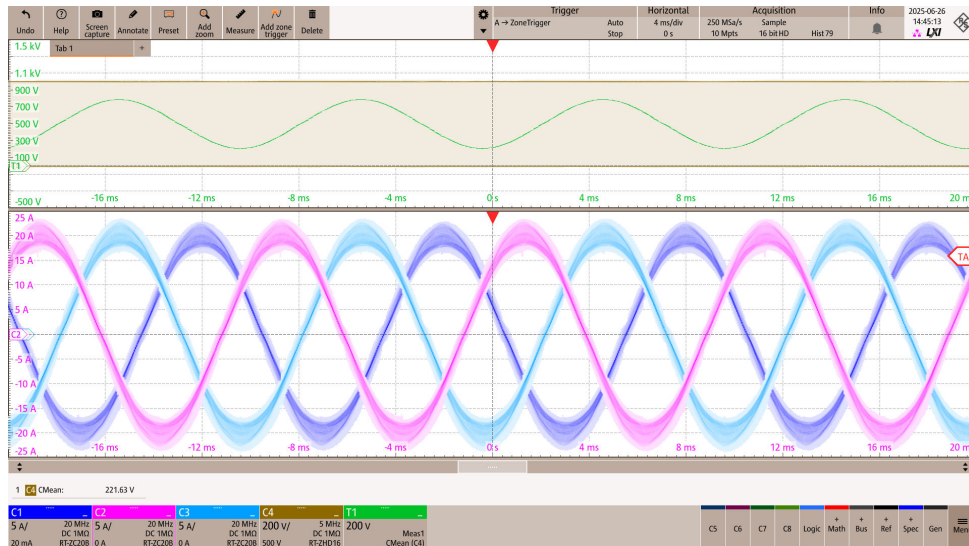
The measurements were taken at switching frequencies of 25 kHz, 50 kHz, and 100 kHz, spanning from the nominal operating frequency up to the maximum value. As expected, an increase in switching frequency results in a noticeable reduction in output current ripple, demonstrating improved waveform quality. Additionally, a decrease in input DC-link current was observed with increasing switching frequency.

Furthermore, in addition to sinusoidal PWM, alternative modulation strategies - namely negative discontinuous PWM and Discontinuous PWM (DPWM1) - were also evaluated. The corresponding waveforms for these tests are provided in Figure B.1 in the appendix.

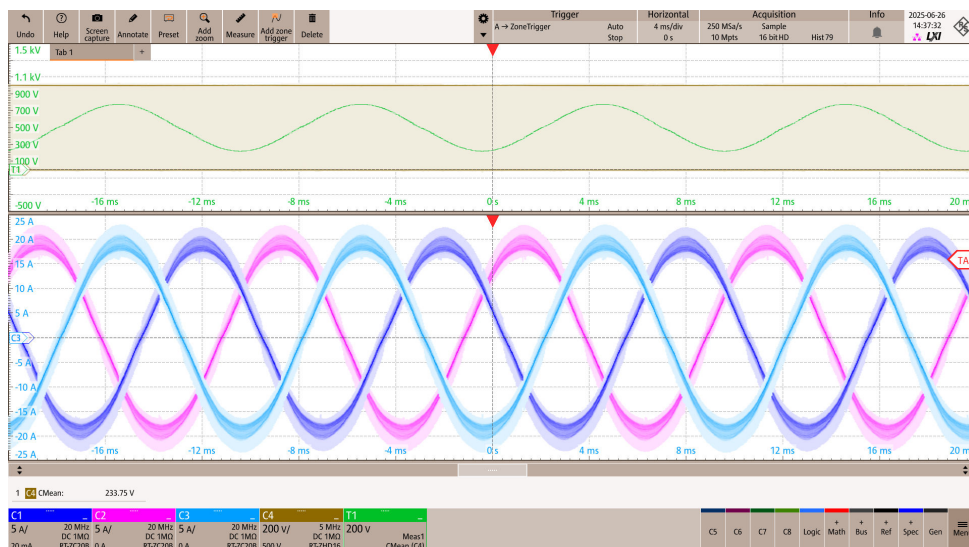
The measurements from the oscilloscope confirm that the interface board and inverter system function reliably under increased power levels and varying switching frequencies. Stable sinusoidal output currents were generated across all tested conditions, and the observed reduction in current ripple with increasing switching frequency aligns with expectations. These results complete the functional validation of the interface board and provide a reliable basis for future closed-loop control experiments.



(a) Switching frequency 25 kHz, 999 V / 9.61 A DC-link input



(b) Switching frequency 50 kHz, 999 V / 9.12 A DC-link input



(c) Switching frequency 100 kHz, 999 V / 8.33 A DC-link input

Figure 4.12: Comparison of output waveforms at different switching frequencies with fixed modulation index and DC-link voltage.

CHAPTER 5

Conclusion

5.1 Summary

The goals of this work were

1. to design an interface board to connect the Wolfspeed inverter and UltraZohm systems
2. to validate and test the board design
3. to test the Wolfspeed inverter with the UltraZohm

Within this thesis, all three points have been completed and tested successfully.

5.2 Final evaluation

The objective of this bachelor's thesis was to design and test an interface board compatible with the Wolfspeed CRD25DA12N-FMC 25 kW two-level three-phase inverter, enabling its integration with the UltraZohm high-performance real-time control platform. The interface board is designed to receive seven digital optical signals - consisting of six PWM gate switching signals and one gate driver disable signal - and transmit two digital optical feedback signals for NTC temperature monitoring and overcurrent detection. In addition, the board differentially transmits analog signals corresponding to the DC-link voltage and output phase currents to the UltraZohm for inverter control.

The design phase involved a detailed analysis of the Wolfspeed inverter's circuitry to determine appropriate signal conditioning, including gain and biasing requirements, for both analog and digital paths. Special attention was given to minimizing the board's footprint and ensuring all components were mounted on the top layer for streamlined manufacturing. Therefore, the digital optical transmitters and receivers were stacked on the top and bottom layers.

A structured and incremental testing process was followed. Initial board bring-up tests validated the power supply section as well as the functionality of both digital and analog signal pathways. Afterwards, the board was integrated with the Wolfspeed inverter. Comprehensive testing confirmed proper transmission of gate driver control signals and accurate DC-link voltage and output phase current sensing signals.

Finally, the inverter was operated up to power levels of 10 kW across different switching frequencies. The interface board reliably maintained signal integrity throughout, demonstrating its successful integration with the inverter.

5.3 Outlook

With the interface board successfully validated, it is now ready for use in further experimental setups with the Wolfspeed inverter. Users of the UltraZohm platform can directly connect to the inverter and perform advanced control experiments.

Further testing of the interface board could involve operating the inverter with a three-phase motor as a load to closely replicate real-world applications and evaluate dynamic performance under different load conditions.

On the design side, minor improvements such as resolving floating pins currently present in the AND gate circuitry could enhance signal reliability. Additionally, adapting the interface board design for compatibility with other Wolfspeed inverter models operating at different power levels would broaden its applicability.

APPENDIX A

List of symbols and abbreviations

A.1 List of symbols

Used symbols:

In the following the most important symbols are listed which are used within this work.

General symbols:

D	Duty cycle
t_{on}	High side switch on time
T_s	Period
f_s	Frequency

General electrical variables:

v	Voltage
i	Current
R	Resistor
C	Capacitor
L	Inductor
P	Power

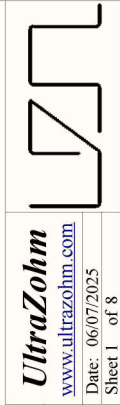
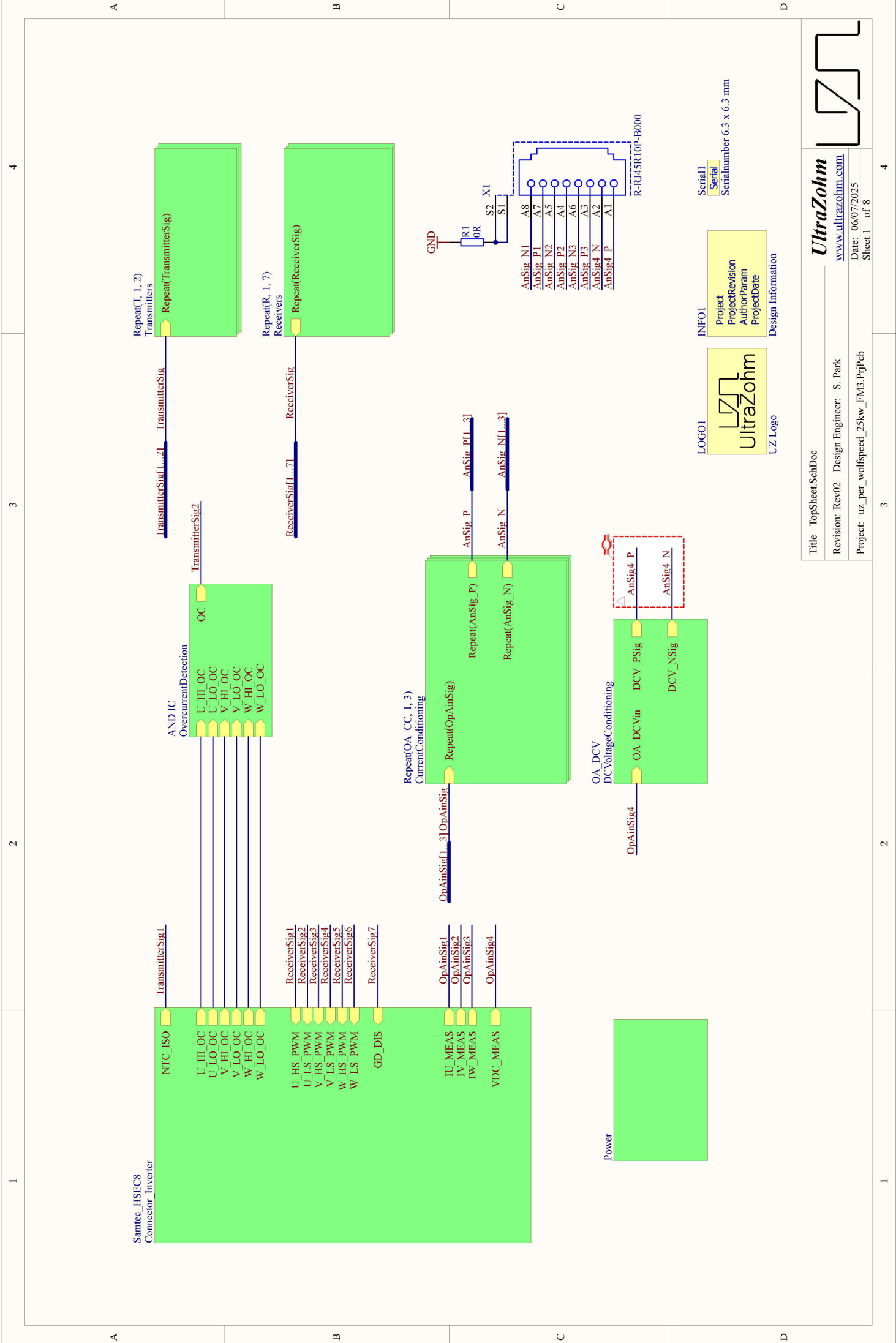
A.2 List of abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
CAN	Controller Area Network
DC	Direct Current
DPWM	Digital Pulse Width Modulation
EMI	Electromagnetic Interference
EV	Electric Vehicle
FPGA	Field Programmable Gate Array
GND	Ground
HLU	Chair of High Power Conversion Systems
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
LDO	Low Dropout Regulator
LED	Light Emitting Diode
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPC	Model Predictive Control
NTC	Negative Temperature Coefficient
Op-Amp	Operational Amplifier
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RMS	Root Mean Square
Rx	Receive
Si	Silicon
SiC	Silicon Carbide
TI	Texas Instruments
Tx	Transmit
WBG	Wide Bandgap

APPENDIX B

Additional Project Data

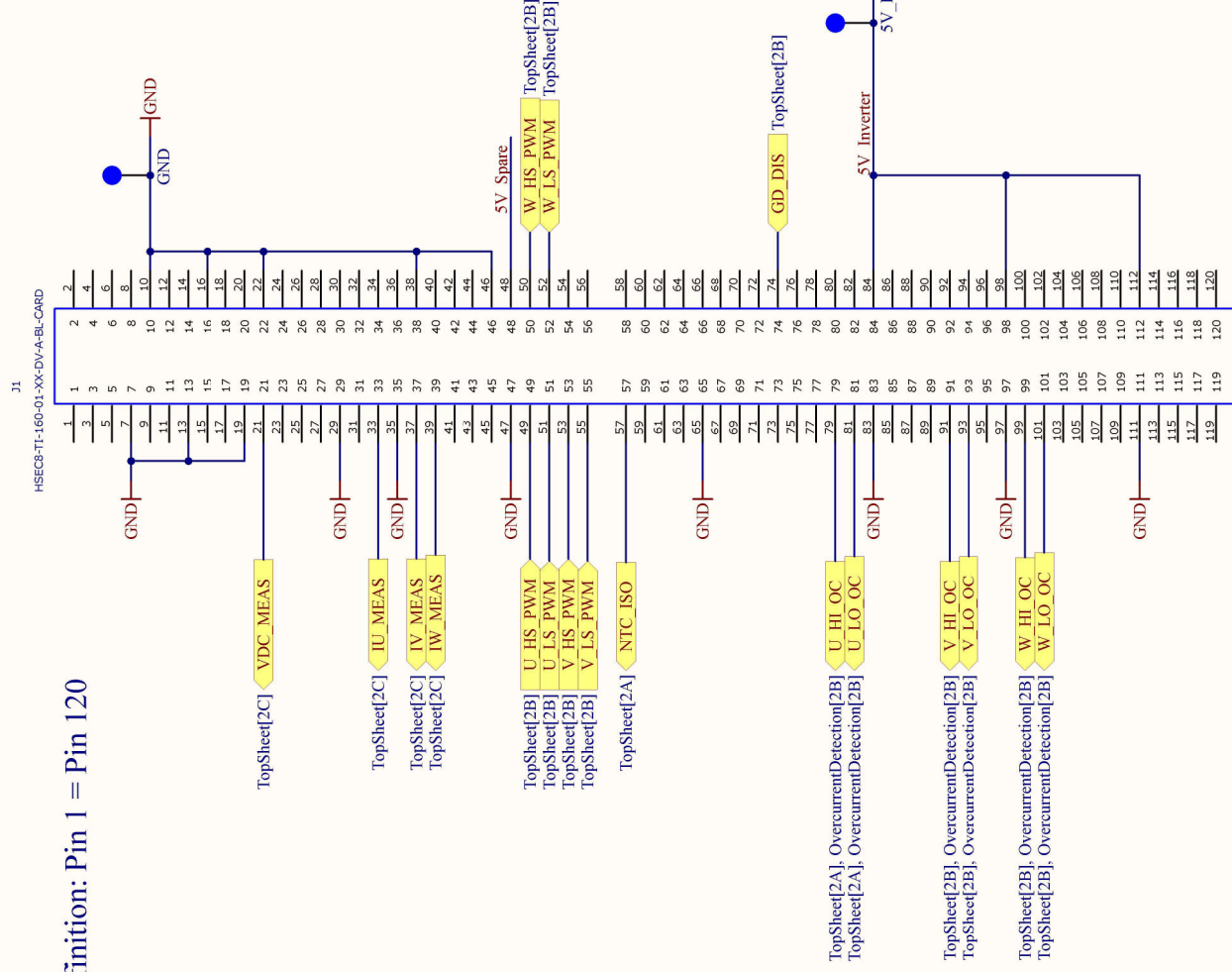
B.1 Circuit Diagrams



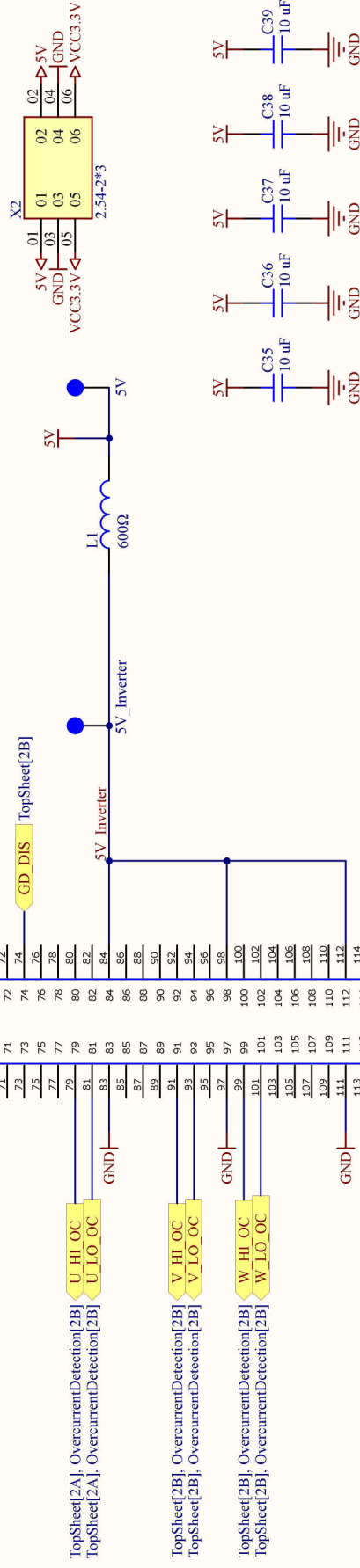
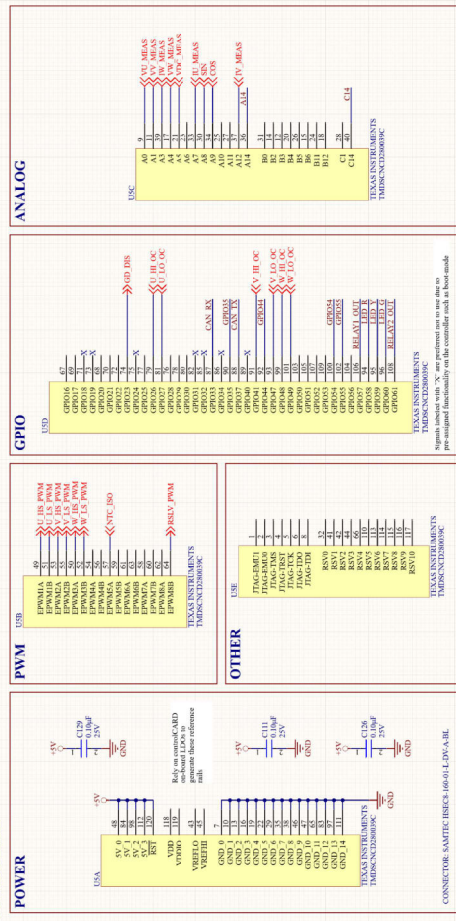
Title TopSheet.SchDoc	
Revision: Rev02	Design Engineer: S. Park
Project: uz_per_wolfspeed_25kw_FM3.PrjPcb	

UltraZohm	
www.ultrazohm.com	
Date: 06/07/2025	Sheet 1 of 8

TI Definition: Pin 1 = Pin 120



CONTROLLER



Correction of 1.68V bias of input signal

$$\text{Gain} = 10/6.65 = 1.50$$

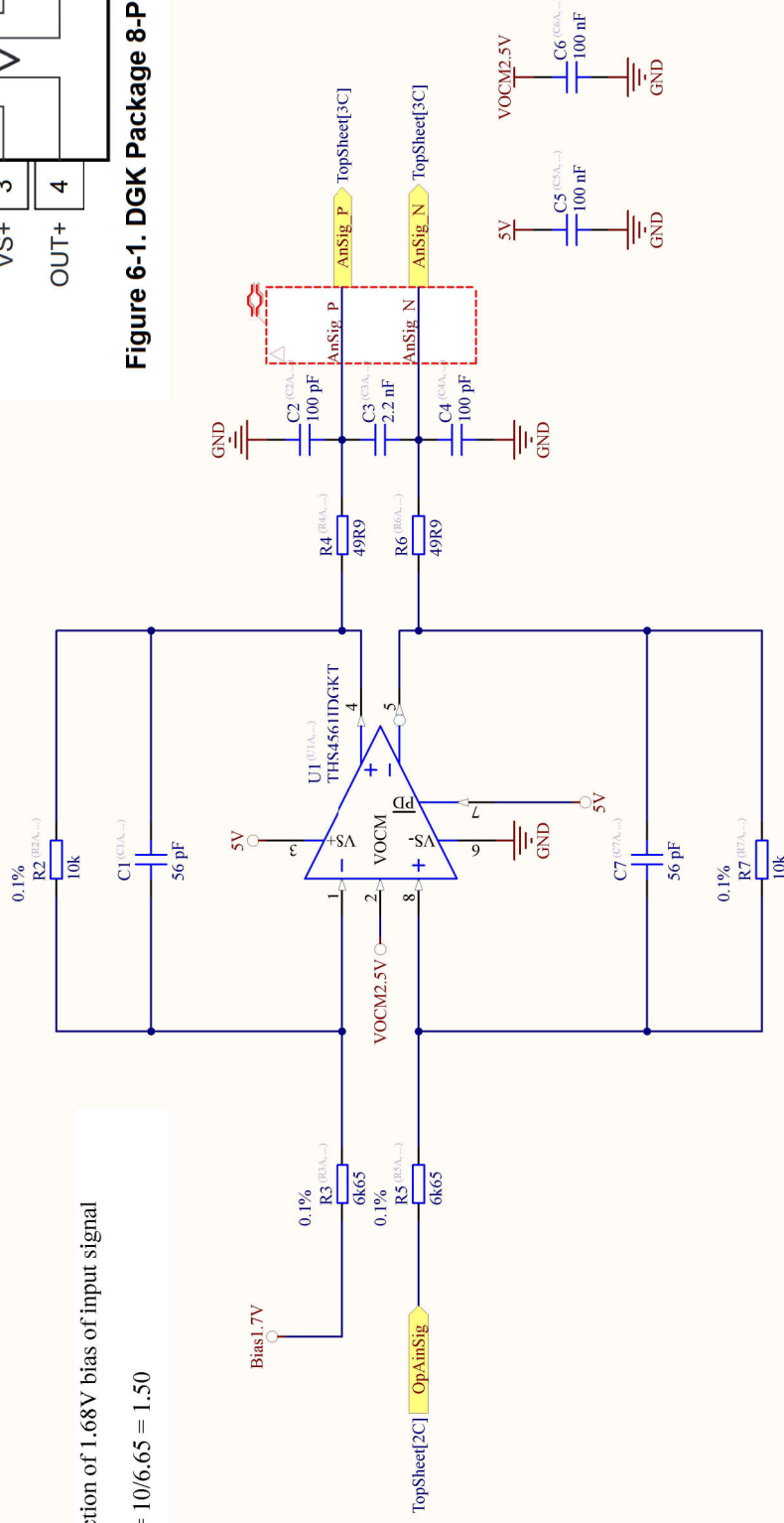
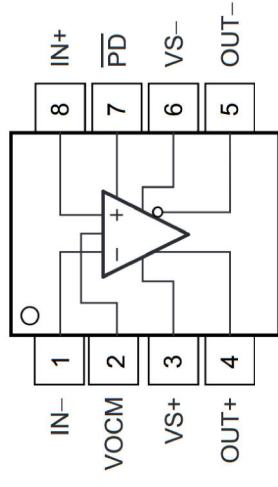


Figure 6-1. DGK Package 8-Pin VSSOP Top View



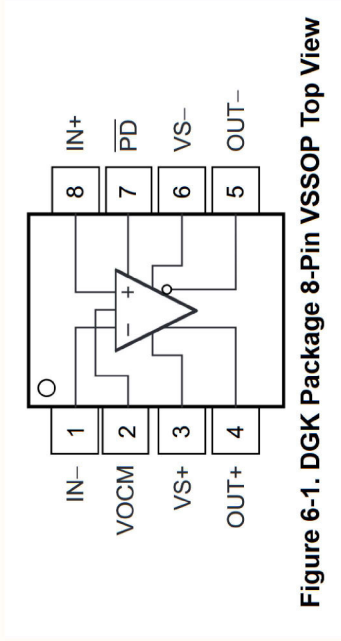
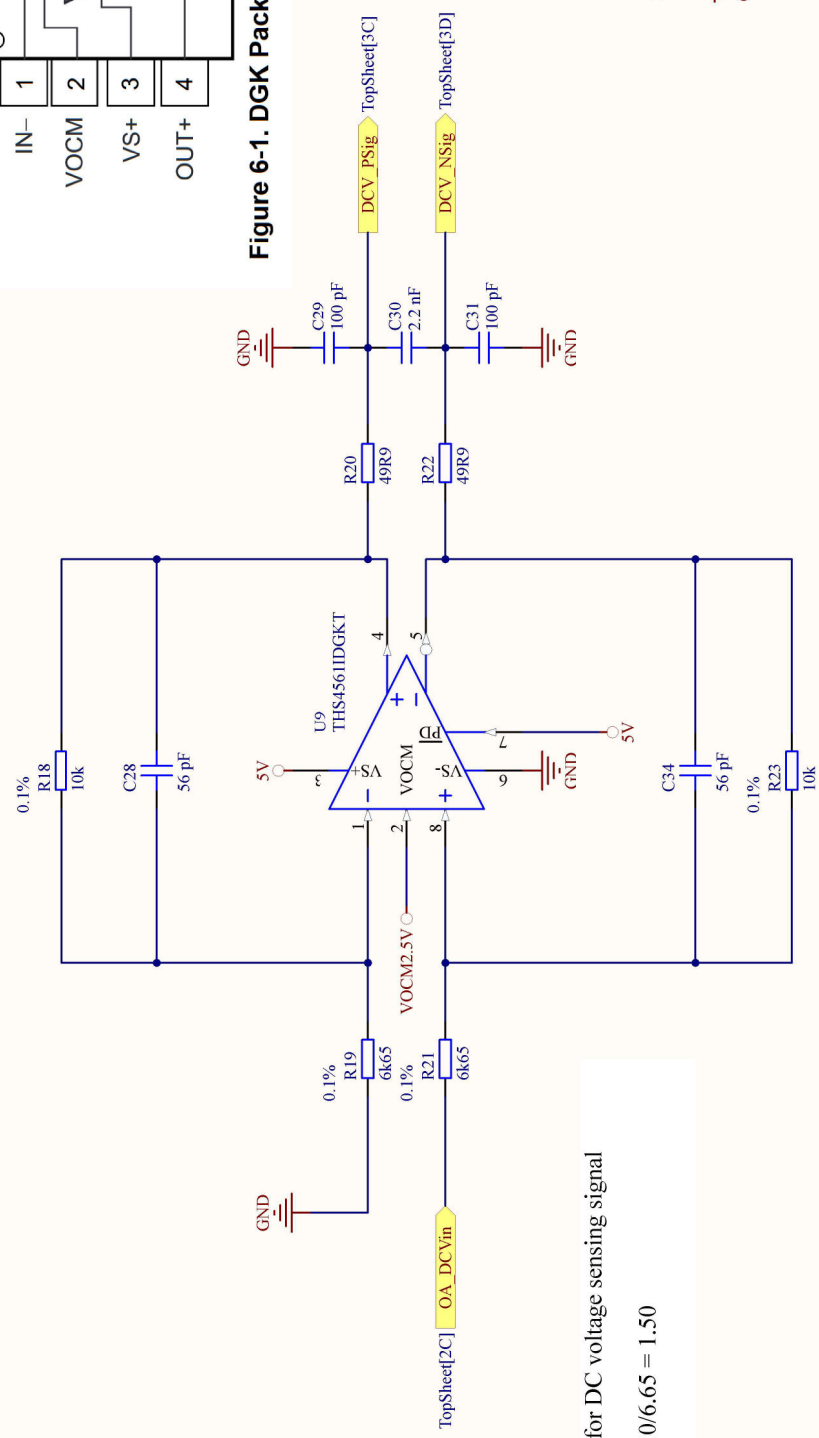
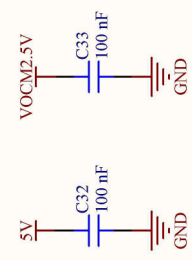


Figure 6-1. DGK Package 8-Pin VSSOP Top View



No bias for DC voltage sensing signal

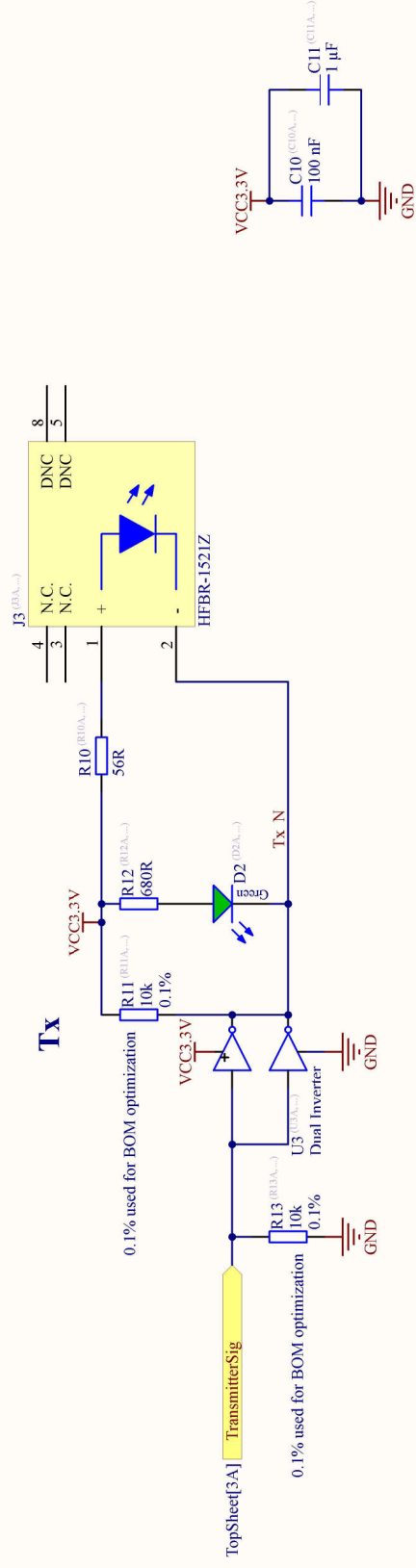
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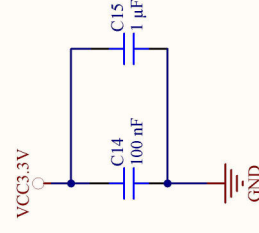
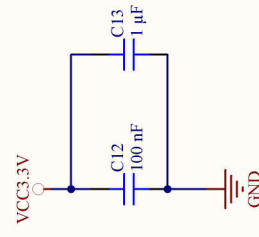
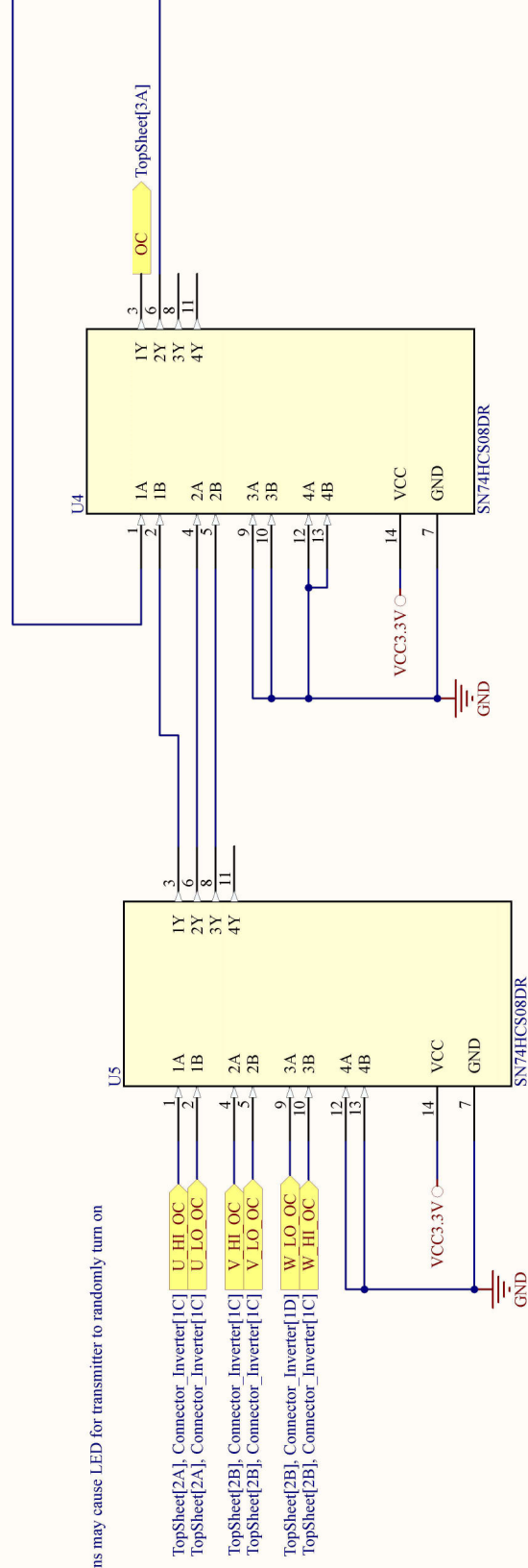
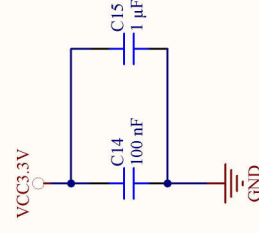
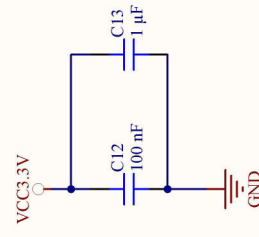
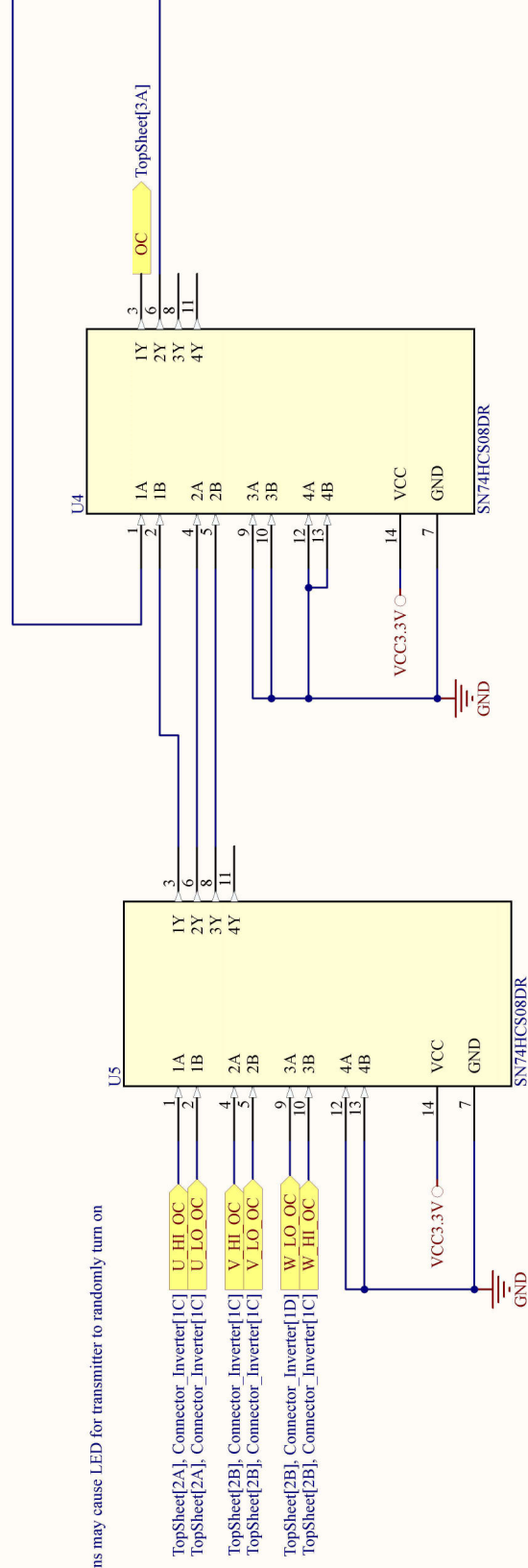
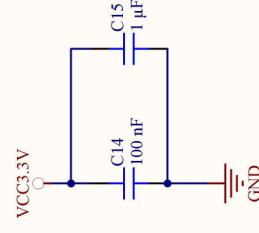
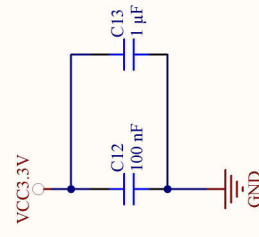
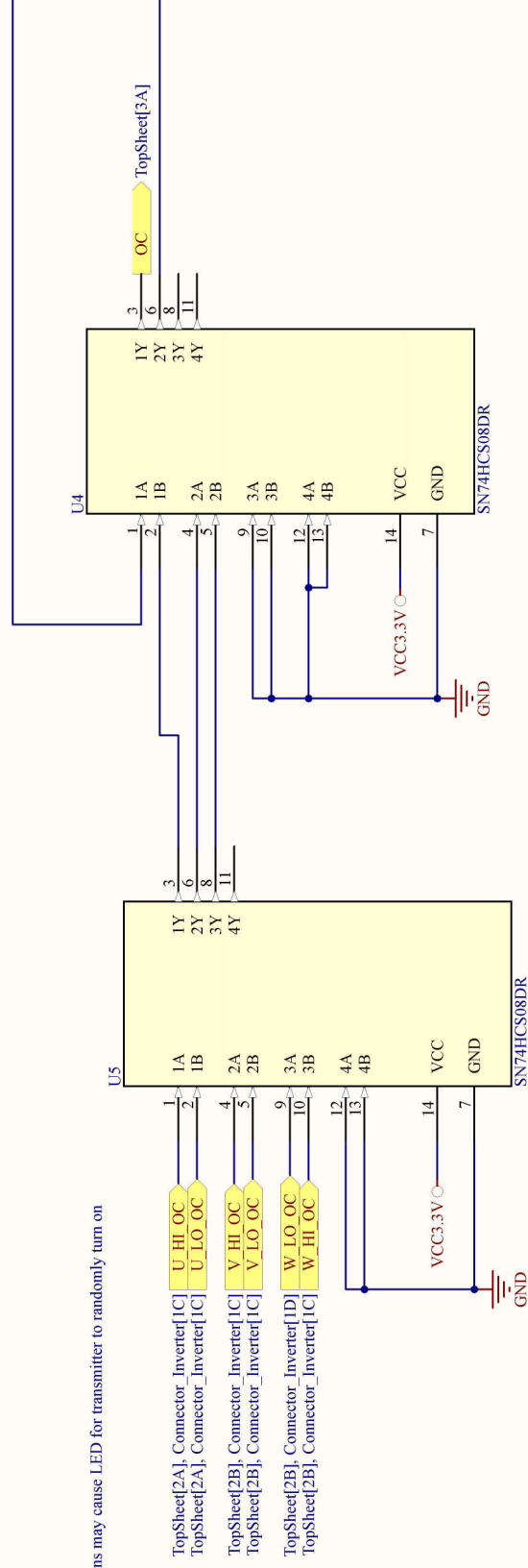
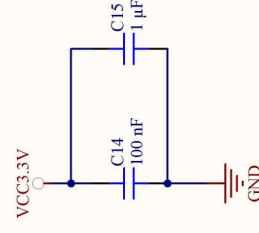
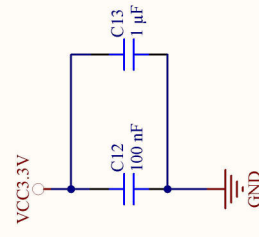
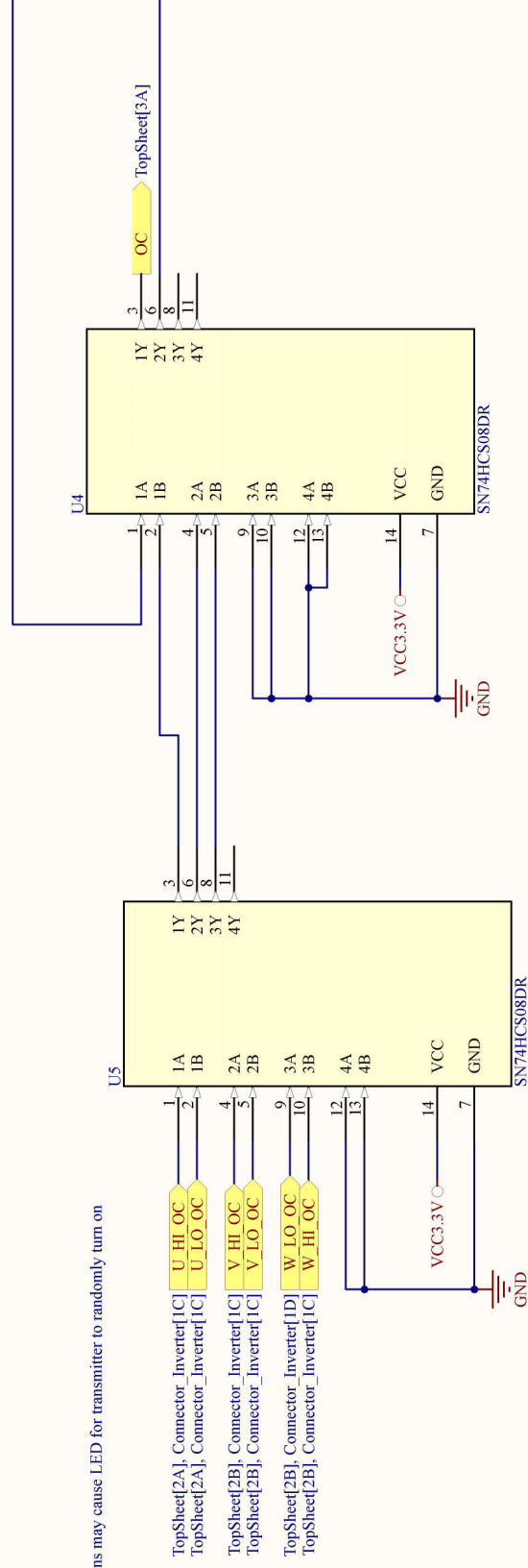


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A	Poor Mans Table of Truth for Rx											
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Receiver LED	Node RxTx	LED D2										
OFF	HIGH	OFF										
ON	LOW	ON										
B												
C												
D	<table><tr><td colspan="2">Title Receivers.SchDoc</td></tr><tr><td>Revision: Rev02</td><td>Design Engineer: S. Park</td></tr><tr><td colspan="2">Project: uz_per_wolfspeed_25kw_FM3.PrjPcb</td></tr></table> UltraZohm www.ultrazohm.com Date: 06/07/2025 Sheet 5 of 8			Title Receivers.SchDoc		Revision: Rev02	Design Engineer: S. Park	Project: uz_per_wolfspeed_25kw_FM3.PrjPcb				
Title Receivers.SchDoc												
Revision: Rev02	Design Engineer: S. Park											
Project: uz_per_wolfspeed_25kw_FM3.PrjPcb												
1	2	3	4									

Poor Mans Table of Truth for Tx

Transmitter LED	Node Tx_N	LED D3	Signal
OFF	HIGH	OFF	LOW
ON	LOW	ON	HIGH

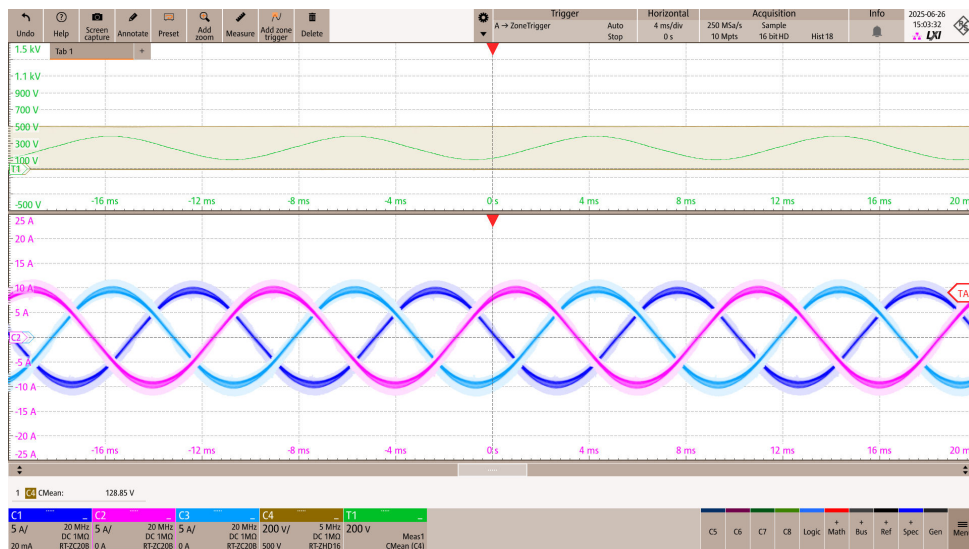




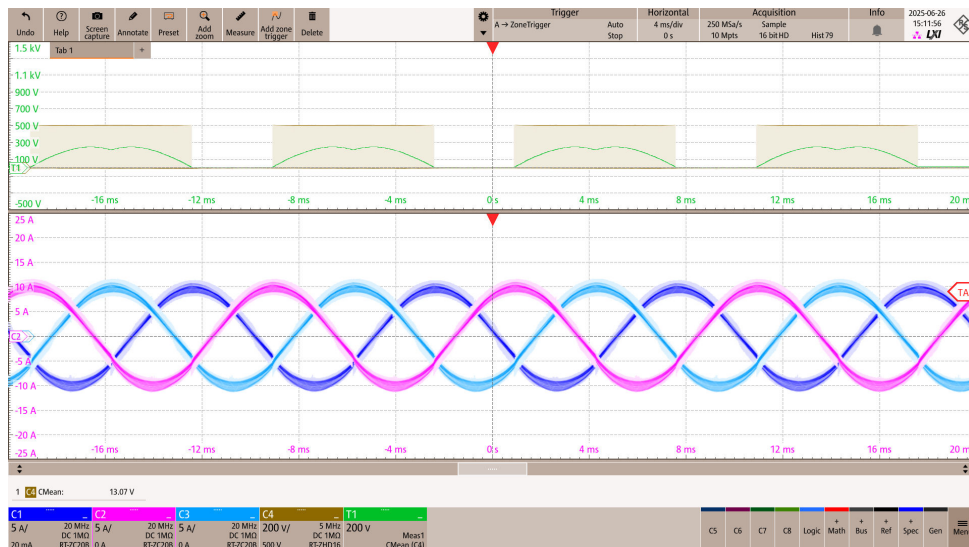
B.2 Bill of Materials

Comment	Description	Quantity	LCSC Part Number
56 pF	Capacitor 0603, 50 VDC, 56 pF, C0G	8	C39148
100 pF	50V 100pF C0G ±5% 0603 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	8	C14858
2.2 nF	Capacitor 0603, 50 VDC, 2.2 nF, X7R	4	C93190
100 nF	Capacitor 0603, 50 VDC, 100nF, X7R	25	C14663
1 µF	Capacitor 0603, 25 VDC, 1 µF, X7R	17	C29936
10 uF	50V 10uF X5R ±10% 1206 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	5	C13585
150060RS75000	WL-SMCW SMD Mono-color Chip LED Waterclear, size 0603, Red, 2 V, 140°	11	C2286
150060GS75000	WL-SMCW SMD Mono-color Chip LED Waterclear, size 0603, Green, 3.2 V, 140°	2	C965804
HSEC8-TI-160-01-XX-DV-A-BL-CARD	MATING CARD LAYOUT FOR HSEC8-160-01-XX-DV-A-BL.	1	
600Ω	WE-CBF SMD EMI Suppression Ferrite Bead, 0805, 600Ω	4	C98308
0R	SMD resistor E24 series	1	C21189
10k	SMD resistor 0.1%, 10ppm	19	C860067
6k65	100mW Thin Film Resistor ±25ppm/°C ±0.1% 6.65kΩ 0603 Chip Resistor - Surface Mount ROHS	8	C861536
49R9	SMD resistor 1%	9	C160046
680R	SMD Resistor 0603	15	C23228
56R	SMD Resistor 0805	2	C17437
THS4561IDGKT	Fully Differential Amplifier, Low-Power, High Supply Range, 60-MHz	4	C2860980
Dual Inverter	This dual inverter is designed for 1.65-V to 5.5-V VCC operation.	9	C116660
SN74HCS08DR	No Description Available	2	C2868021
TPS7A2033PDBVR	No Description Available	1	C2862740
REF35170QDBVR	No Description Available	1	C20345634
REF35250QDBVR	No Description Available	1	C6265005
R-RJ45R10P-B000		1	C386758
2.54-2*3	Pin Header 3x2	1	C5116479

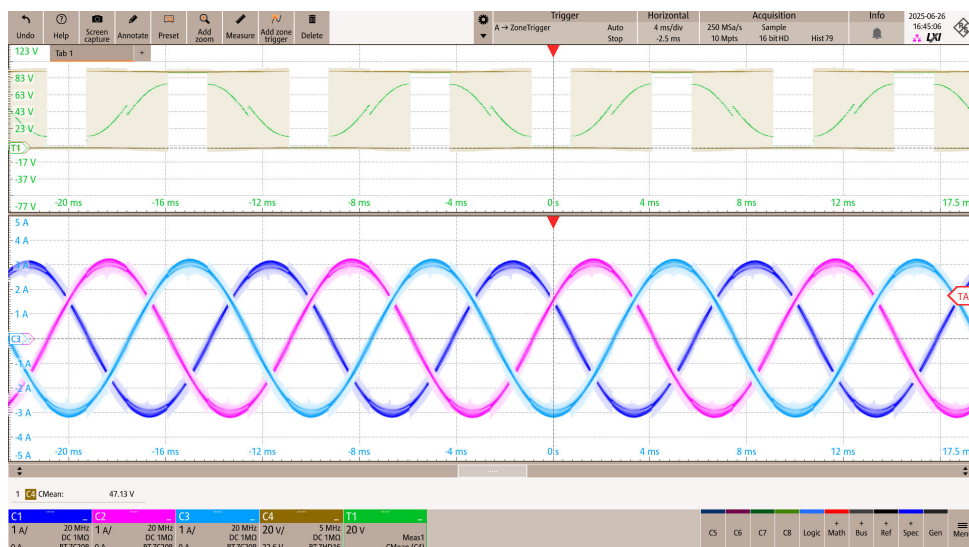
B.3 PWM Modulation Testing Results



(a) Sinusoidal PWM



(b) Negative discontinuous PWM



(c) Positive negative discontinuous PWM

Figure B.1: Testing of different PWM modulation techniques

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