

Place UZ Logo from Library

Revision

Serial
Serial #

Rev04

DC-link-Caps

2.5V_REF

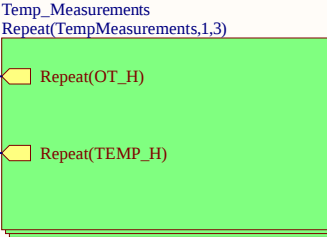
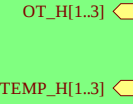
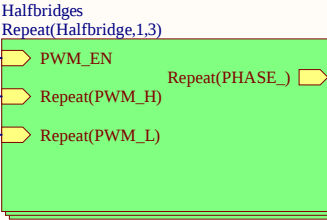
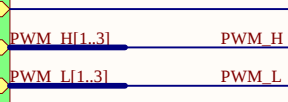
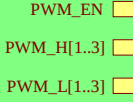
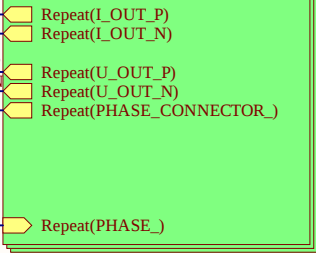
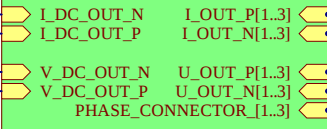
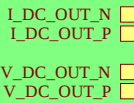
DC-link

Connectors

Phase_Measurements

Repeat(PhaseMeasurements,1,3)

X1
DigitalCarrierJack

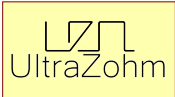


INFO

Project
ProjectRevision
AuthorParam
ProjectDate

Design Information

LOGO1



UZ Logo

Title TopSheet.SchDoc

Revision: Rev04

Design Engineer: K.Patel / D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

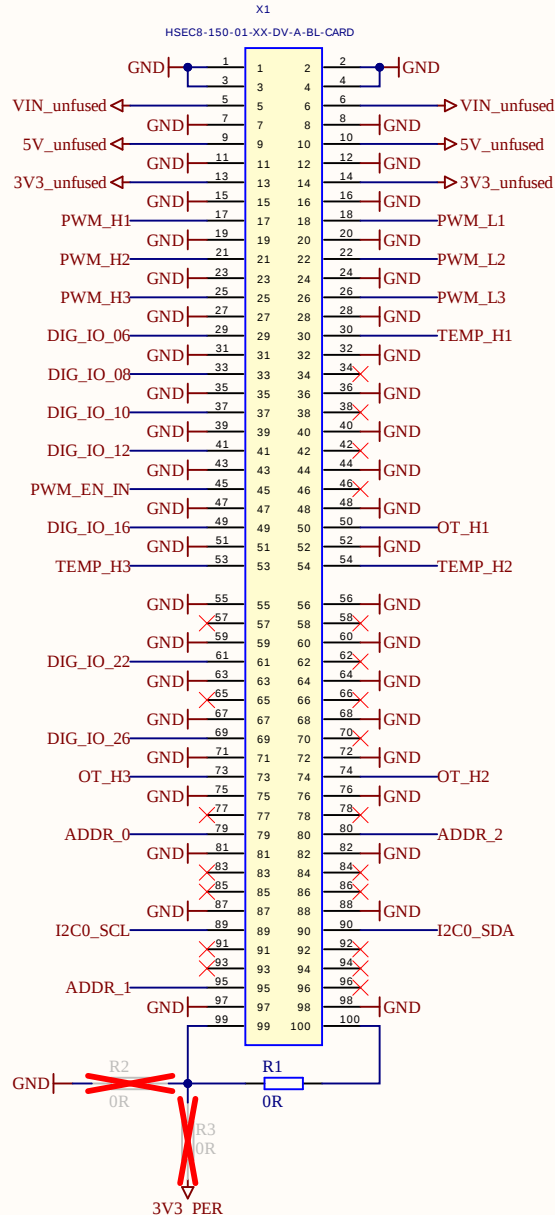
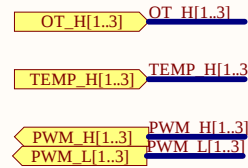
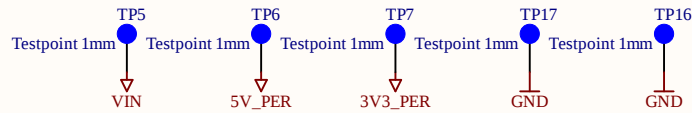
UltraZohm

www.ultrazohm.com

Date: 07.04.2025

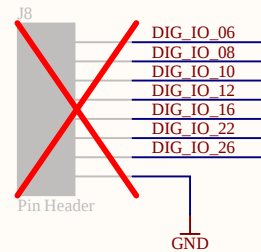
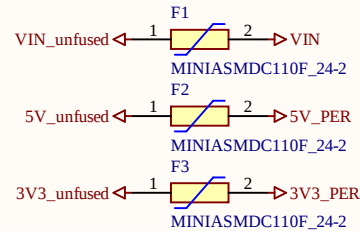
Sheet 1 of 15



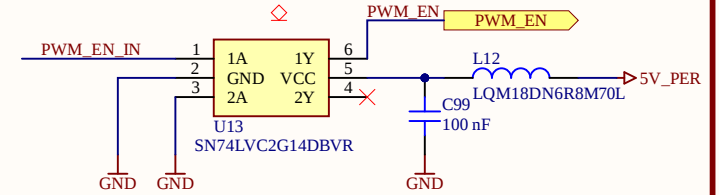


Temp_H/L signals:
Pulswidth modulated signal to the SoC. Pulswidth linear correlated to the temperature of the Mosfets
Frequency 11kHz

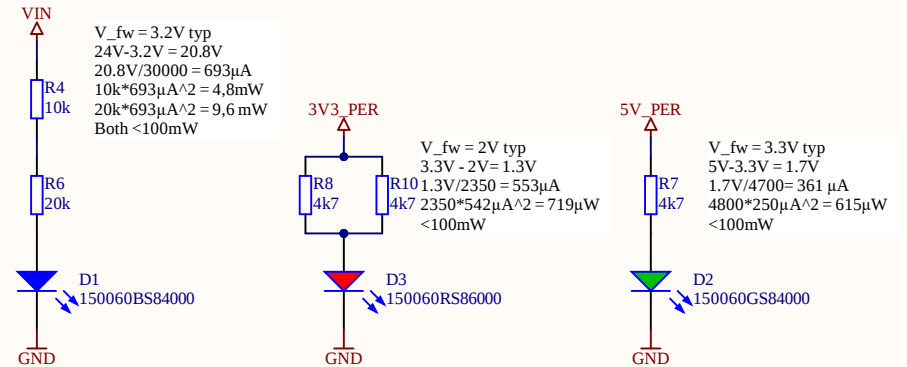
OT_H/L signals:
Active low signal.
When in normal operation, signal is 3V3.
When the measured temp exceeds 105°C, the OT signal will be set to LOW.



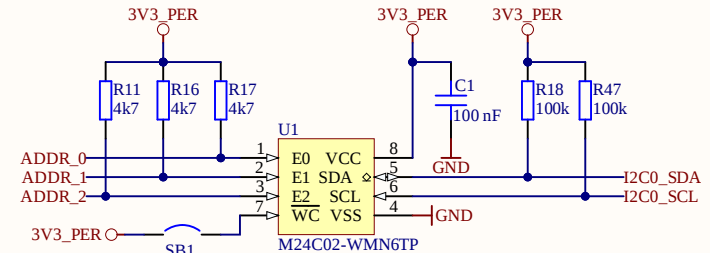
Inverting Schmitt Trigger



Status LEDs for UZ-supply rails



EEPROM



Note: place solder bump to protect EEPROM memory from write access.

Title DigitalCarrierJack.SchDoc

Revision: Rev04 Design Engineer: K.Patel / D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

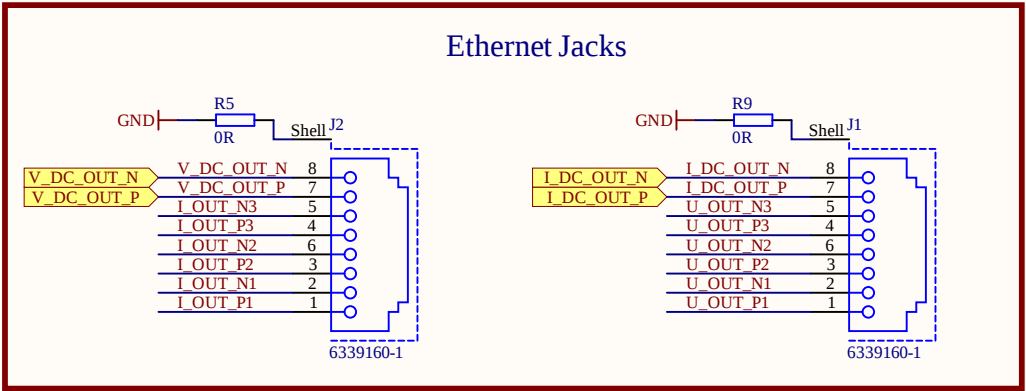
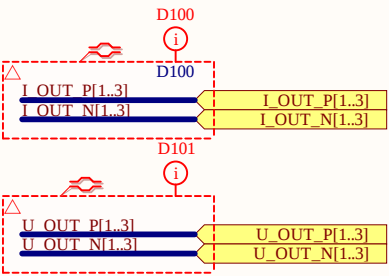
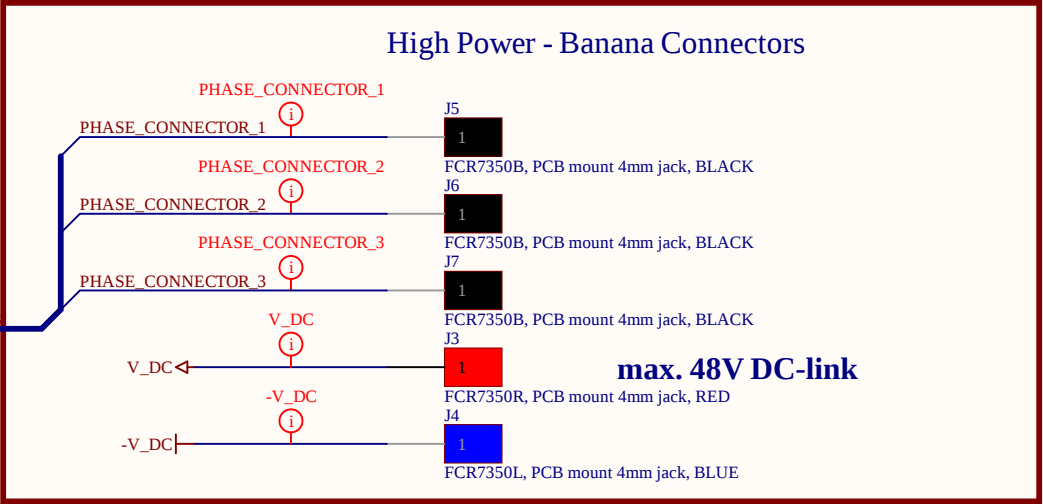
UltraZohm

www.ultrazohm.com

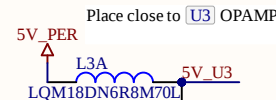
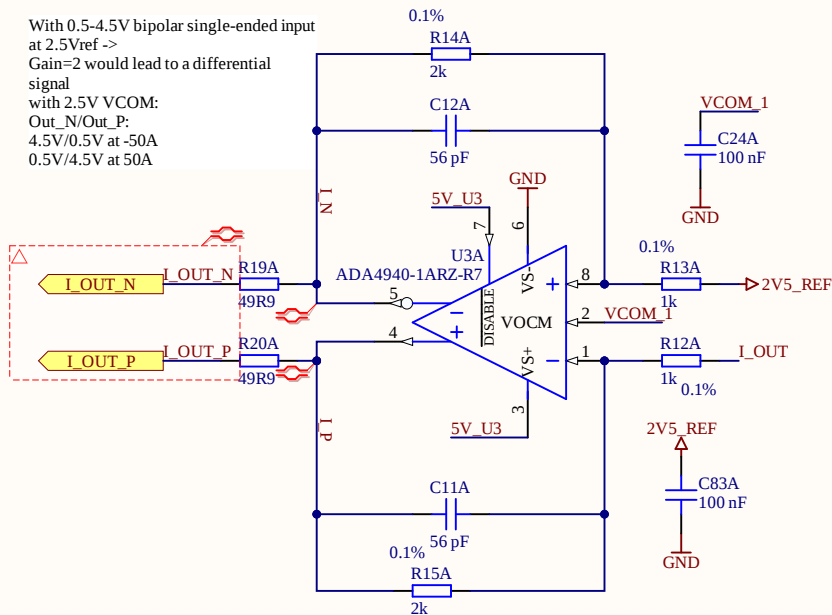
Date: 07.04.2025

Sheet 2 of 15





With 0.5-4.5V bipolar single-ended input at 2.5Vref ->
Gain=2 would lead to a differential signal with 2.5V VCOM:
Out_N/Out_P:
4.5V/0.5V at -50A
0.5V/4.5V at 50A

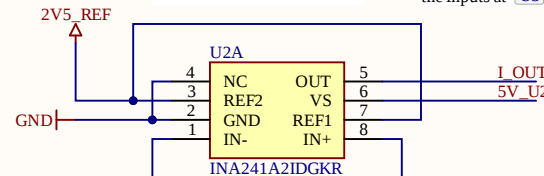


50A max @2mOhm = 1000mV
With fixed 20V/V Gain and 2.5V ref ->
0.5-4.5V bipolar single-ended

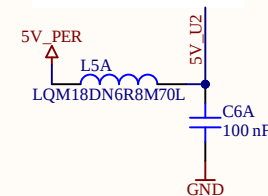
Phase Current Measurement + Single->Diff OPAMP



U2 the terminals IN- and IN+ are connected inverted. This is done to improve the PCB-layout. This is fixed, by inverting the inputs at U3 again.



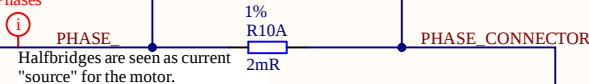
Place close to U2 OPAMP



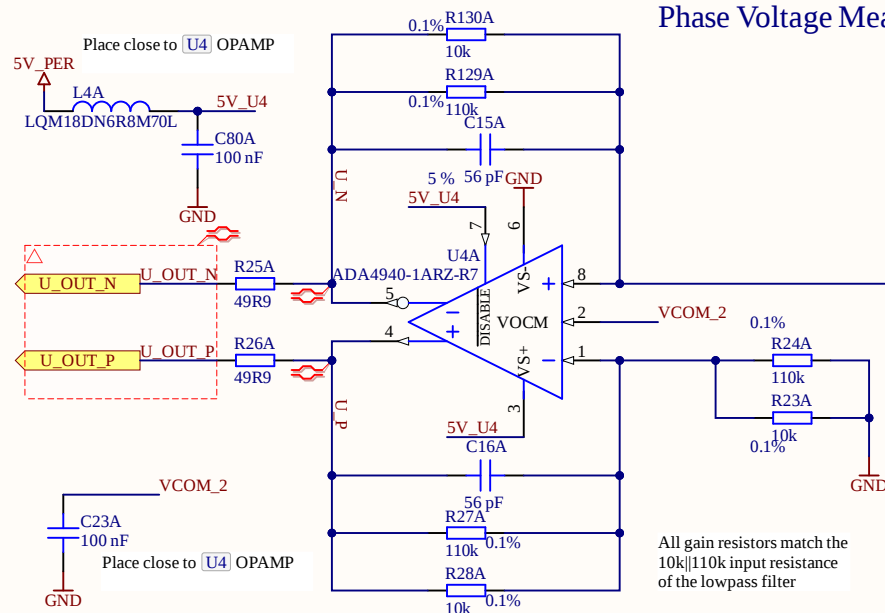
Phases

PHASE

Halfbridges are seen as current "source" for the motor.



Phase Voltage Measurement + Single->Diff OPAMP



Voltage measurement scaled with voltage divider [R22] and [R21]:
Max 48V (LowPass max 60V as buffer)
 $10k \parallel 110k \rightarrow 48V * 10k / (10k + 110k) = 4V$
 $48V / (10k \parallel 110k) = 5.2mA$

Max operation 60V:
 $60V * 10k / (10k + 110k) = 5V$
 $60V / (10k \parallel 110k) = 6.5mA$

PHASE CONNECTOR

Direction towards the connectors and motor

LowPass Filter:
Max Target:
6000rpm at 18 pole pairs
->fg=1800Hz
With LowPass & Feedback
Lowpass. Resulting frequency
response calculated via LTSpice
Simulation ->1.745kHz

All gain resistors match the $10k \parallel 110k$ input resistance of the lowpass filter

Title Phase_Measurements.SchDoc

Revision: Rev04

Design Engineer: K.Patel / D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

UltraZohm

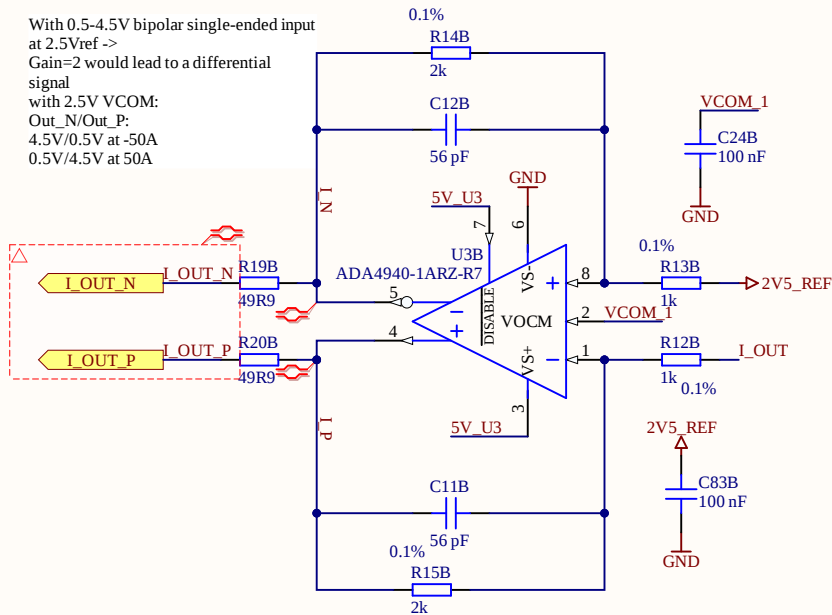
www.ultrazohm.com

Date: 07.04.2025

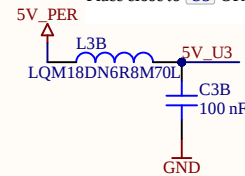
Sheet 4.1 of 15



With 0.5-4.5V bipolar single-ended input at 2.5Vref ->
Gain=2 would lead to a differential signal with 2.5V VCOM:
Out_N/Out_P:
4.5V/0.5V at -50A
0.5V/4.5V at 50A



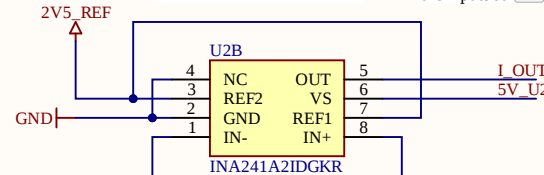
Place close to U3 OPAMP



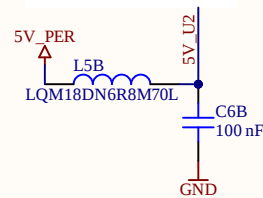
50A max @2mOhm = 1000mV
With fixed 20V/V Gain and 2.5V ref ->
0.5-4.5V bipolar single-ended

Phase Current Measurement + Single->Diff OPAMP

U2 the terminals IN- and IN+ are connected inverted. This is done to improve the PCB-layout. This is fixed, by inverting the inputs at U3 again.



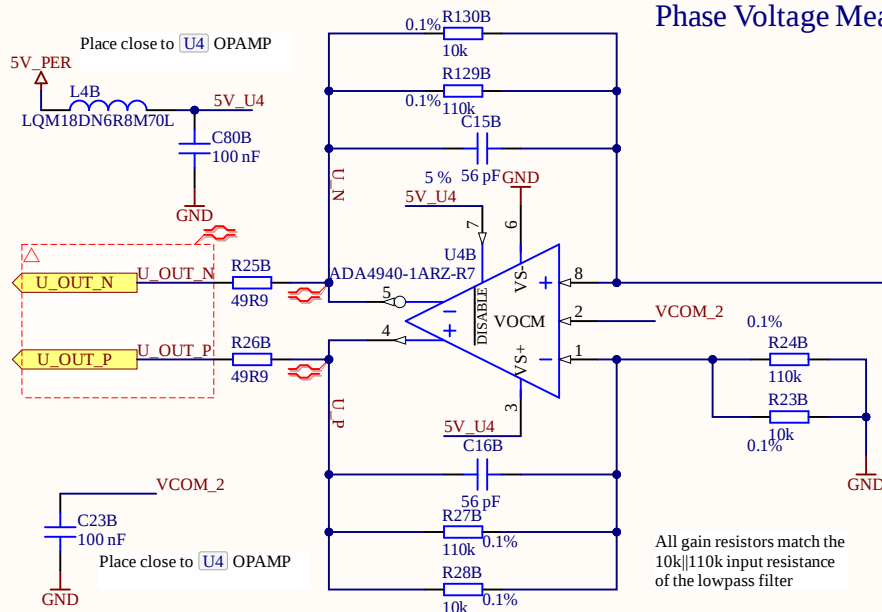
Place close to U2 OPAMP



Phases

PHASE
Halfbridges are seen as current "source" for the motor.

Phase Voltage Measurement + Single->Diff OPAMP



Voltage measurement scaled with voltage divider [R22] and [R21]:
Max 48V (LowPass max 60V as buffer)
 $10k \parallel 110k \rightarrow 48V \cdot 10k / (10k + 110k) = 4V$
 $48V / (10k \parallel 110k) = 5.2mA$

Max operation 60V:
 $60V \cdot 10k / (10k + 110k) = 5V$
 $60V / (10k \parallel 110k) = 6.5mA$

PHASE CONNECTOR

Direction towards the connectors and motor

LowPass Filter:
Max Target:
6000rpm at 18 pole pairs
 $\rightarrow f_g = 1800Hz$
With LowPass & Feedback Lowpass. Resulting frequency response calculated via LTSpice Simulation $\rightarrow 1.745kHz$

All gain resistors match the $10k \parallel 110k$ input resistance of the lowpass filter

Title Phase_Measurements.SchDoc

Revision: Rev04

Design Engineer: K.Patel / D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

UltraZohm

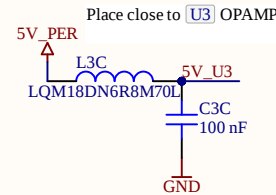
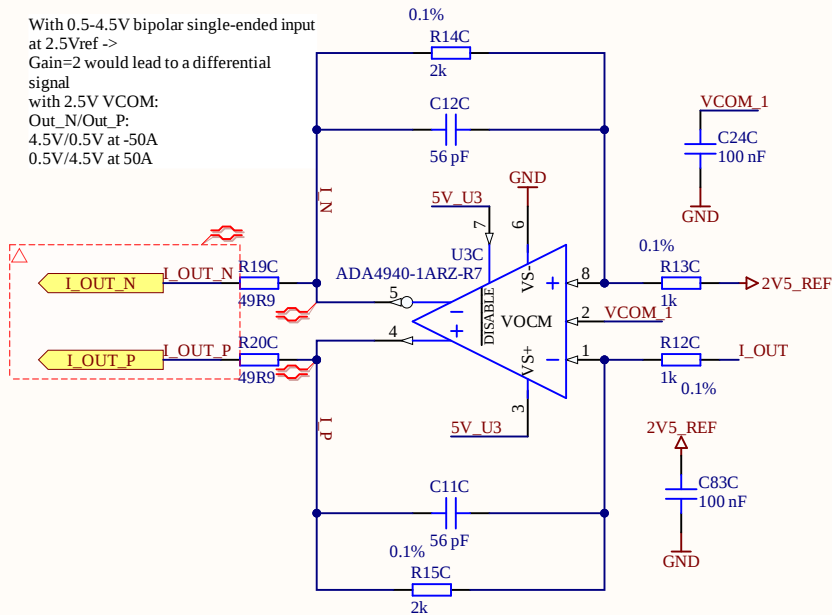
www.ultrazohm.com

Date: 07.04.2025

Sheet 4.2 of 15



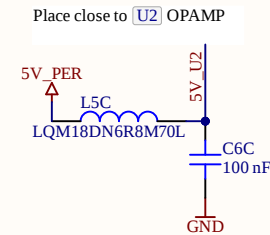
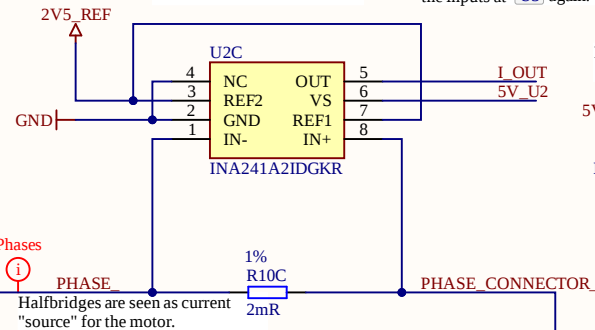
With 0.5-4.5V bipolar single-ended input at 2.5Vref ->
Gain=2 would lead to a differential signal with 2.5V VCOM:
Out_N/Out_P:
4.5V/0.5V at -50A
0.5V/4.5V at 50A



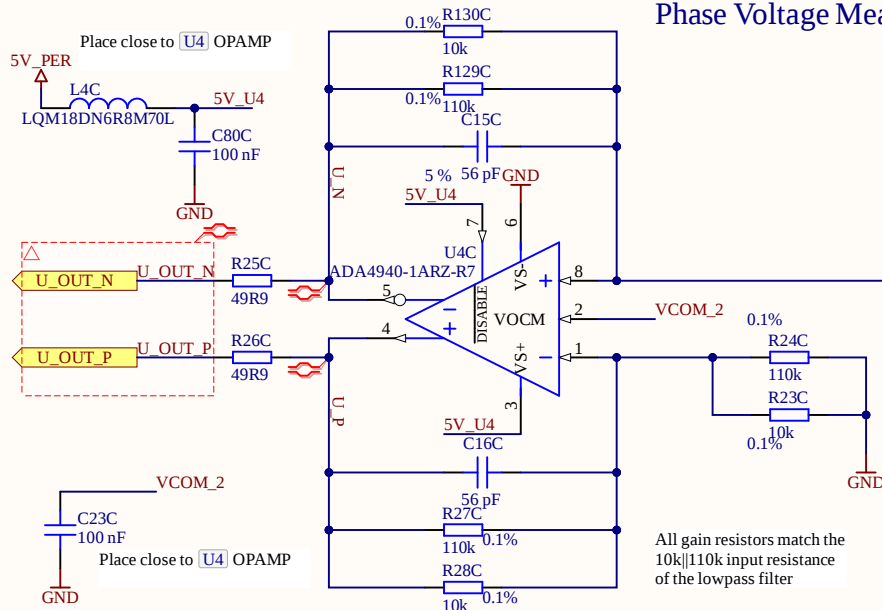
50A max @2mOhm = 1000mV
With fixed 20V/V Gain and 2.5V ref ->
0.5-4.5V bipolar single-ended

Phase Current Measurement + Single->Diff OPAMP

U2 the terminals IN- and IN+ are connected inverted. This is done to improve the PCB-layout. This is fixed, by inverting the inputs at U3 again.



Phase Voltage Measurement + Single->Diff OPAMP



Voltage measurement scaled with voltage divider [R22] and [R21]:
Max 48V (LowPass max 60V as buffer)
 $10k \parallel 110k \rightarrow 48V * 10k / (10k + 110k) = 4V$
 $48V / (10k \parallel 110k) = 5.2mA$
Max operation 60V:
 $60V * 10k / (10k + 110k) = 5V$
 $60V / (10k \parallel 110k) = 6.5mA$

Direction towards the connectors and motor

LowPass Filter:
Max Target:
6000rpm at 18 pole pairs
->fg=1800Hz
With LowPass & Feedback Lowpass. Resulting frequency response calculated via LTSpice Simulation ->1.745kHz

All gain resistors match the $10k \parallel 110k$ input resistance of the lowpass filter

Title Phase_Measurements.SchDoc

Revision: Rev04 Design Engineer: K.Patel / D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

UltraZohm

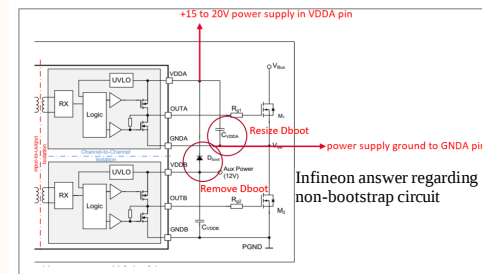
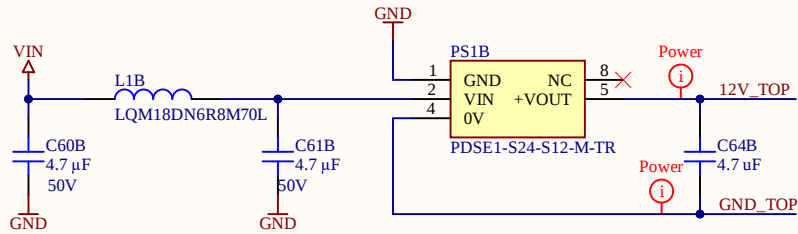
www.ultrazohm.com

Date: 07.04.2025

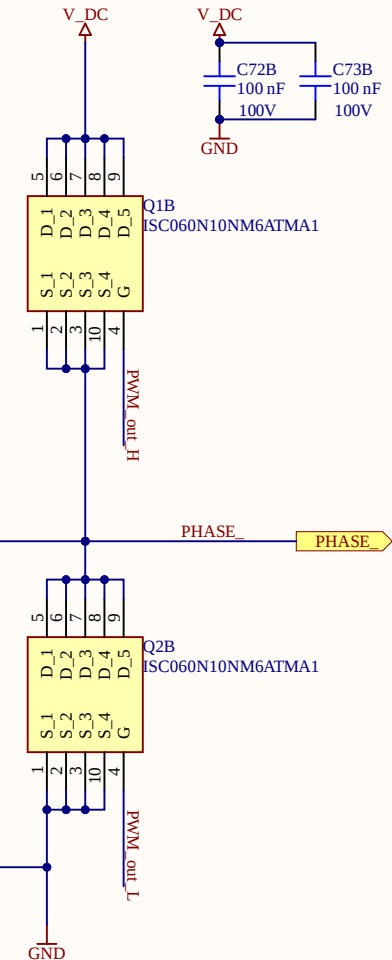
Sheet 4.3 of 15



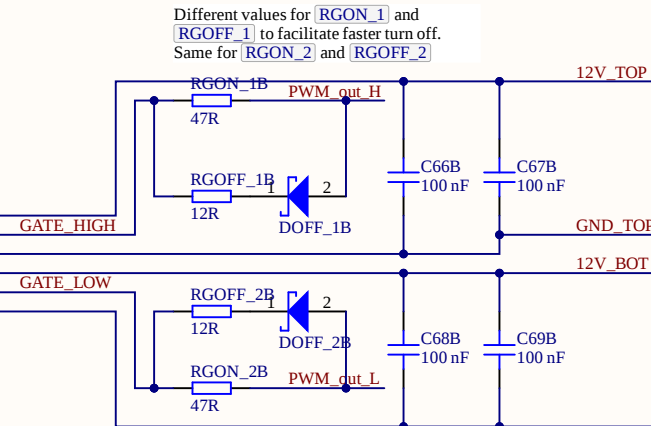
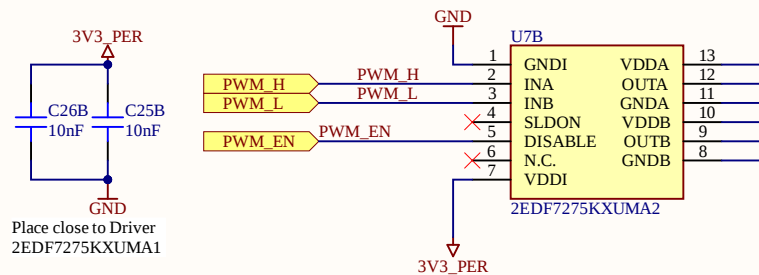
Isolated Top Side Gate Supply



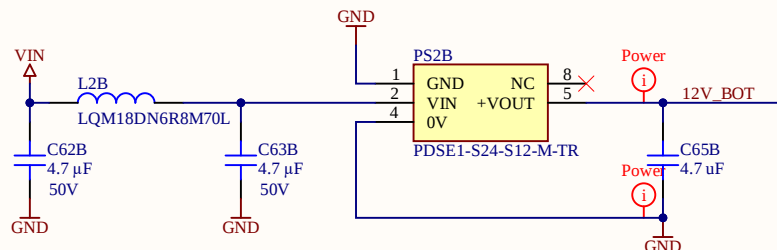
MOSFETS



Gate Driver



Isolated Bottom Side Gate Supply



IG_charging_peak <4A
IG_discharging_peak <8A

->Max currents:
IG_charging = $12V / (47 + 0.42) \text{ Ohm} = 253 \text{ mA}$
IG_discharging = $12V / (12 + 0.18) \text{ Ohm} = 985 \text{ mA}$

Datasheet said minimum
20x CISS for
output-caps:
 $2 \times 100 \text{ nF} > 20 \times 2.5 \text{ nF}$

Title Halfbridges.SchDoc

Revision: Rev04

Design Engineer: K.Patel / D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

UltraZohm

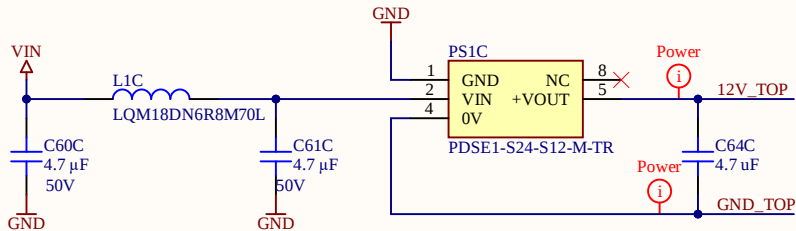
www.ultrazohm.com

Date: 07.04.2025

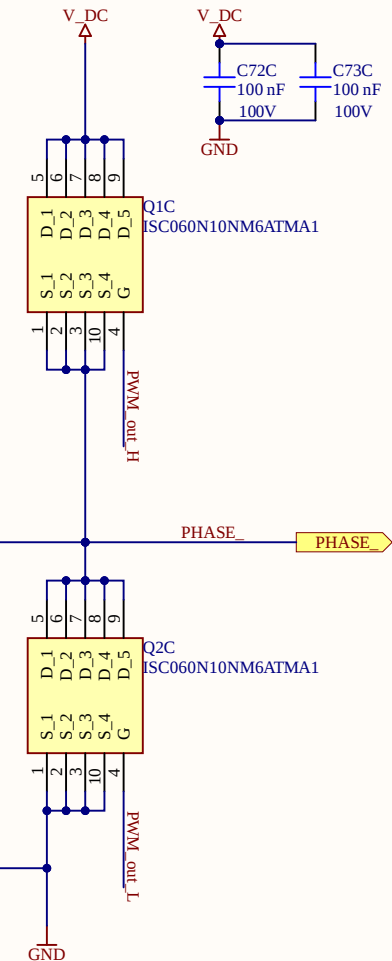
Sheet 5.2 of 15



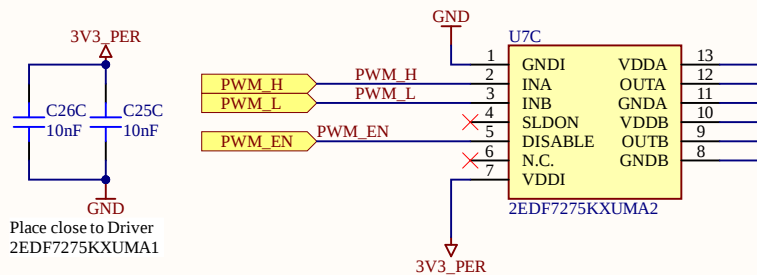
Isolated Top Side Gate Supply



MOSFETS



Gate Driver

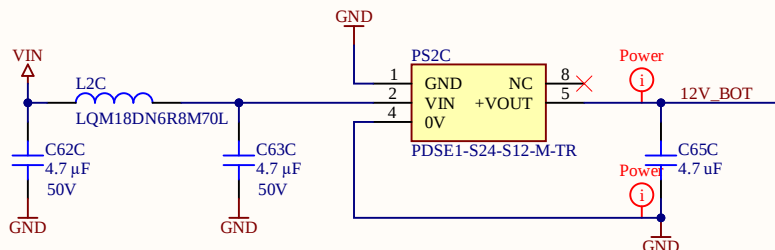


IG_charging_peak <4A
IG_discharging_peak <8A

-> Max currents:
IG_charging = $12V / (47 + 0.42) \Omega = 253mA$
IG_discharging = $12V / (12 + 0.18) \Omega = 985mA$

Datasheet said minimum
20x CISS for
output-caps:
 $2 \times 100nF > 20 \times 2.5nF$

Isolated Bottom Side Gate Supply



Title Halfbridges.SchDoc

Revision: Rev04 Design Engineer: K.Patel / D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

UltraZohm

www.ultrazohm.com

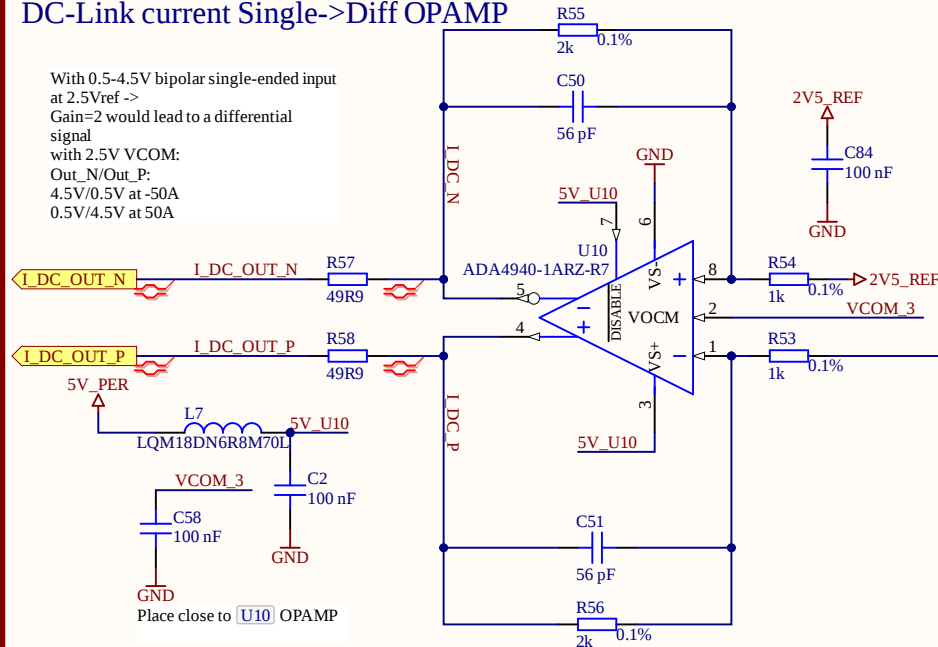
Date: 07.04.2025

Sheet 5.3 of 15



DC-Link current Single->Diff OPAMP

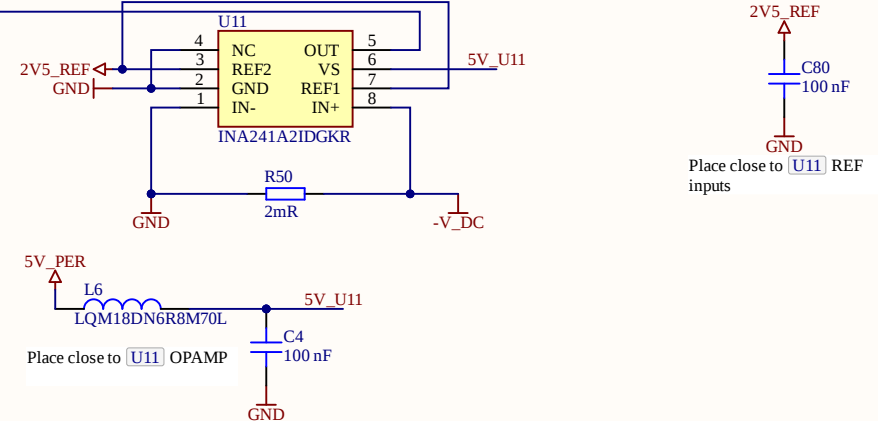
With 0.5-4.5V bipolar single-ended input at 2.5Vref ->
Gain=2 would lead to a differential signal with 2.5V VCOM:
Out_N/Out_P:
4.5V/0.5V at -50A
0.5V/4.5V at 50A



50A max @2mOhm =
1000mV
With fixed 20V/V Gain and
2.5V ref ->
0.5- 4.5V bipolar
single-ended

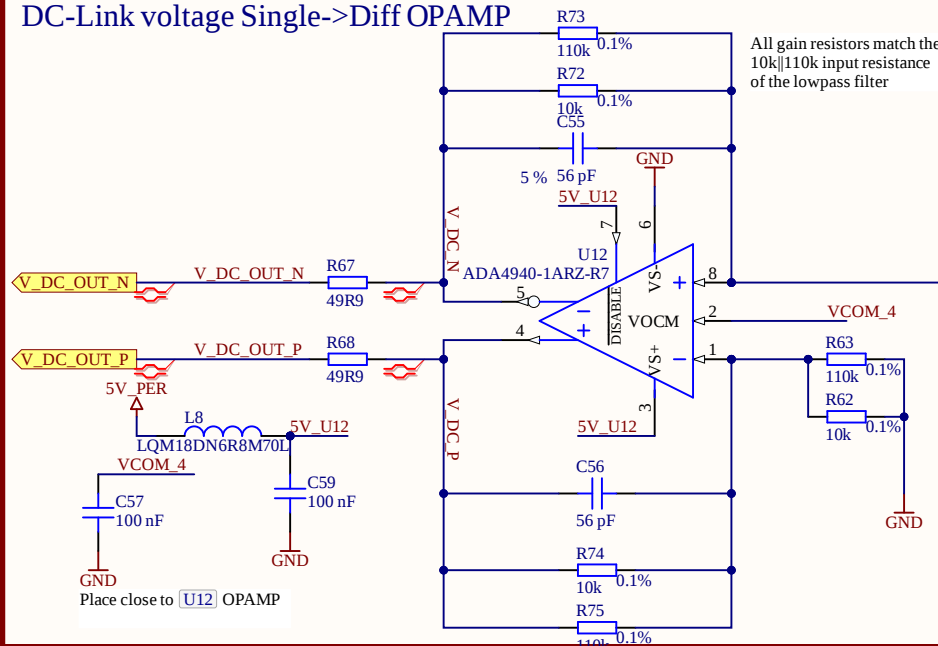
U11 the terminals IN- and IN+ are connected inverted. This is done to improve the PCB-layout. This is fixed, by inverting the inputs at U10 again.

DC-Link current measurement



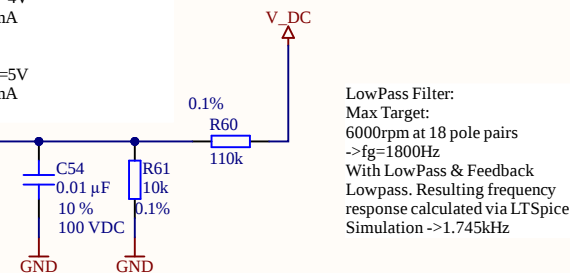
DC-Link voltage Single->Diff OPAMP

All gain resistors match the 10k||110k input resistance of the lowpass filter



Voltage measurement scaled with voltage divider [R60] and [R61]:
Max 48V (LowPass max 60V as buffer)
10k||110k->
 $48V * 10k / (10k + 110k) = 4V$
 $48V / (10k || 110k) = 5.2mA$
Max operation 60V:
 $60V * 10k / (10k + 110k) = 5V$
 $60V / (10k || 110k) = 6.5mA$

DC-Link Voltage lowpass



LowPass Filter:
Max Target:
6000rpm at 18 pole pairs
->fg=1800Hz
With LowPass & Feedback
Lowpass. Resulting frequency
response calculated via LTSpice
Simulation ->1.745kHz

Title DC-link.SchDoc

Revision: Rev04

Design Engineer: K.Patel / D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

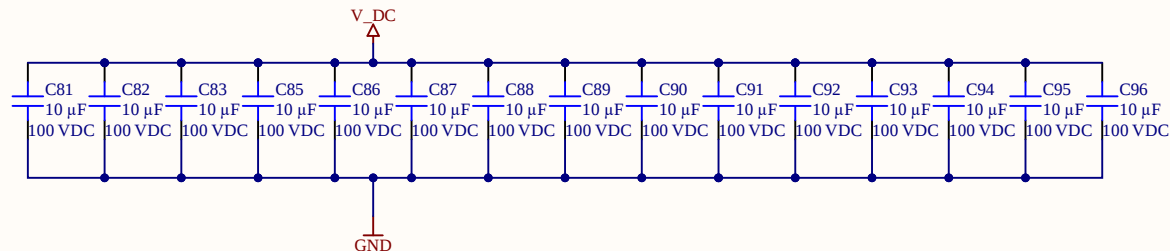
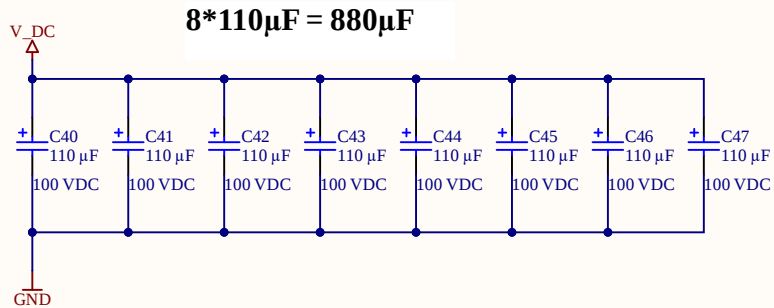
UltraZohm

www.ultrazohm.com

Date: 07.04.2025

Sheet 6 of 15





Additional MLCC caps with low internal R
 $15 \times 10\mu\text{F} = 150\mu\text{F}$

Total DC-Link capacitance
 $880\mu\text{F} + 150\mu\text{F} = 1030\mu\text{F}$

Title DC-Link-Caps.SchDoc

Revision: Rev04

Design Engineer: K.Patel / D. Hufnagel

Project: UZ_D_Inverter.PrjPCB

UltraZohm

www.ultrazohm.com

Date: 07.04.2025

Sheet 7 of 15



4



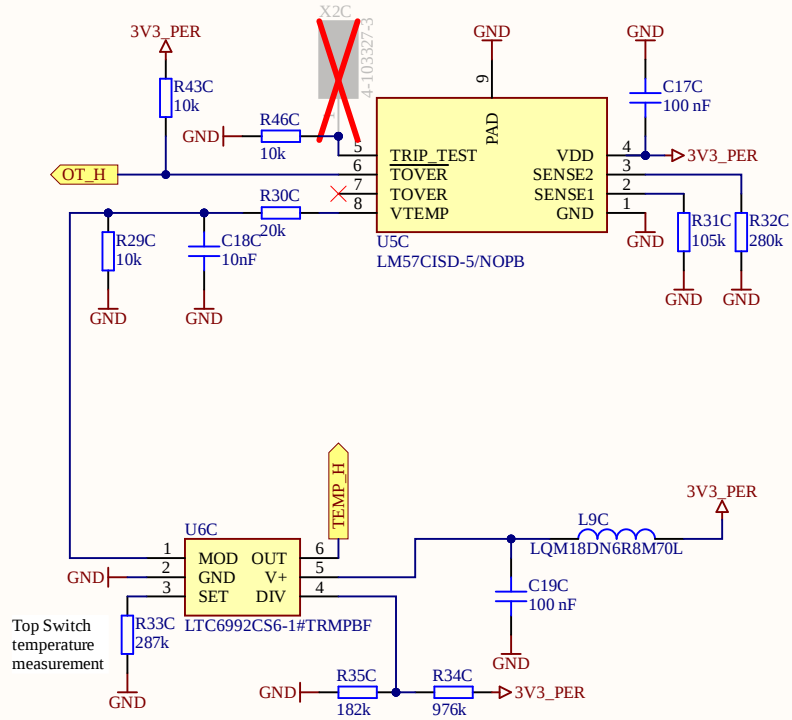
4

4



4

Top MOSFET Temp Measurement

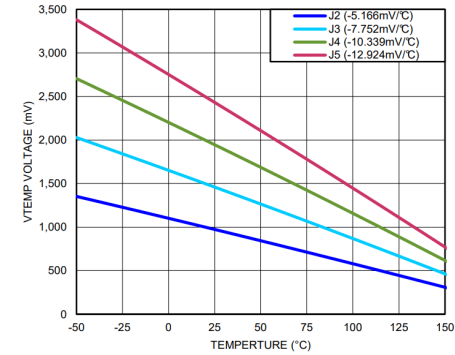


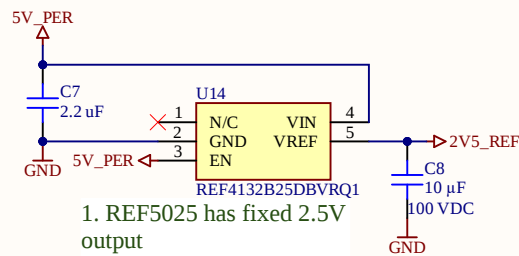
R_SENSE1 (R31) = 105k
R_SENSE2 (R32) = 280k is Gain
->I4 ->Leads to:
1.11V@105°C
2.00V@20°C

/TOVER trips at 105°C

VTEMP has voltage divider with 20k/10k:
MOD input voltages->
 $1.11V * 10/(10+20) = 0.37V @ 105^{\circ}C$
 $2.00V * 10/(10+20) = 0.67V @ 20^{\circ}C$

MOD input should be between 0.14V and 0.9V





- 1. REF5025 has fixed 2.5V output
- 2. Max output current is 10mA

12.1 Layout Guidelines

Figure 31 illustrates an example of a PCB layout for a data acquisition system using the REF4132-Q1. Some key considerations are:

- Connect low-ESR, 0.1-μF ceramic bypass capacitors at V_{IN} , V_{REF} of the REF4132-Q1.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

12.2 Layout Example

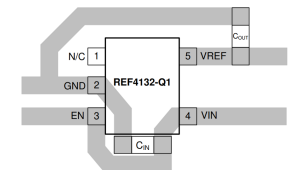


Figure 31. Layout Example

10.2.1 Design Requirements

A detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Example Parameters	
DESIGN PARAMETER	VALUE
Input voltage V_{IN}	5 V
Output voltage V_{OUT}	2.5 V
REF4132-Q1 input capacitor	1 μ F
REF4132-Q1 output capacitor	10 μ F