

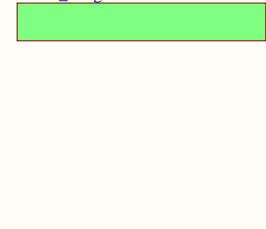
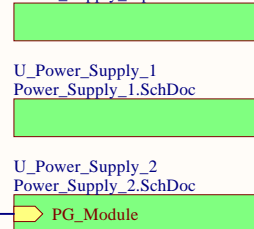
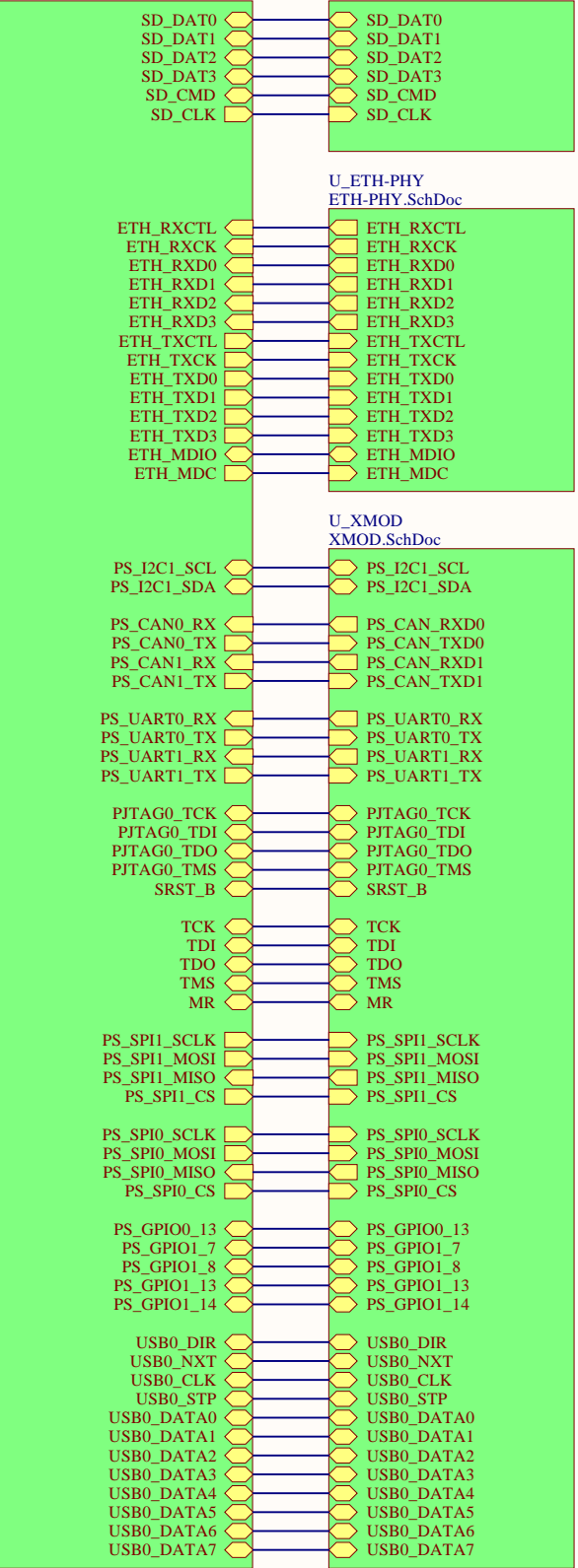
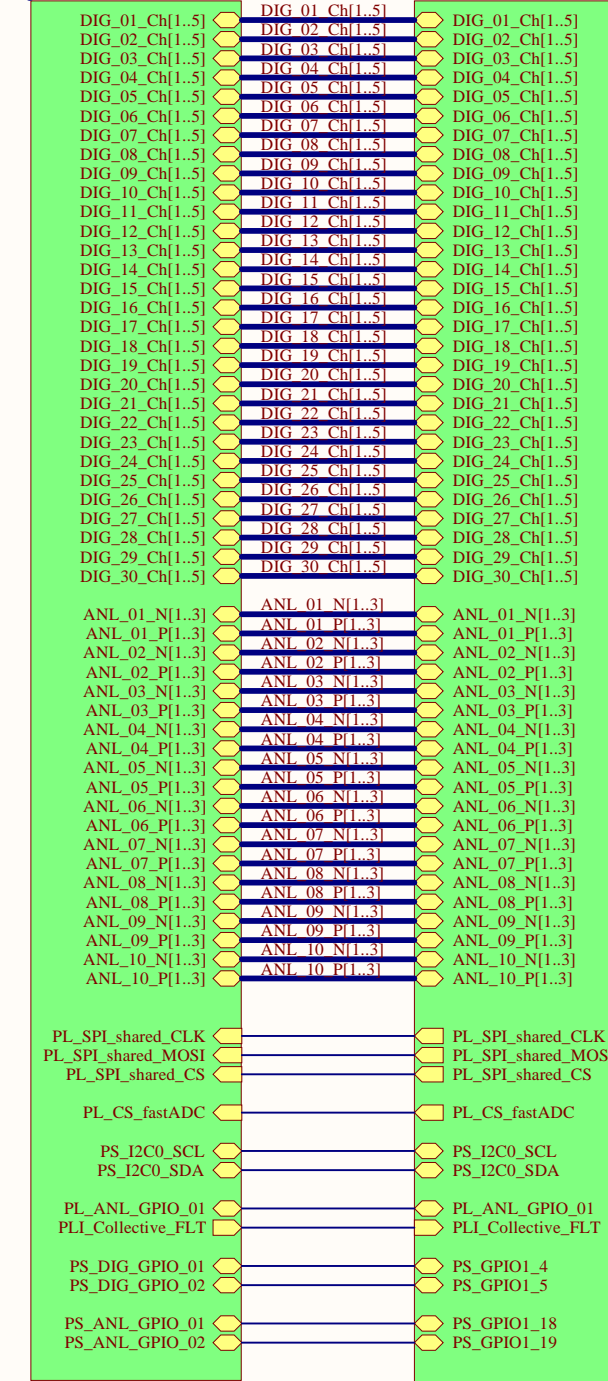
U_Signal_Distribution
Signal_Distribution.SchDoc

U_Board2Board
Board2Board.SchDoc


U_SD_Card
SD_Card.SchDoc


U_Power_Supply_Input
Power_Supply_Input.SchDoc

U_Block_Diagram
Block_Diagram.SchDoc




design information, revision number, ...


PCB_Logo  SerialI
Serial
Serialnumber 6,3 x 6.3mm

 Project Logo

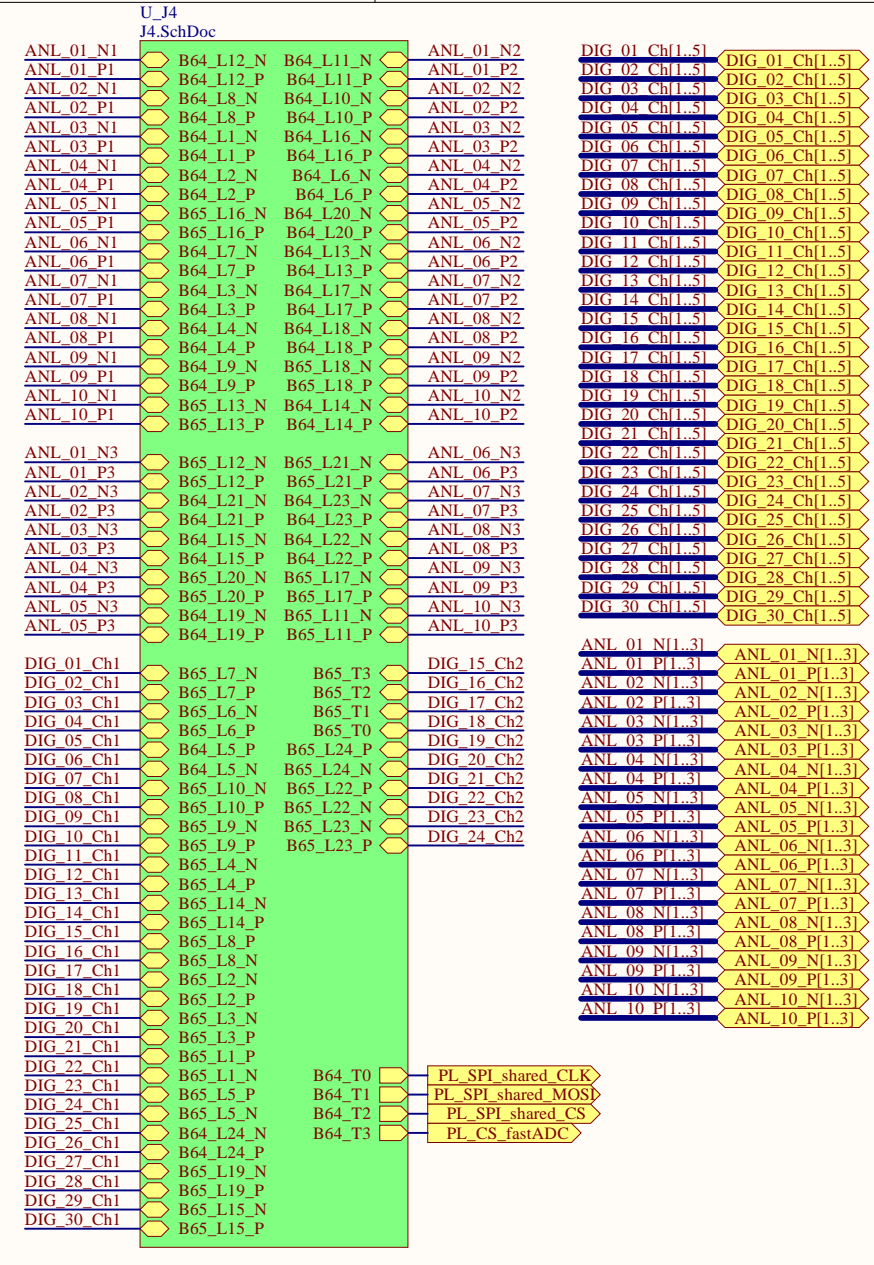
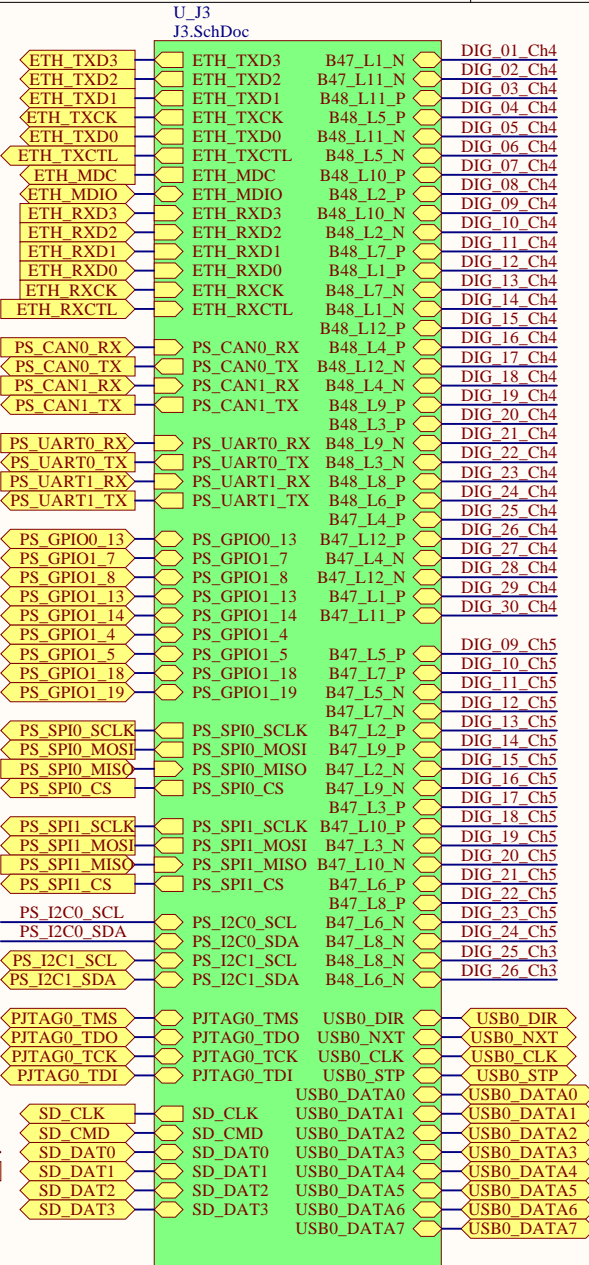
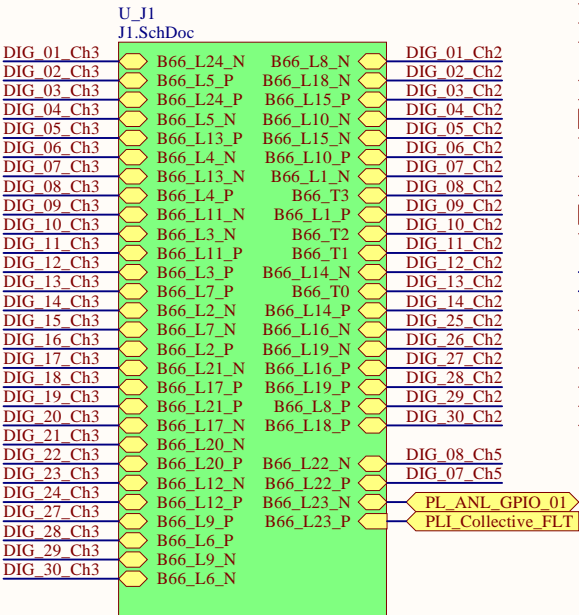
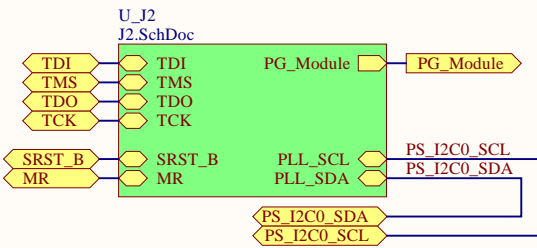
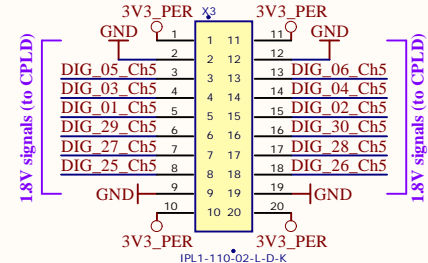
mounting holes for M3 screws

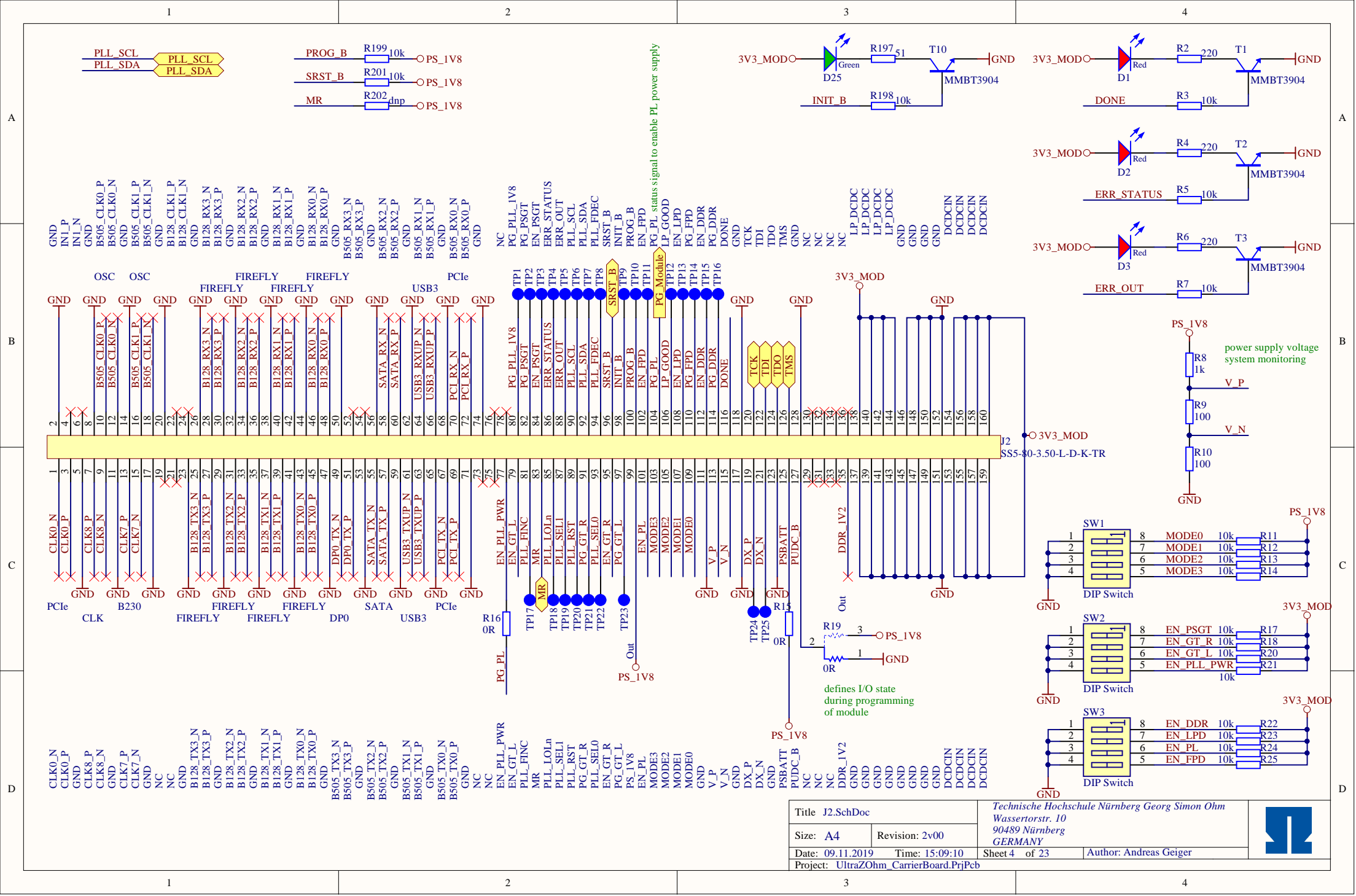


MH1 MH2 MH3
MH4 MH5 MH6

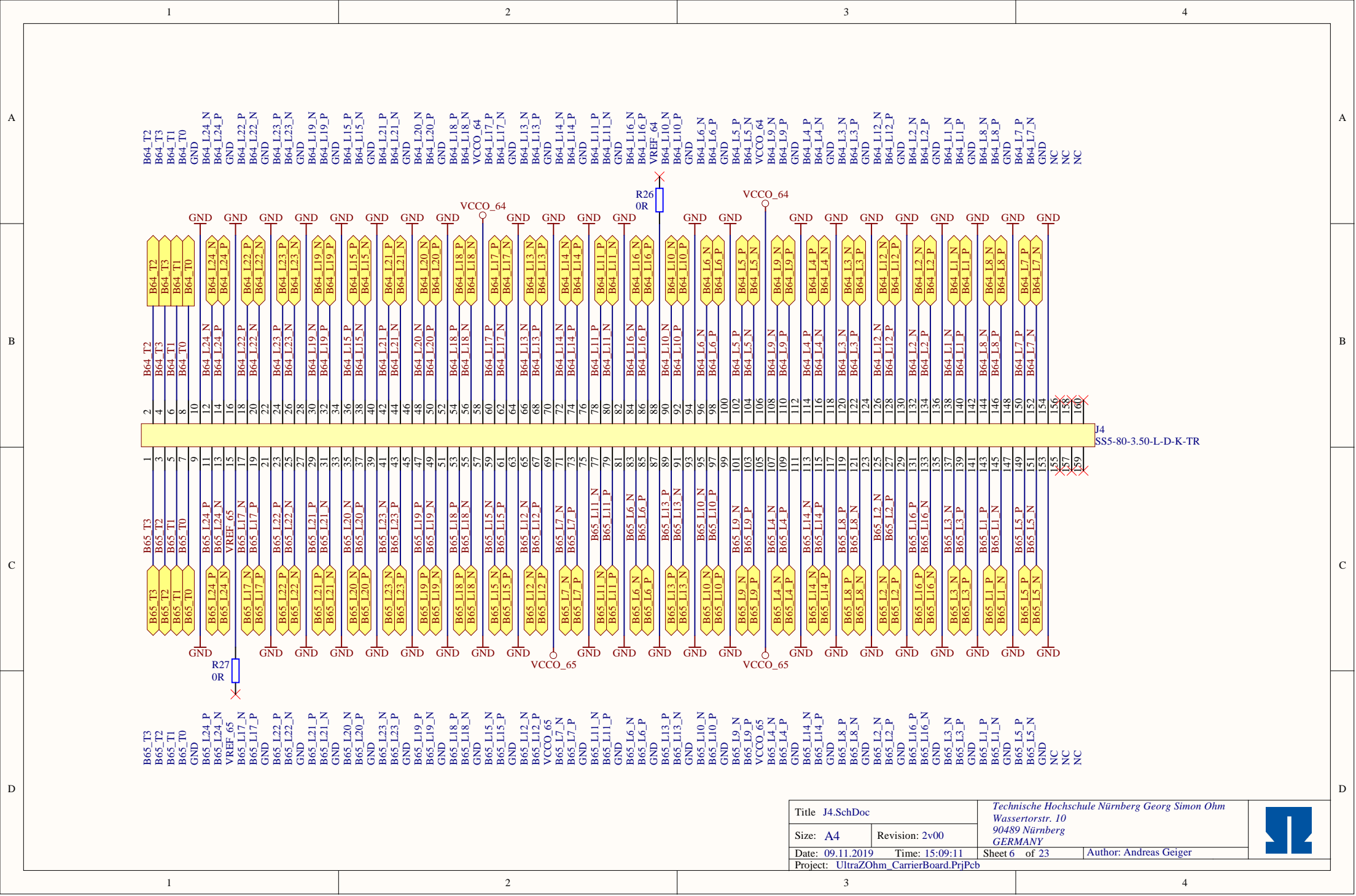
Title CarrierBoard_TopSheet.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY		
Size: A4	Revision: 2v00	Date: 09.11.2019	Time: 15:09:10	
Project: UltraZOhm_CarrierBoard.PrjPcb		Sheet 1 of 23	Author: Andreas Geiger	

The 5th digital socket is not full connected with FPGA pins. DIG_01...DIG06 and DIG_25...DIG_30 of this socket can be used externally via this connector.





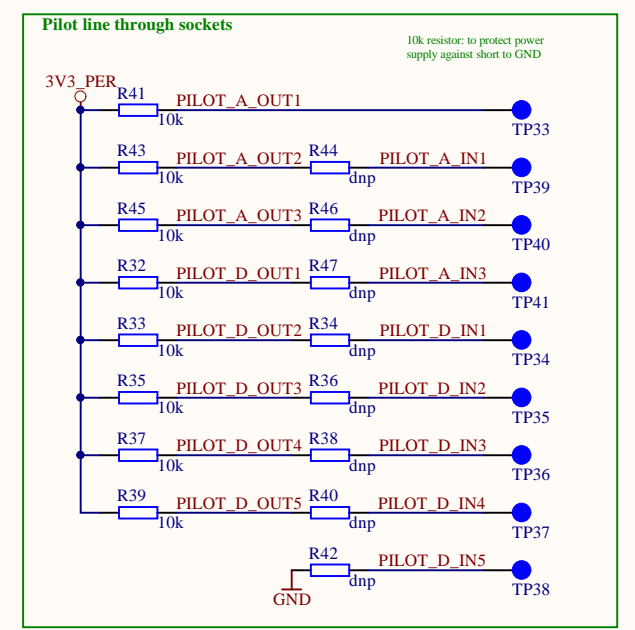
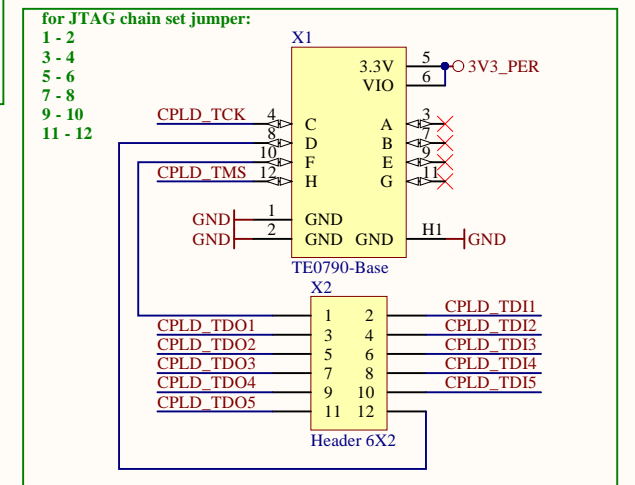
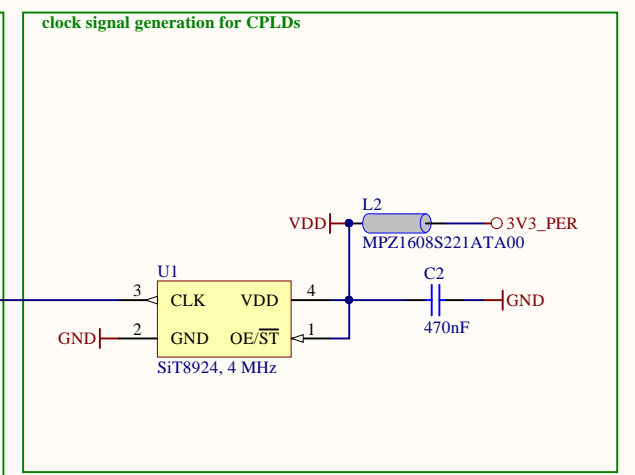
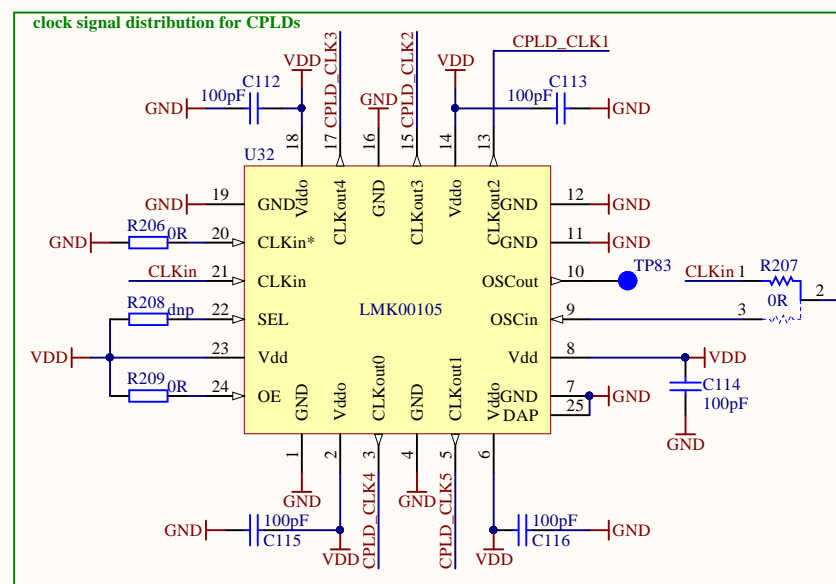
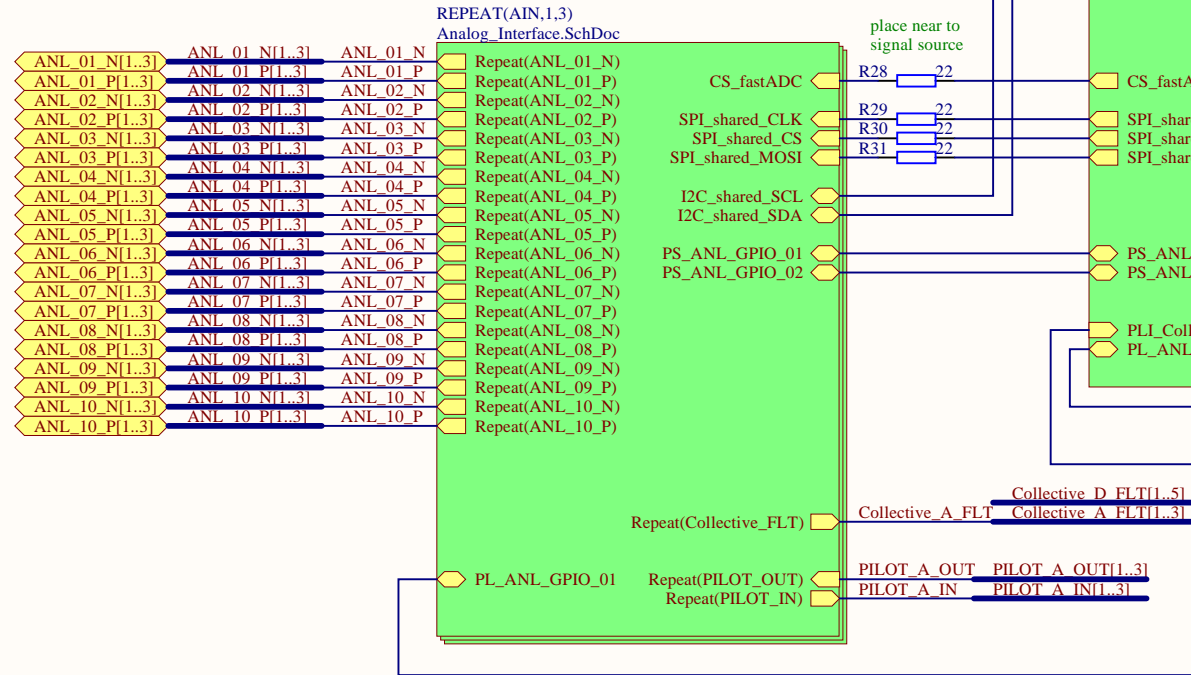
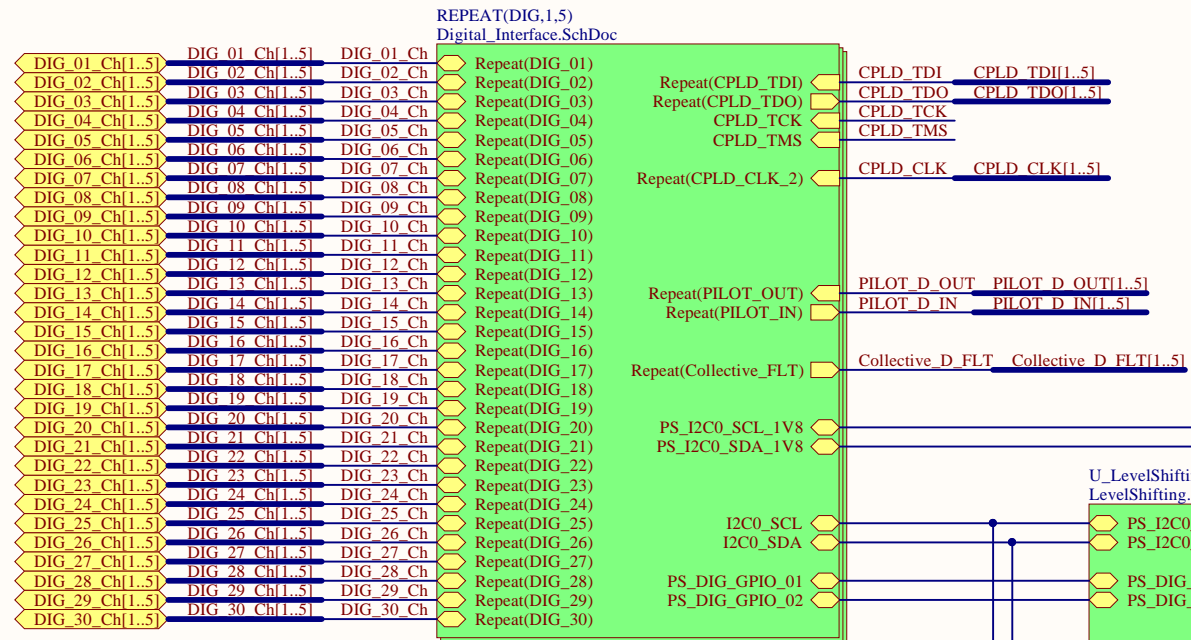
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Size: A4	Revision: 2v00			
Date: 09.11.2019	Time: 15:09:10	Sheet 4 of 23	Author: Andreas Geiger	
Project: UltraZOhm_CarrierBoard.PrjPcb				



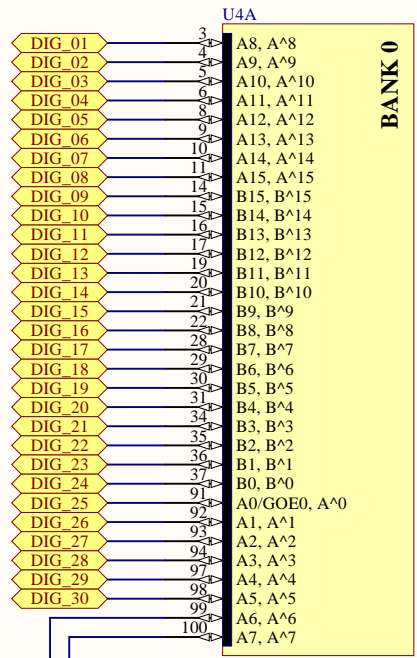
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 B65_T2
 B65_T1
 B65_T0
 GND
 B65_L24_P
 B65_L24_N
 VREF_65
 B65_L17_N
 B65_L17_P
 GND
 B65_L22_P
 B65_L22_N
 GND
 B65_L21_P
 B65_L21_N
 GND
 B65_L20_N
 B65_L20_P
 GND
 B65_L23_N
 B65_L23_P
 GND
 B65_L19_P
 B65_L19_N
 GND
 B65_L18_P
 B65_L18_N
 GND
 B65_L15_N
 B65_L15_P
 GND
 B65_L12_N
 B65_L12_P
 VCCO_65
 B65_L7_N
 B65_L7_P
 GND
 B65_L11_N
 B65_L11_P
 GND
 B65_L6_N
 B65_L6_P
 GND
 B65_L13_P
 B65_L13_N
 GND
 B65_L10_N
 B65_L10_P
 GND
 B65_L9_N
 B65_L9_P
 VCCO_65
 B65_L4_P
 B65_L4_N
 GND
 B65_L14_N
 B65_L14_P
 GND
 B65_L8_P
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 B65_L16_N
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 B65_L3_P
 GND
 B65_L1_P
 B65_L1_N
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 B65_L5_P
 B65_L5_N
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 NC
 NC
 NC
 B64_T2
 B64_T3
 B64_T1
 B64_T0
 GND
 B64_L24_N
 B64_L24_P
 GND
 B64_L22_P
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 GND
 B64_L7_P
 B64_L7_N
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 NC
 NC
 NC

Title J4.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm	
Size: A4		Wassertorstr. 10	
Revision: 2v00		90489 Nürnberg	
Date: 09.11.2019		GERMANY	
Time: 15:09:11		Sheet 6 of 23	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			

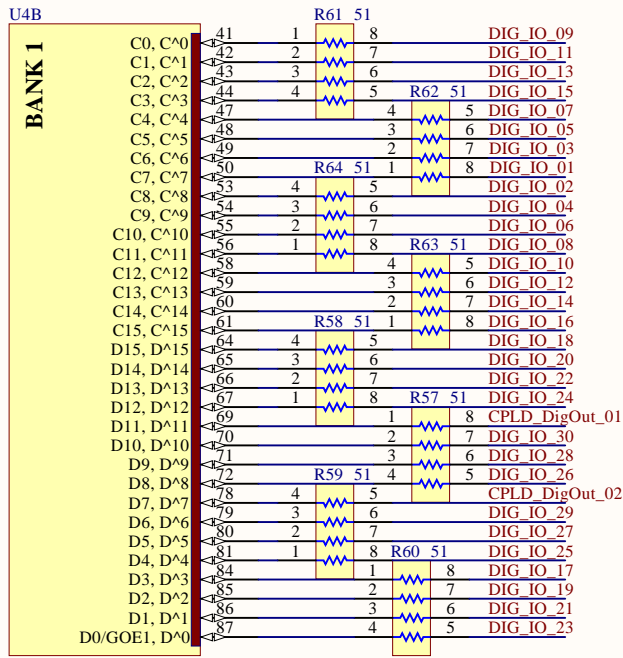




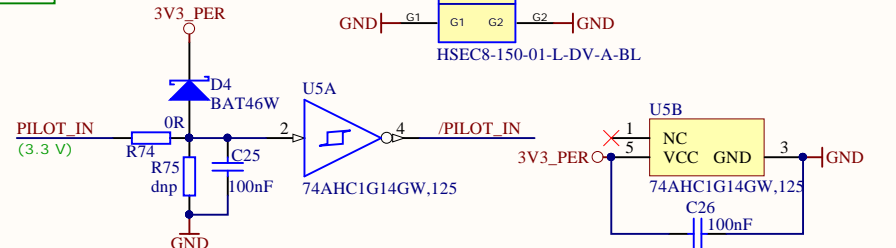
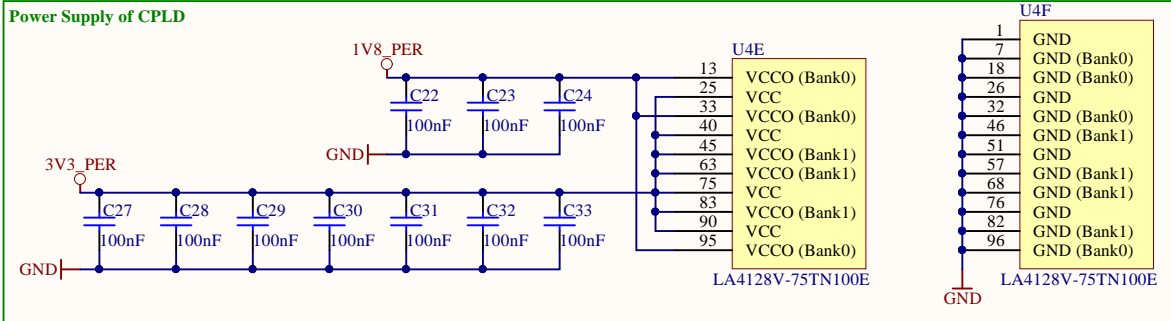
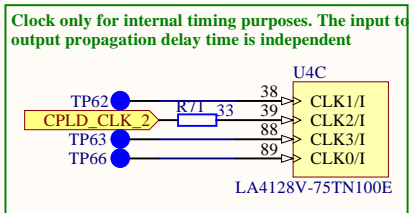
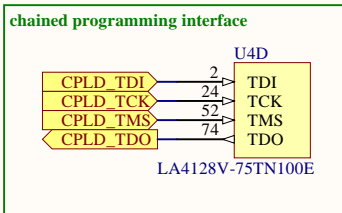
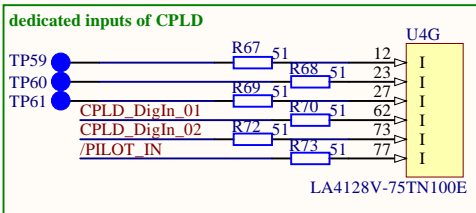
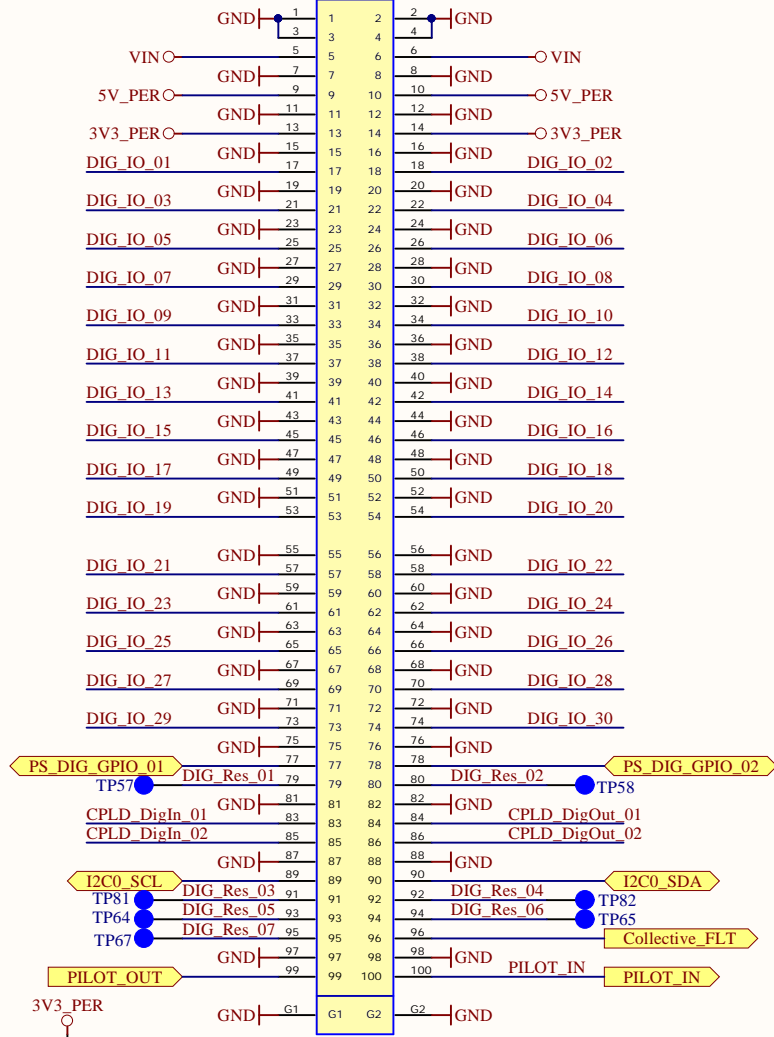
BANK 0 @ 1.8V



BANK 1 @ 3.3V



X6



Title Digital_Interface.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm	
Size: A4		Wassertorstr. 10	
Revision: 2v00		90489 Nürnberg	
Date: 09.11.2019		GERMANY	
Time: 15:09:11		Author: Andreas Geiger	
Project: UltraZOhm_CarrierBoard.PrjPcb		Sheet 8 of 23	

A

A

B

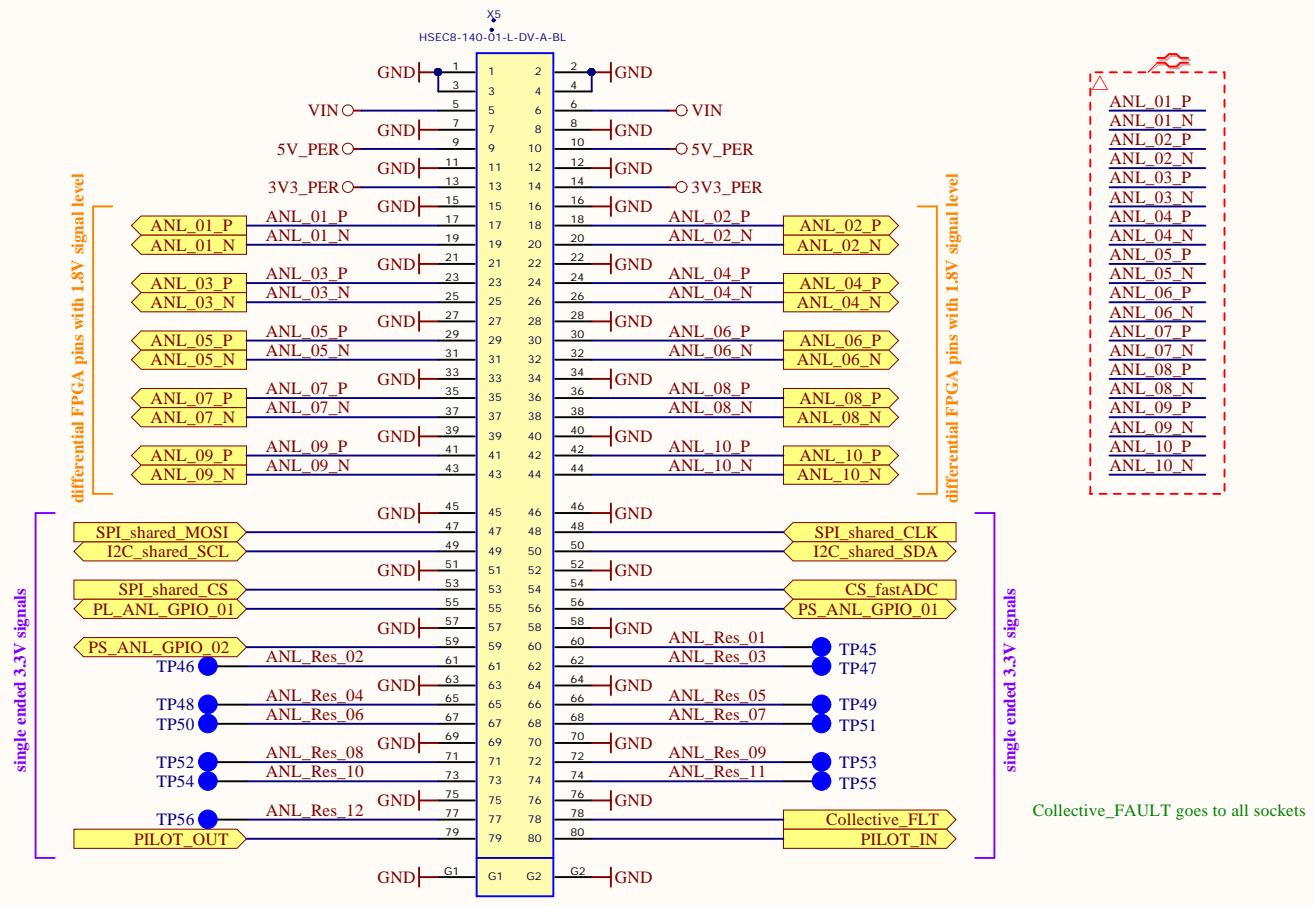
B

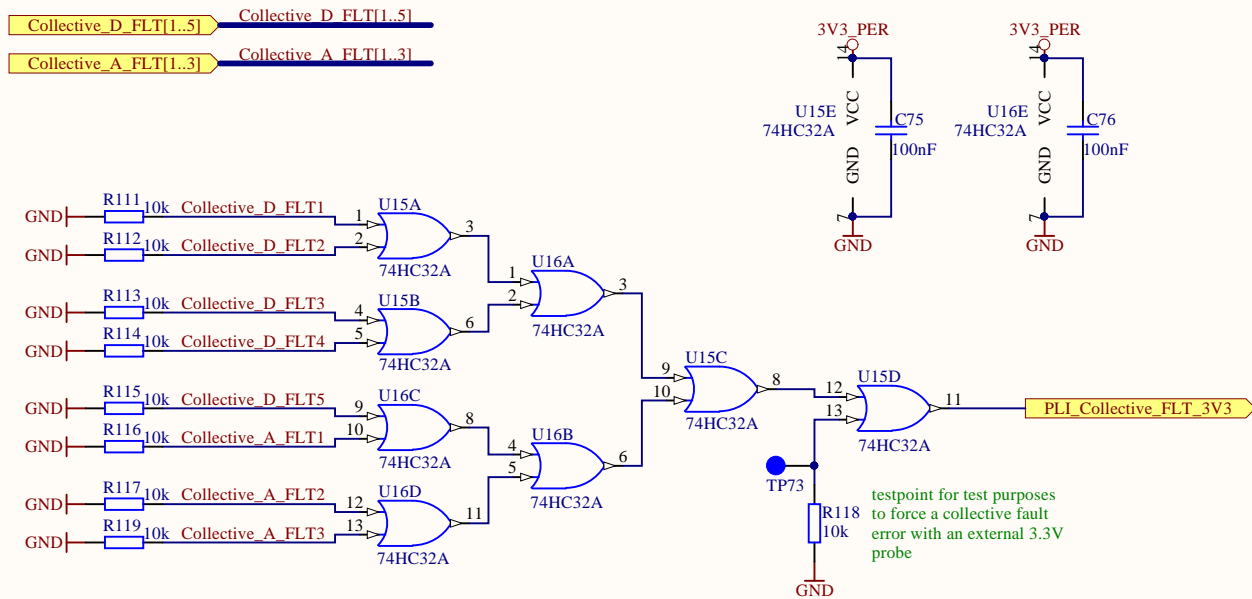
C

C

D

D

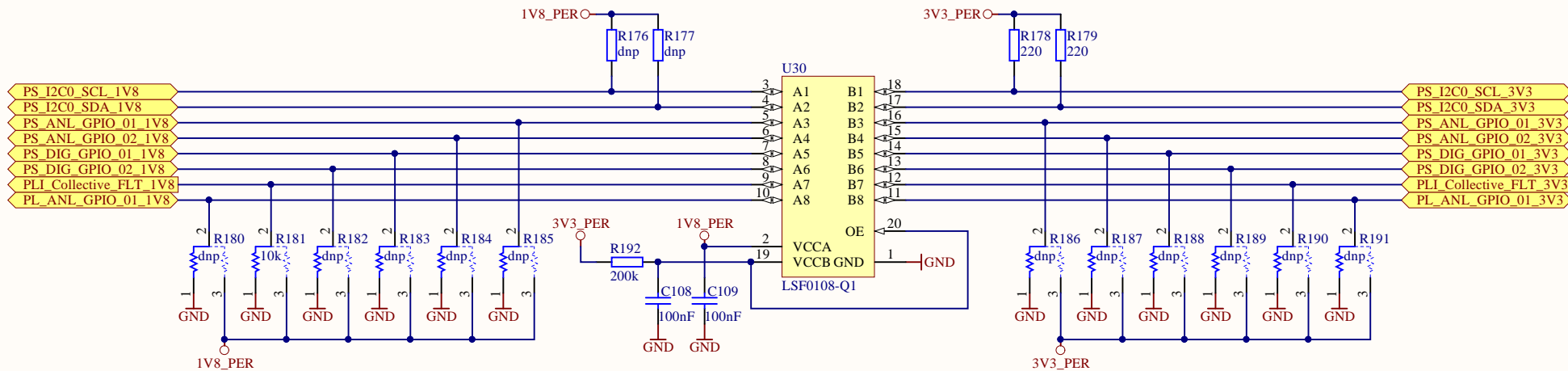




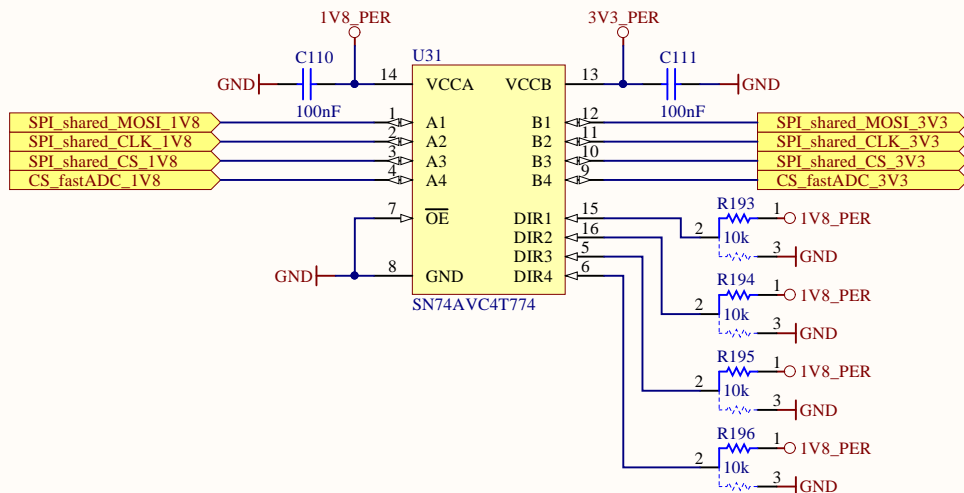
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Size: A4	Revision: 2v00		
Date: 09.11.2019	Time: 15:09:12	Sheet 10 of 23	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			



Bidirectional Level Shifting 1.8V to 3.3V

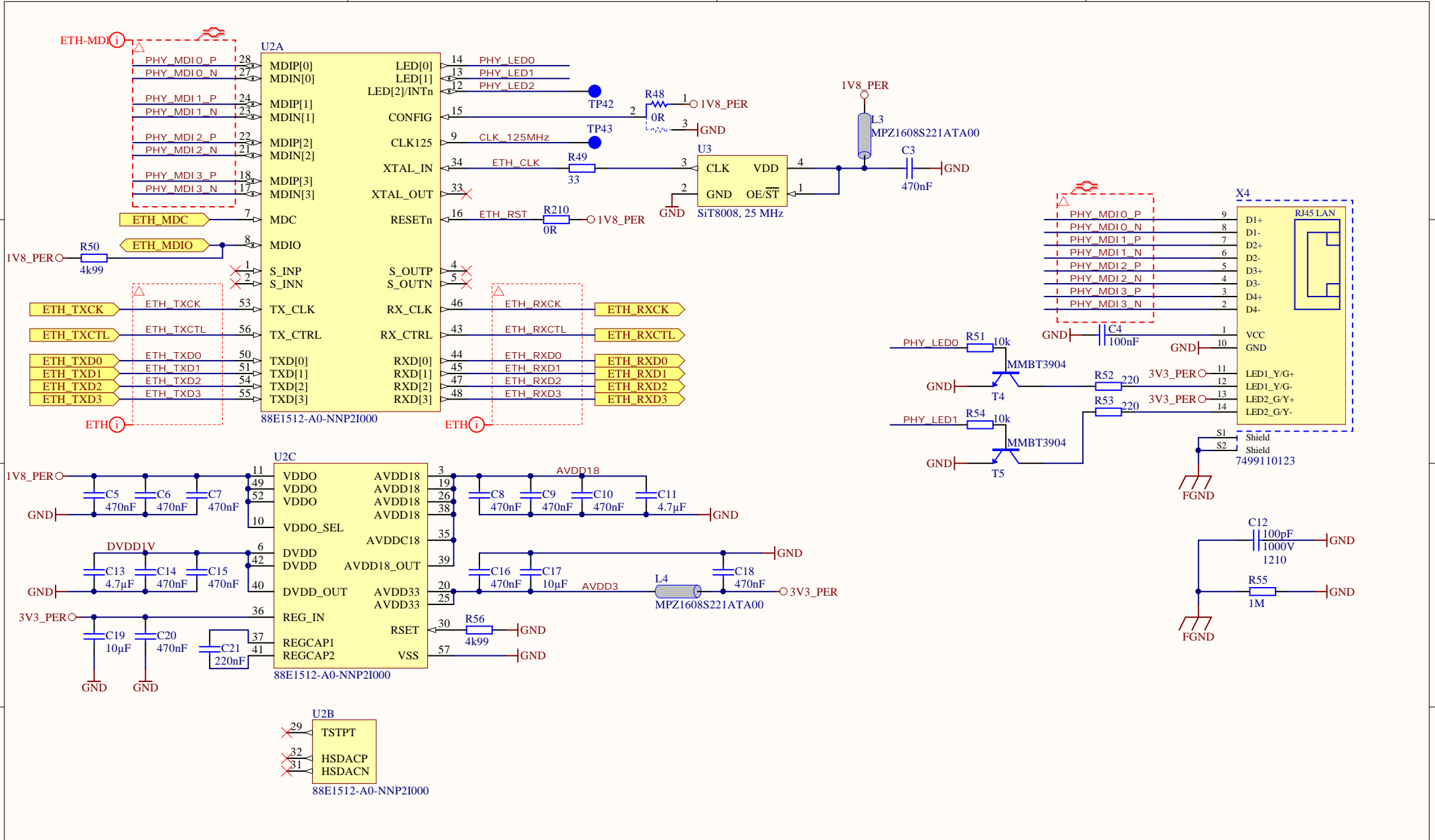


Level Shifting 1.8V to 3.3V

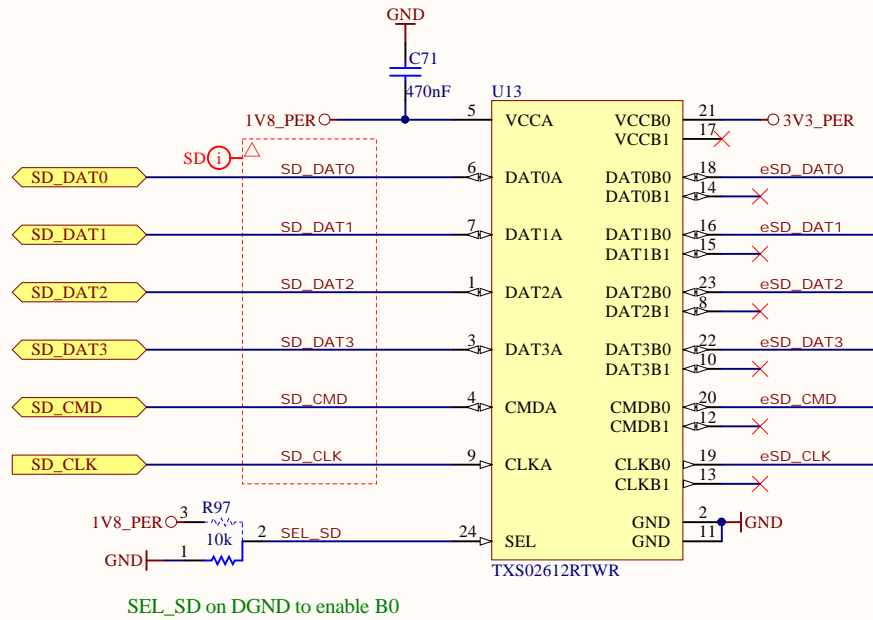


Title LevelShifting_SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm	
Size: A4	Revision: 2v00	Wassertorstr. 10 90489 Nürnberg GERMANY	
Date: 09.11.2019	Time: 15:09:12	Sheet 11 of 23	Author: Andreas Geiger
Project: UltraZOem_CarrierBoard.PriPcb			

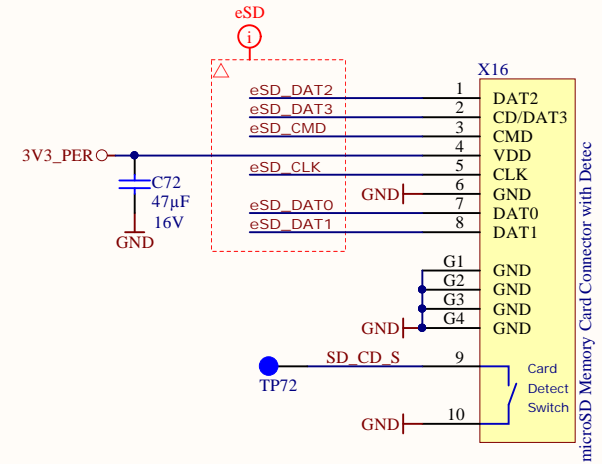




Bidirectional Level Shifting 1.8V to 3.3V



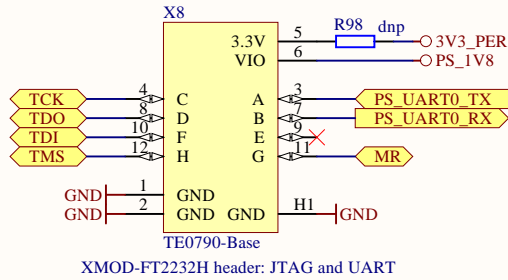
SD Card Connector



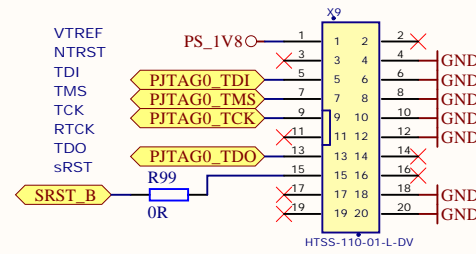
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Size: A4	Revision: 2v00	Wassertorstr. 10	
Date: 09.11.2019	Time: 15:09:12	90489 Nürnberg	
Project: UltraZOhm_CarrierBoard.PrjPcb	Sheet 13 of 23	GERMANY	
		Author: Andreas Geiger	



JTAG-Interface
 JTAG/UART header ('XMOD FTDI JTAG Adapter'-compatible) for access to MPSoC module

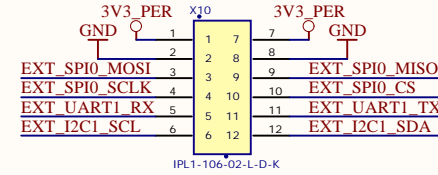


PJTAG-Interface (optional)
 ARM JTAG

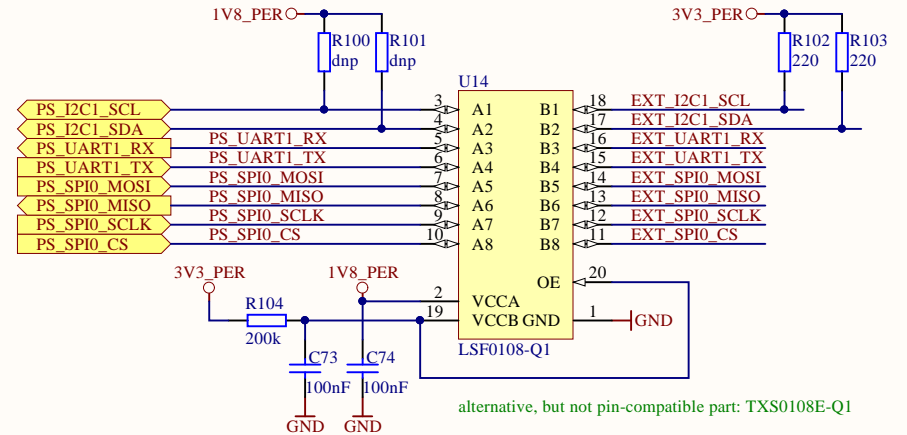


SPI, UART, I2C-Interface (from Processor System)

SPI, UART and I2C Connector @ 3.3V level



Bidirectional Level Shifting 1.8V to 3.3V

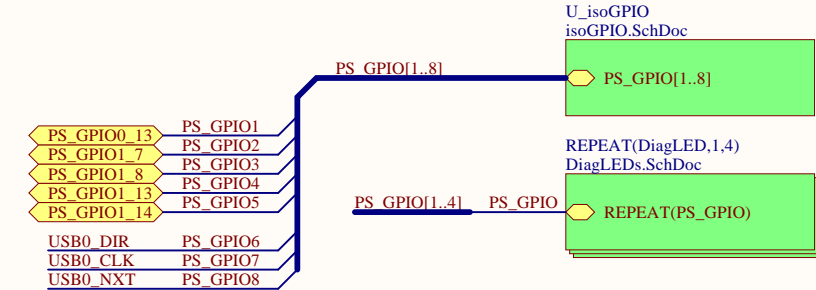


2x Isolated CAN-Interface

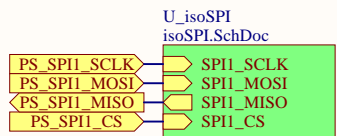
(renamed numbering, because multi channel design in Altium Designer starts with index 1 instead of 0)



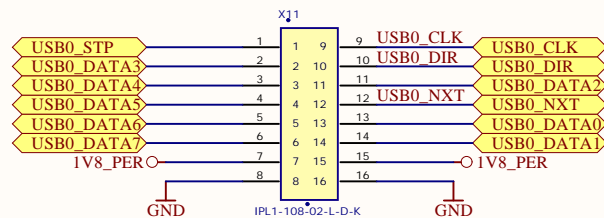
Isolated External GPIO Interface



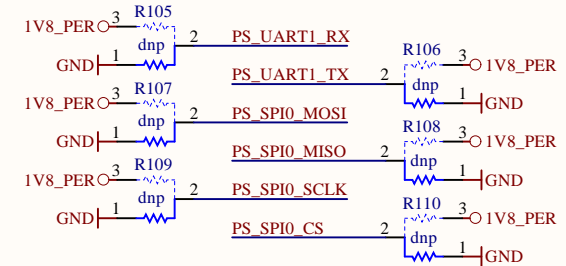
Isolated SPI-Interface

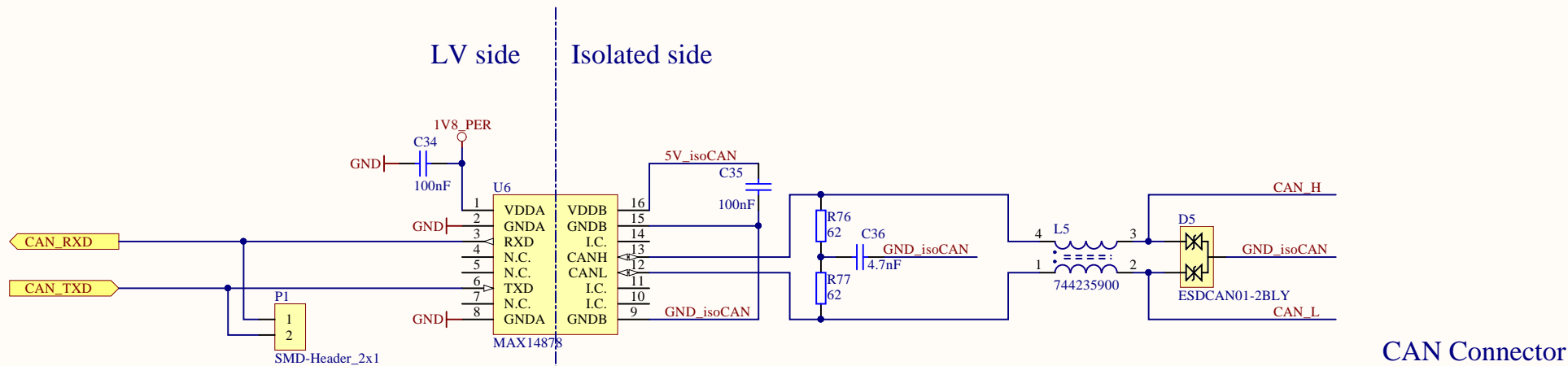


USB Pins on Header
 (for use as extension port or pin use as GPIO)

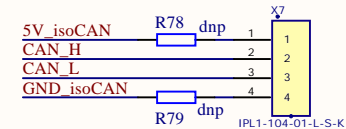


Pull-Up/Pull-Downs @ 1.8V stage

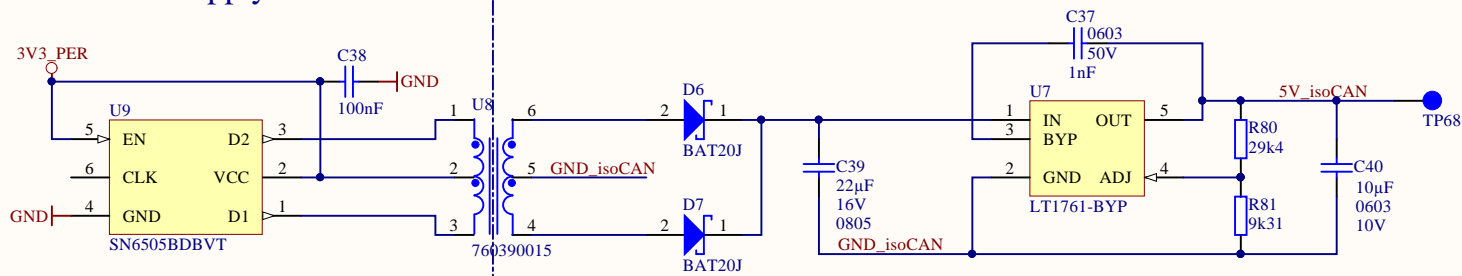




2pol Pin-Header for debugging purposes
(or do not place CAN PHY chip on-board
and use RXD and TXD externally)



Isolated Power Supply

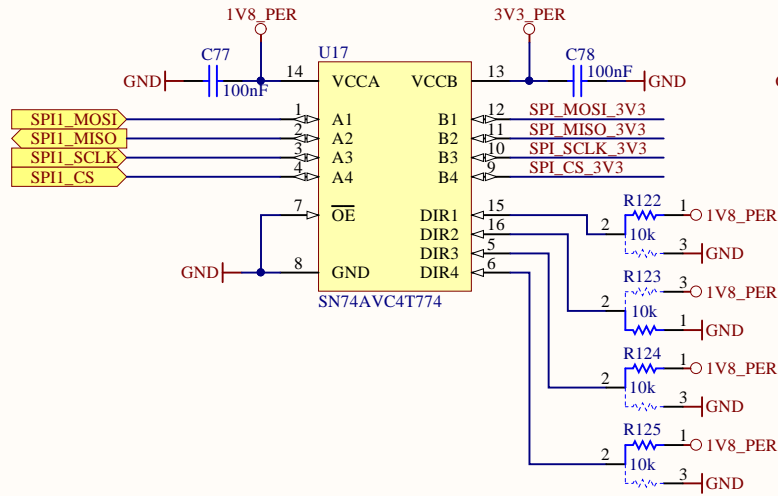


@Falviu: 750316029 instead? recommended at homepage. Or SN6501 instead?
[Link](#)

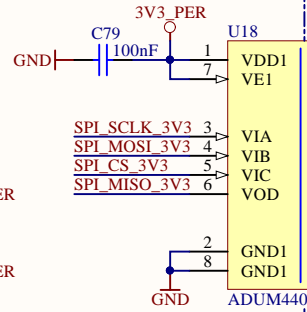
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Size: A4	Revision: 2v00	Wassertorstr. 10	
Date: 09.11.2019	Time: 15:09:12	90489 Nürnberg	
Project: UltraZOhm_CarrierBoard.PrjPcb		Sheet 15 of 23	Author: Andreas Geiger



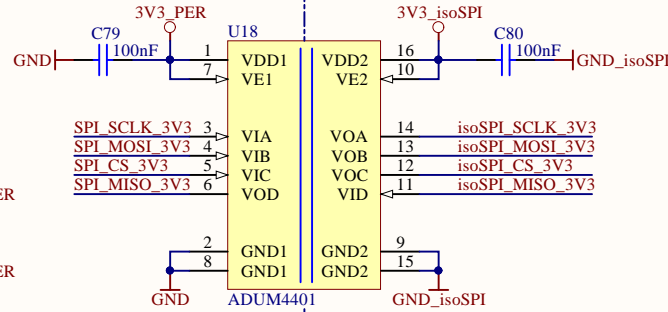
Level Shifting 1.8V to 3.3V



LV side



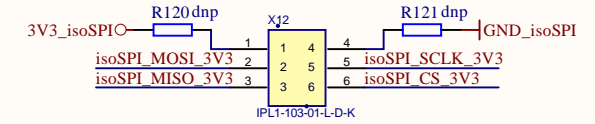
Isolated side



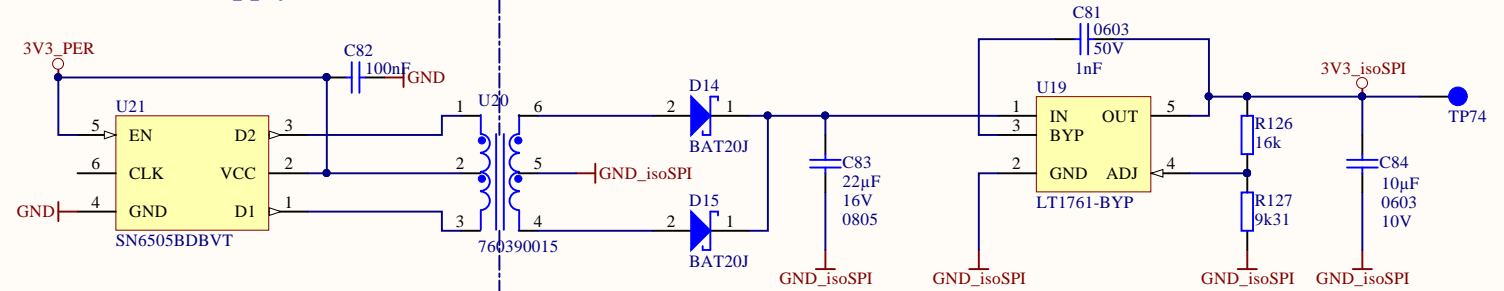
take ADUM4402 if SoC acts as SPI slave

alternative pin-compatible part: Texas Instruments ISO7741DW

SPI Connector



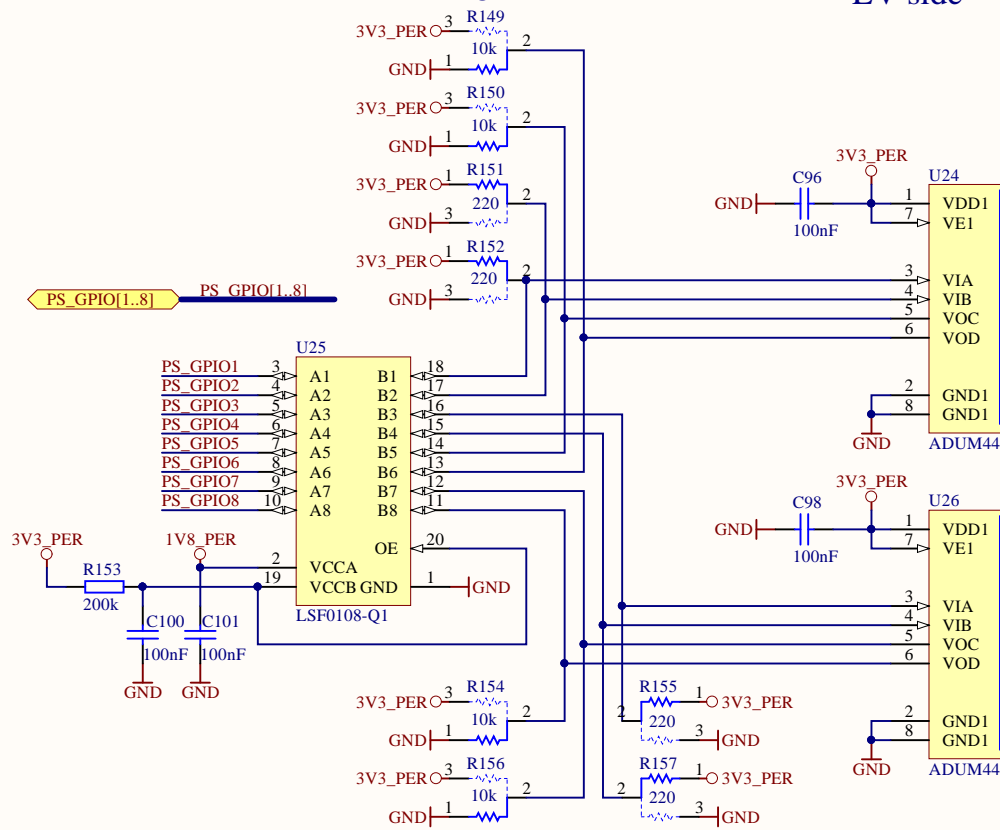
Isolated Power Supply



Title isoSPI.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm	
Size: A4		Wassertorstr. 10	
Revision: 2v00		90489 Nürnberg	
Date: 09.11.2019		GERMANY	
Time: 15:09:12		Sheet 16 of 23	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			



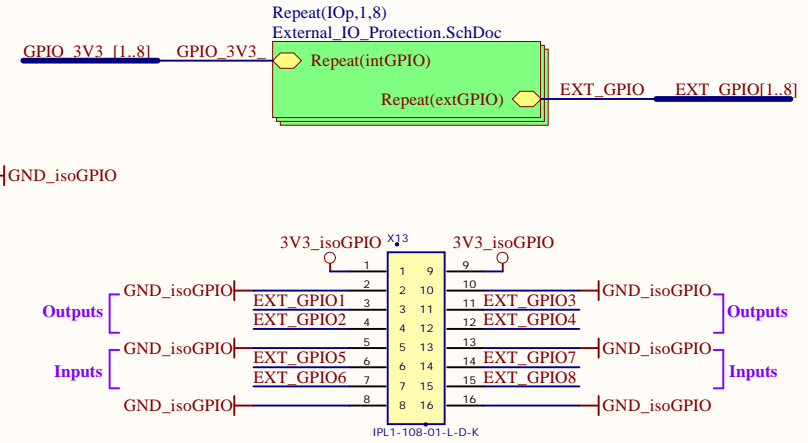
Bidirectional Level Shifting 1.8V to 3.3V



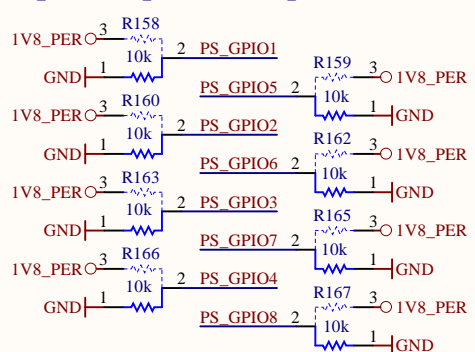
LV side

Isolated side

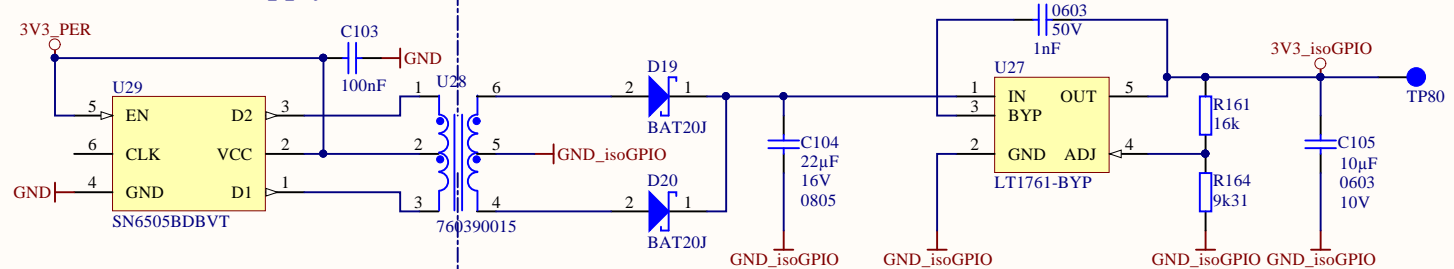
IO Protection with TVS-Diode and PTC-Resistor



Input/Output Pull-Up/Pull-Downs

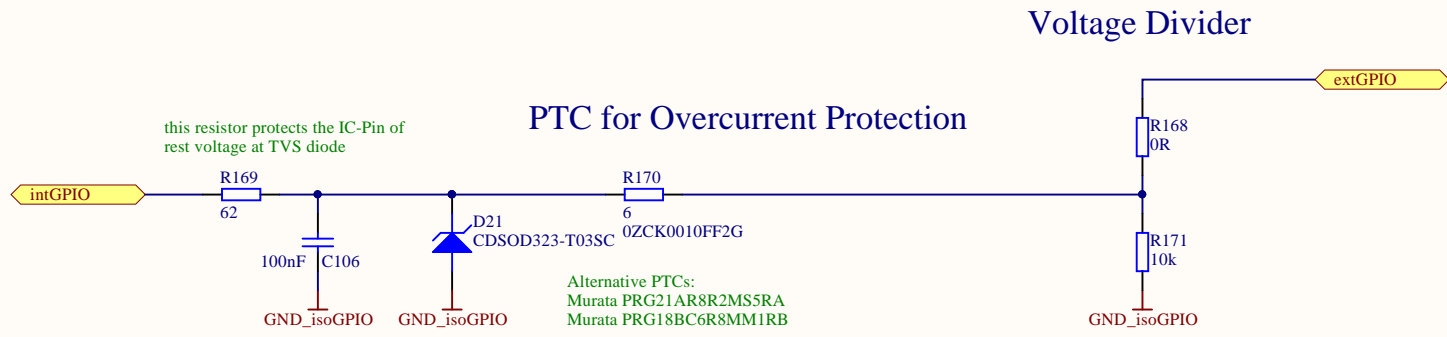


Isolated Power Supply

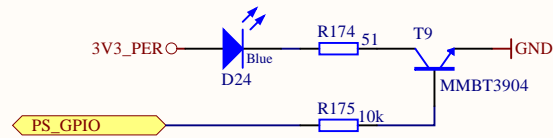



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Size: A4		Wassertorstr. 10	
Revision: 2v00		90489 Nürnberg	
Date: 09.11.2019		GERMANY	
Time: 15:09:12		Sheet 17 of 23	Author: Andreas Geiger
Project: UltraZOhm_CarrierBoard.PrjPcb			



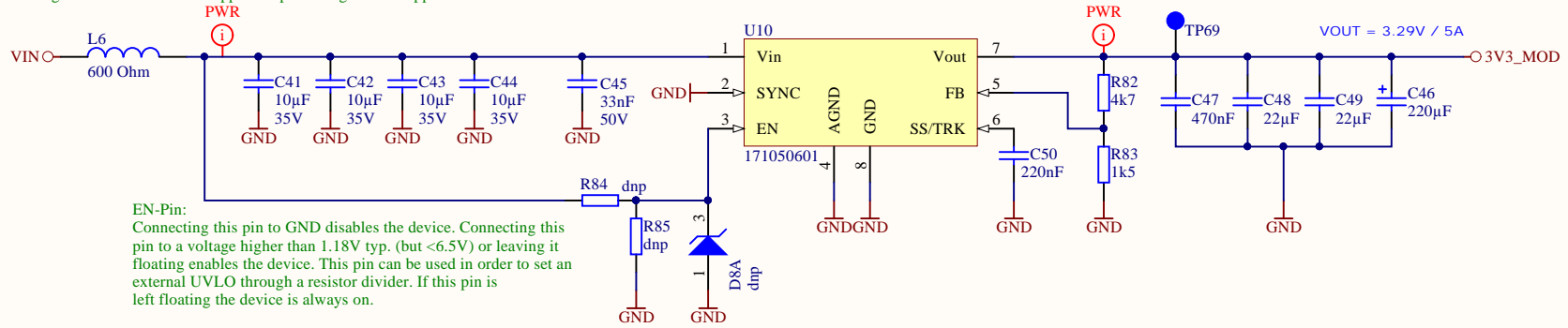


Title External_IO_Protection.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Wassertorstr. 10 90489 Nürnberg GERMANY		
Size: A4	Revision: 2v00			
Date: 09.11.2019	Time: 15:09:12	Sheet 18 of 23	Author: Andreas Geiger	
Project: UltraZOhm_CarrierBoard.PrjPcb				



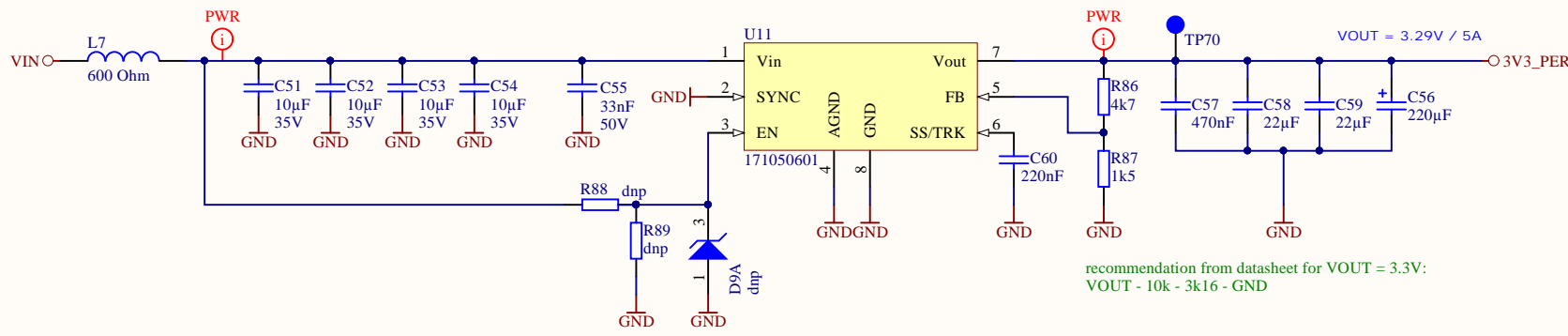
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Size: A4	Revision: 2v00	<i>Wassertorstr. 10</i>	
Date: 09.11.2019	Time: 15:09:12	<i>90489 Nürnberg</i>	
Project: UltraZOhm_CarrierBoard.PrjPcb		Sheet 19 of 23	Author: Andreas Geiger
			

Notes: preferred to use 2x 22µF/50V capacitors at Vin, but this design uses 35V caps due to worse availability at distributors.
 Datasheet: recommended minimum input capacitance is 22 µF (including derating) ceramic with voltage rating at least 25% higher than the maximum applied input voltage for the application.



EN-Pin:
 Connecting this pin to GND disables the device. Connecting this pin to a voltage higher than 1.18V typ. (but <6.5V) or leaving it floating enables the device. This pin can be used in order to set an external UVLO through a resistor divider. If this pin is left floating the device is always on.

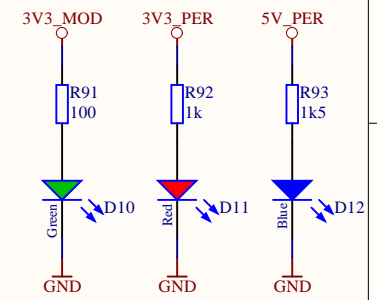
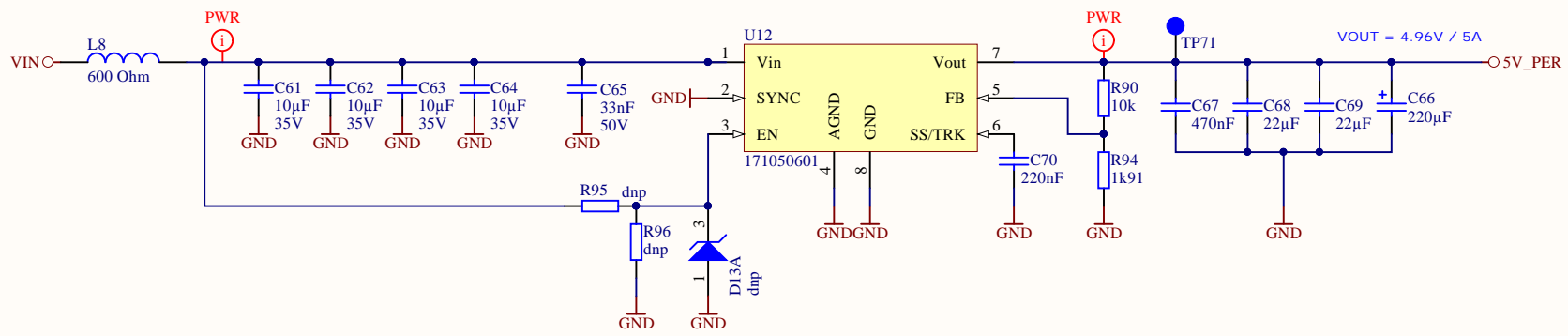
power supply for:
 - Trenz module (PL_1V8, PS_1V8, ...)



power supply for:
 - digital and analog sockets
 - SD-Card
 - Ethernet
 - CAN

recommendation from datasheet for VOUT = 3.3V:
 VOUT - 10k - 3k16 - GND

power supply for:
 - digital and analog sockets



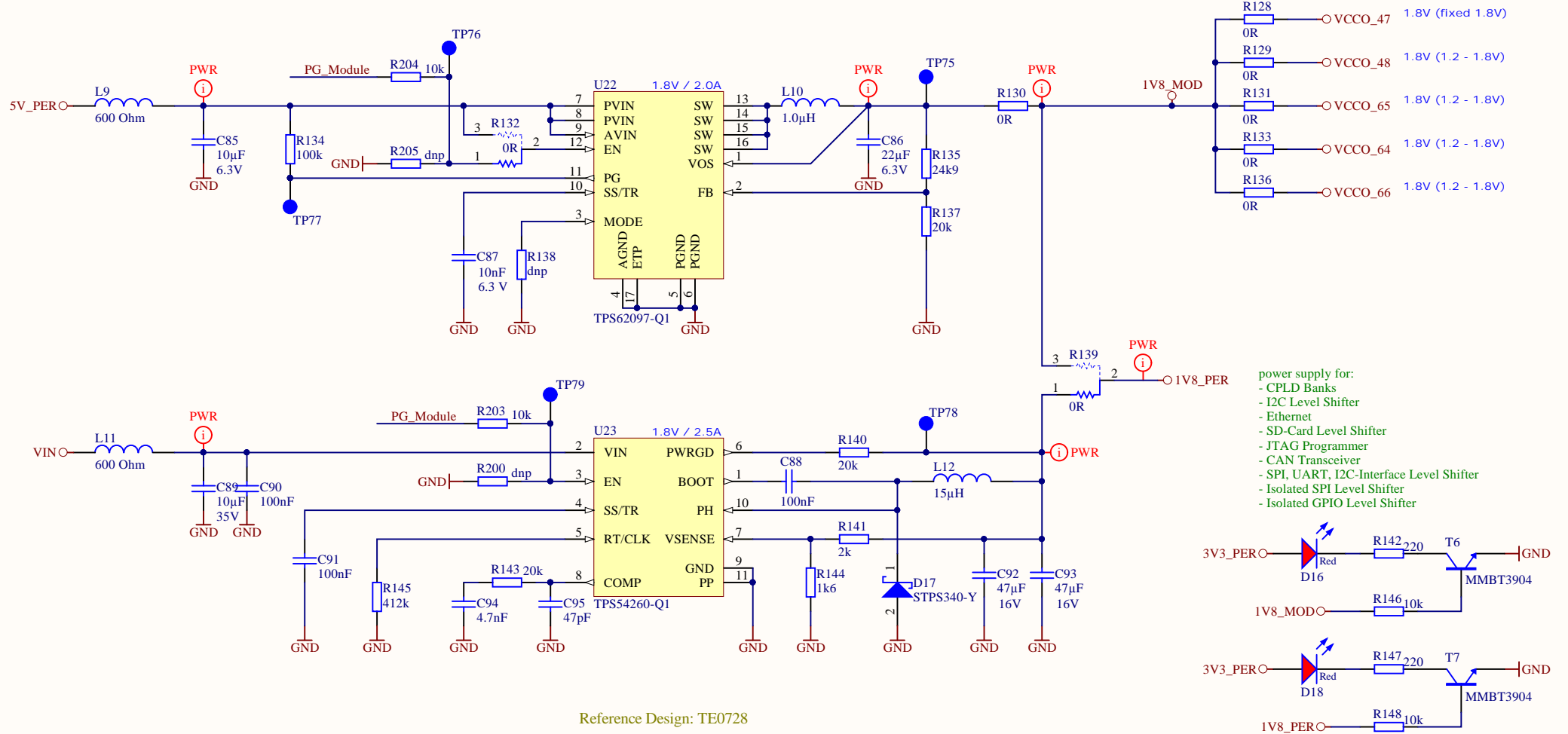
Title Power_Supply_1.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm	
Size: A4	Revision: 2v00	Wassertorstr. 10	
Date: 09.11.2019	Time: 15:09:12	90489 Nürnberg	
Project: UltraZOhm_CarrierBoard.PrjPcb		Sheet 20 of 23	Author: Andreas Geiger
		GERMANY	



PG_Module PG_Module

power good signal from Trenez module to enable banks and peripherals after module is supplied sufficiently

bank power supply with jumper selectable (place near to Trenez module!)



- power supply for:
- CPLD Banks
 - I2C Level Shifter
 - Ethernet
 - SD-Card Level Shifter
 - JTAG Programmer
 - CAN Transceiver
 - SPI, UART, I2C-Interface Level Shifter
 - Isolated SPI Level Shifter
 - Isolated GPIO Level Shifter

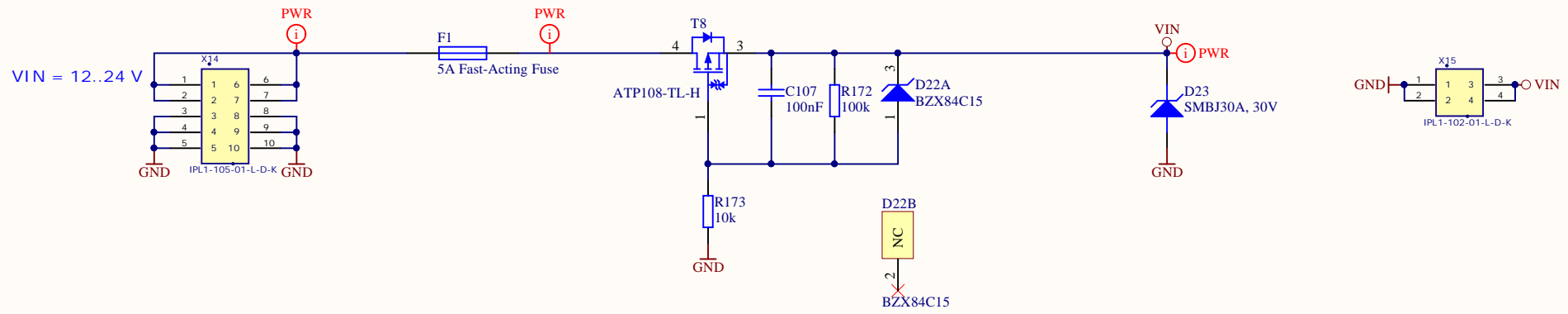
Reference Design: TE0728

Reference Design: TPS82085SIL (TE0808/POWER.SchDoc) not in stock at distributors...

Title Power_Supply_2.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm	
Size: A4		Wassertorstr. 10	
Revision: 2v00		90489 Nürnberg	
Date: 09.11.2019		GERMANY	
Time: 15:09:13		Author: Andreas Geiger	
Project: UltraZOhm_CarrierBoard.PrjPcb		Sheet 21 of 23	



Short Circuit Protection Reverse Polarity Protection Overvoltage Protection



Title Power_Supply_Input.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm	
Size: A4		Wassertorstr. 10	
Revision: 2v00		90489 Nürnberg	
Date: 09.11.2019		GERMANY	
Time: 15:09:13		Author: Andreas Geiger	
Sheet 22 of 23		Project: UltraZOhm_CarrierBoard.PrjPcb	



