Power Supply Encoder

3V3_PER_fused — L1A BLM31PG330SN1L — +3V3_E
5V_PER_fused — L2A BLM31PG330SN1L — +5V_E
VIN_fused — L3A BLM31PG330SN1L — VIN_E

Encoder Supply Voltage

S1A SS-3235S-L1

24V supply for encoder
VIN_E → V_Supply

5V supply for encoder
+5V_E → V_Supply

Encoder Input

J1A DSUB1.385-2H9

RS485_B_DATA	1
GND_DSUB	6
RS485_A_DATA	2
	7
RS485_B_CLOCK	3
	8
RS485_A_CLOCK	4
	9
V_Supply	5
	11
	10

R26A 0R → GND
R28A 0R → GND

X2A Pin Header
RS485_B_DATA
RS485_A_DATA
RS485_B_CLOCK
RS485_A_CLOCK
V_Supply
GND_Header
R27A 0R → GND

do not change the DSUB positions on the PCB

READ_WRITE_CLOCK_SH
TX-S_CLOCK_SH
RX-S_CLOCK_SH
READ_WRITE_DATA_SH
TX-S_DATA_SH
RX-S_DATA_SH

R42A 100k, R43A 100k, R44A 100k, R45A 100k → GND

U2A TXB0108PWR
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
OE → +3V3_E
VCCA ← +3V3_E
VCCB ← +5V_E
GND → GND

+5V_E
R3A 1k, R4A 1k, R5A 1k, R6A 1k, R7A 1k, R9A 1k
C1A 1 nF, C2A 1 nF, C3A 1 nF, C4A 1 nF, C5A 1 nF, C6A 1 nF → GND

RX-S_DATA
TX-S_DATA
READ_WRITE_DATA
RX-S_CLOCK
TX-S_CLOCK
READ_WRITE_CLOCK

R10A 0R 75_R1
R11A 0R 75_RE1
R12A 0R 75_DE1
R16A 10k → GND
R23A 10k → GND

U3A
R RE DE D
VCC B A GND

+5V_E → R18A 1k
C12A 1 nF → GND
R39A 10R RS485_B_DATA → D4A CDSOT23-SM712
R22A 120R
R36A 10R RS485_A_DATA → D4A CDSOT23-SM712
C10A 1 nF → GND
R20A 1k → GND

R13A 0R 75_R2
R14A 0R 75_RE2
R17A 0R 75_DE2
R15A 10k → GND
R24A 10k → GND

U4A
R RE DE D
VCC B A GND

+5V_E → R19A 1k
C13A 1 nF → GND
R37A 10R RS485_B_CLOCK → D5A CDSOT23-SM712
R25A 120R
R38A 10R RS485_A_CLOCK → D5A CDSOT23-SM712
C11A 1 nF → GND
R21A 1k → GND

+3V3_E
C7A 100 nF, C8A 100 nF → GND

+5V_E
C9A 100 nF, C14A 100 nF, C15A 100 nF, C16A 100 nF → GND

Title Encoder_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 02	Design Engineer: TG/MH	
Project: uz_d_absolute_encoder.PrjPCB		Date: 24.04.2026
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Power Supply Encoder

3V3_PER_fused — L1B BLM31PG330SN1L — +3V3_E
5V_PER_fused — L2B BLM31PG330SN1L — +5V_E
VIN_fused — L3B BLM31PG330SN1L — VIN_E

Encoder Supply Voltage

S1B SS-3235S-L1

24V supply for encoder
VIN_E → V_Supply

5V supply for encoder
+5V_E → V_Supply

Encoder Input

J1B DSUB1.385-2H9

RS485_B_DATA	1
GND_DSUB	6
RS485_A_DATA	2
	7
RS485_B_CLOCK	3
	8
RS485_A_CLOCK	4
	9
V_Supply	5
	11
	10

R26B 0R → GND
R28B 0R → GND

do not change the DSUB positions on the PCB

X2B Pin Header
RS485_B_DATA
RS485_A_DATA
RS485_B_CLOCK
RS485_A_CLOCK
V_Supply
GND_Header
R27B 0R → GND

READ_WRITE_CLOCK_SH
TX-S_CLOCK_SH
RX-S_CLOCK_SH
READ_WRITE_DATA_SH
TX-S_DATA_SH
RX-S_DATA_SH

R42B 100k, R43B 100k, R44B 100k, R45B 100k

U2B TXB0108PWR
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
OE
VCCA VCCB GND
+3V3_E, +5V_E

R3B 1k, R4B 1k, R5B 1k, R6B 1k, R7B 1k, R9B 1k
C1B 1 nF, C2B 1 nF, C3B 1 nF, C4B 1 nF, C5B 1 nF, C6B 1 nF

RX-S_DATA
TX-S_DATA
READ_WRITE_DATA
RX-S_CLOCK
TX-S_CLOCK
READ_WRITE_CLOCK

R10B 0R 75_R1
R11B 0R 75_RE1
R12B 0R 75_DE1
R16B 10k
R23B 10k

U3B R RE DE D VCC B A GND

R18B 1k, C12B 1 nF, R39B 10R RS485_B_DATA
R22B 120R
R36B 10R RS485_A_DATA
C10B 1 nF, R20B 1k
D4B CDSOT23-SM712

R13B 0R 75_R2
R14B 0R 75_RE2
R17B 0R 75_DE2
R15B 10k
R24B 10k

U4B R RE DE D VCC B A GND

R19B 1k, C13B 1 nF, R37B 10R RS485_B_CLOCK
R25B 120R
R38B 10R RS485_A_CLOCK
C11B 1 nF, R21B 1k
D5B CDSOT23-SM712

C7B 100 nF, C8B 100 nF
C9B 100 nF, C14B 100 nF, C15B 100 nF, C16B 100 nF

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Power Supply Encoder

3V3_PER_fused — L1C BLM31PG330SN1L — +3V3_E
5V_PER_fused — L2C BLM31PG330SN1L — +5V_E
VIN_fused — L3C BLM31PG330SN1L — VIN_E

Encoder Supply Voltage

S1C SS-3235S-L1

24V supply for encoder
VIN_E → V_Supply

5V supply for encoder
+5V_E → V_Supply

Encoder Input

J1C DSUB1.385-2H9

RS485_B_DATA	1
GND_DSUB	6
RS485_A_DATA	2
	7
RS485_B_CLOCK	3
	8
RS485_A_CLOCK	4
	9
V_Supply	5

R26C 0R → GND
11, 10 → R28C 0R → GND

do not change the DSUB positions on the PCB

X2C Pin Header
RS485_B_DATA
RS485_A_DATA
RS485_B_CLOCK
RS485_A_CLOCK
V_Supply
GND_Header → R27C 0R → GND

READ_WRITE_CLOCK_SH
TX-S_CLOCK_SH
RX-S_CLOCK_SH
READ_WRITE_DATA_SH
TX-S_DATA_SH
RX-S_DATA_SH

R42C 100k, R43C 100k, R44C 100k, R45C 100k → GND

U2C TXB0108PWR
A1 A2 A3 A4 A5 A6 A7 A8 — B1 B2 B3 B4 B5 B6 B7 B8
OE → +3V3_E
VCCA ← +3V3_E
VCCB ← +5V_E
GND

+5V_E
R3C 1k, R4C 1k, R5C 1k, R6C 1k, R7C 1k, R9C 1k
C1C 1 nF, C2C 1 nF, C3C 1 nF, C4C 1 nF, C5C 1 nF, C6C 1 nF → GND

RX-S_DATA
TX-S_DATA
READ_WRITE_DATA
RX-S_CLOCK
TX-S_CLOCK
READ_WRITE_CLOCK

R10C 0R 75_R1
R11C 0R 75_RE1
R12C 0R 75_DE1
R16C 10k → GND
R23C 10k → GND

U3C
R, RE, DE, D — VCC, B, A, GND

+5V_E → R18C 1k
C12C 1 nF → GND
R39C 10R RS485_B_DATA
R22C 120R
R36C 10R RS485_A_DATA
C10C 1 nF → GND
R20C 1k → GND
D4C CDSOT23-SM712

R13C 0R 75_R2
R14C 0R 75_RE2
R17C 0R 75_DE2
R15C 10k → GND
R24C 10k → GND

U4C
R, RE, DE, D — VCC, B, A, GND

+5V_E → R19C 1k
C13C 1 nF → GND
R37C 10R RS485_B_CLOCK
R25C 120R
R38C 10R RS485_A_CLOCK
C11C 1 nF → GND
R21C 1k → GND
D5C CDSOT23-SM712

+3V3_E: C7C 100 nF, C8C 100 nF → GND
+5V_E: C9C 100 nF, C14C 100 nF, C15C 100 nF, C16C 100 nF → GND

Title Encoder_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 02	Design Engineer: TG/MH	
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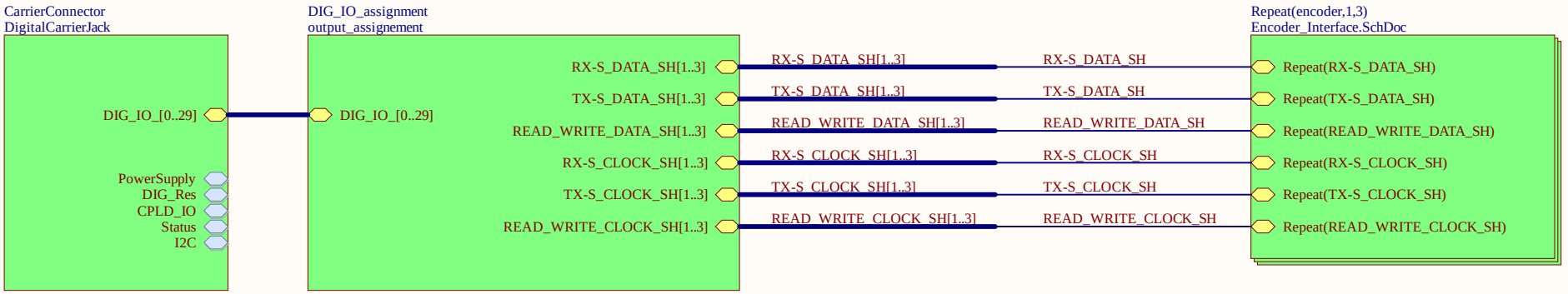


Chose size of UZ logo by chosing footprint type

UltraZohm

LOGO

uz_d_absolute_encoder

Project

02

Revision

ZC_GGG
ZC_PPP
ProjectRevision
ZC_vv

ZC Serialnumber

TG/MH

Designer

05/25

Date

Serial

Serial

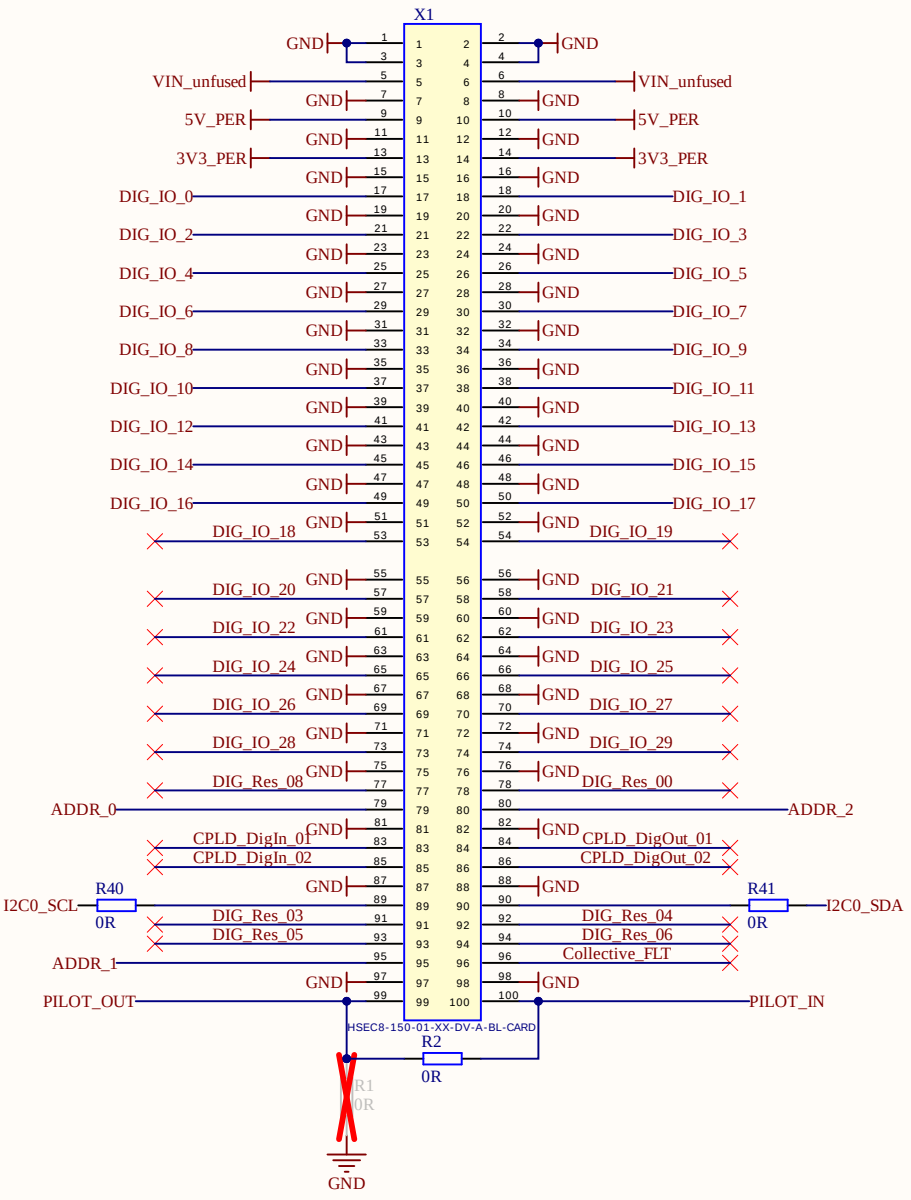
1.0mm

MH1

1.0mm

MH2

Title TopSheet.SchDoc		**UltraZohm** www.ultrazohm.com
Revision: 02	Design Engineer: TG/MH	Date: 24.04.2026
Project: uz_d_absolute_encoder.PrjPCB		Sheet 1 of 6



DIG_IO_[0..29] DIG_IO_[0..29]

DigCon_Status
PILOT_IN PILOT_IN
PILOT_OUT PILOT_OUT
Collective_FLT Collective_FLT
Status

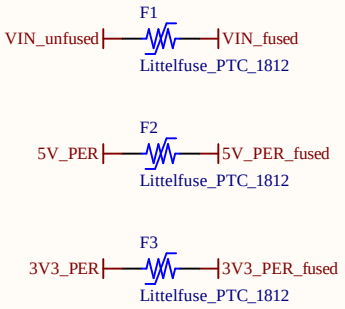
DigCon_DIG_Res
DIG_Res_00 DIG_Res_00
DIG_Res_03 DIG_Res_03
DIG_Res_04 DIG_Res_04
DIG_Res_05 DIG_Res_05
DIG_Res_06 DIG_Res_06
DIG_Res_08 DIG_Res_08
DIG_Res

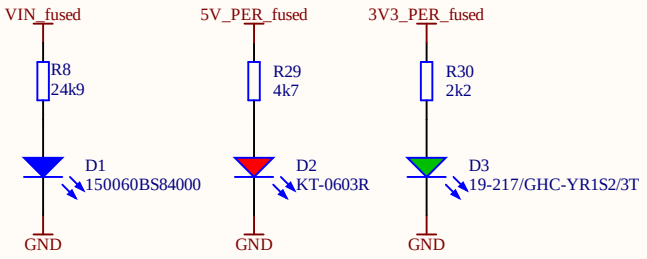
DigCon_PowerSupply
VIN VIN
5V_PER 5V
3V3_PER 3V3
GND GND
PowerSupply

DigCon_I2C
I2C0_SCL I2C0_SCL
I2C0_SCA I2C0_SCA
I2C

DigCon_DCPLD_IO
CPLD_DigIn_01 DCPLD_DigIn_01
CPLD_DigIn_02 DCPLD_DigIn_02
CPLD_DigOut_01 DCPLD_DigOut_01
CPLD_DigOut_02 DCPLD_DigOut_02
CPLD_IO

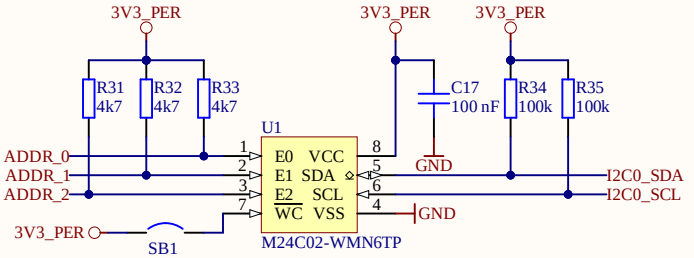
Fused Voltages





EEPROM Interface

(please do not exclude or delete from design)



Note: place solder bump to protect EEPROM memory from write access.

Title DigitalCarrierJack.SchDoc		UltraZohm www.ultrazohm.com
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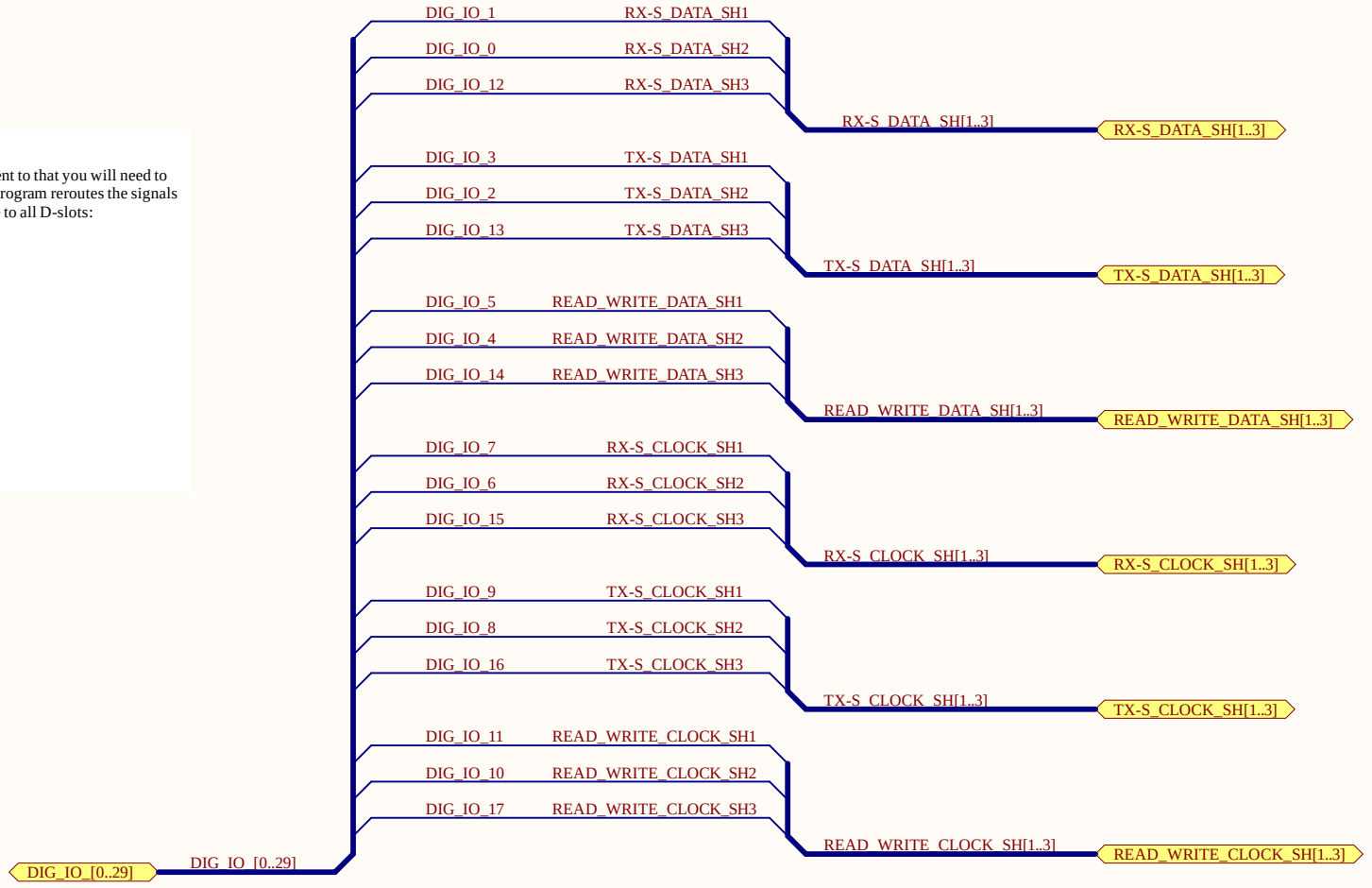
CPLD program uz_d_abs_encoder:

Attention! IO Mapping schown here is different to that you will need to respect in the FPGA design, since the CPLD program reroutes the signals in order to make the adapter board compatible to all D-slots:

Adapter Board <-> FPGA IO Pin - Function
DIG_IO_00 -> Dig_IO_06: RX-Data_2
DIG_IO_01 -> DIG_IO_07: RX-Data_1
DIG_IO_02 <- DIG_IO_09: TX-Data_2
DIG_IO_03 <- DIG_IO_08: TX-Data_1
DIG_IO_04 <- DIG_IO_10: RW_Data_2
DIG_IO_05 <- DIG_IO_11: RW_Data_1
DIG_IO_08 <- DIG_IO_14: TX-Clock_2
DIG_IO_09 <- DIG_IO_15: TX-Clock_1
DIG_IO_10 <- DIG_IO_16: RW-Clock_2
DIG_IO_11 <- DIG_IO_17: RW-Clock_1
DIG_IO_12 -> DIG_IO_18: RX-Data_3
DIG_IO_13 <- DIG_IO_12: TX-Data_3
DIG_IO_14 <- DIG_IO_20: RW-Data_3



Title output_assignement.SchDoc		UltraZohm	
Revision: 02	Design Engineer: TG/MH	www.ultrazohm.com	
Project: uz_d_absolute_encoder.PrjPCB		Date: 24.04.2026	
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