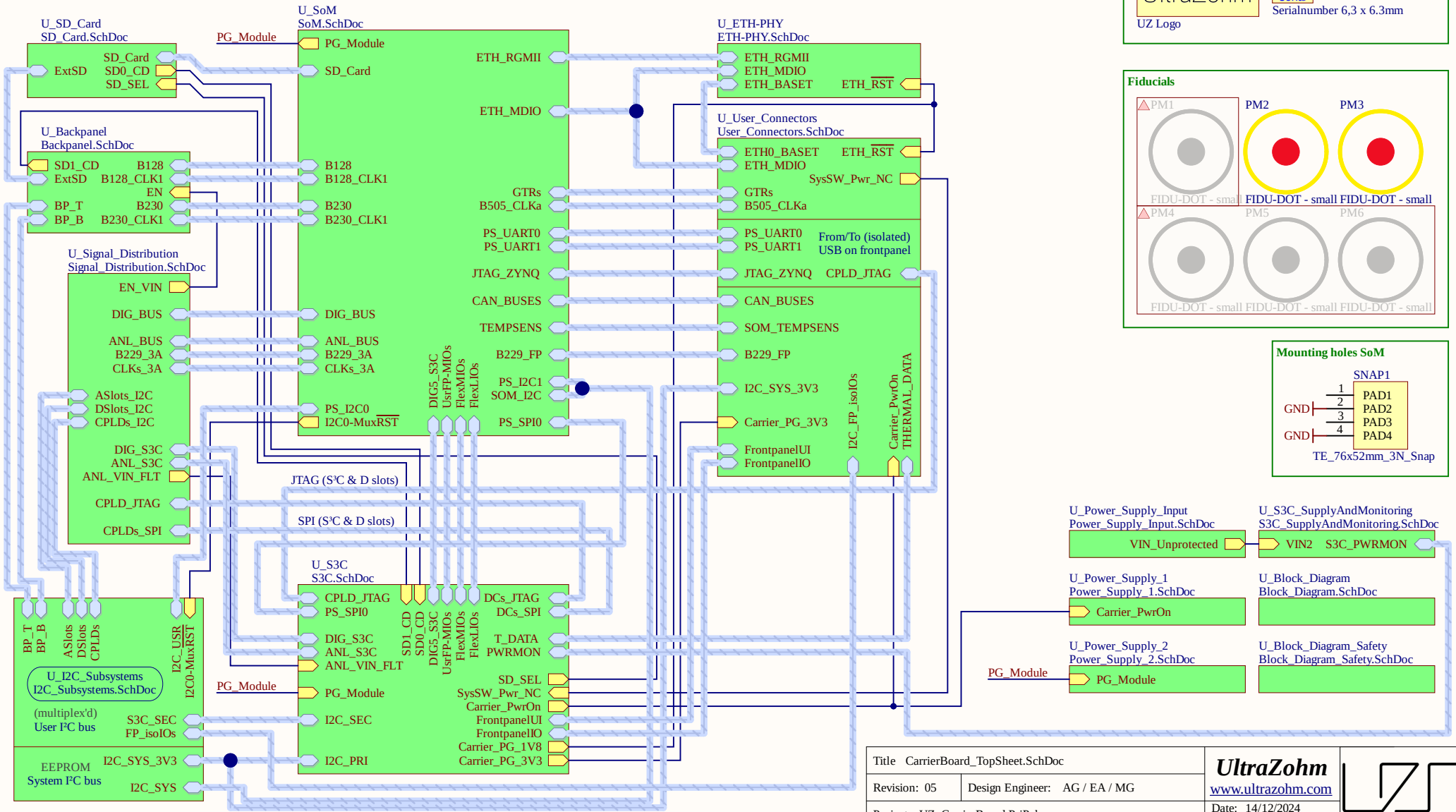
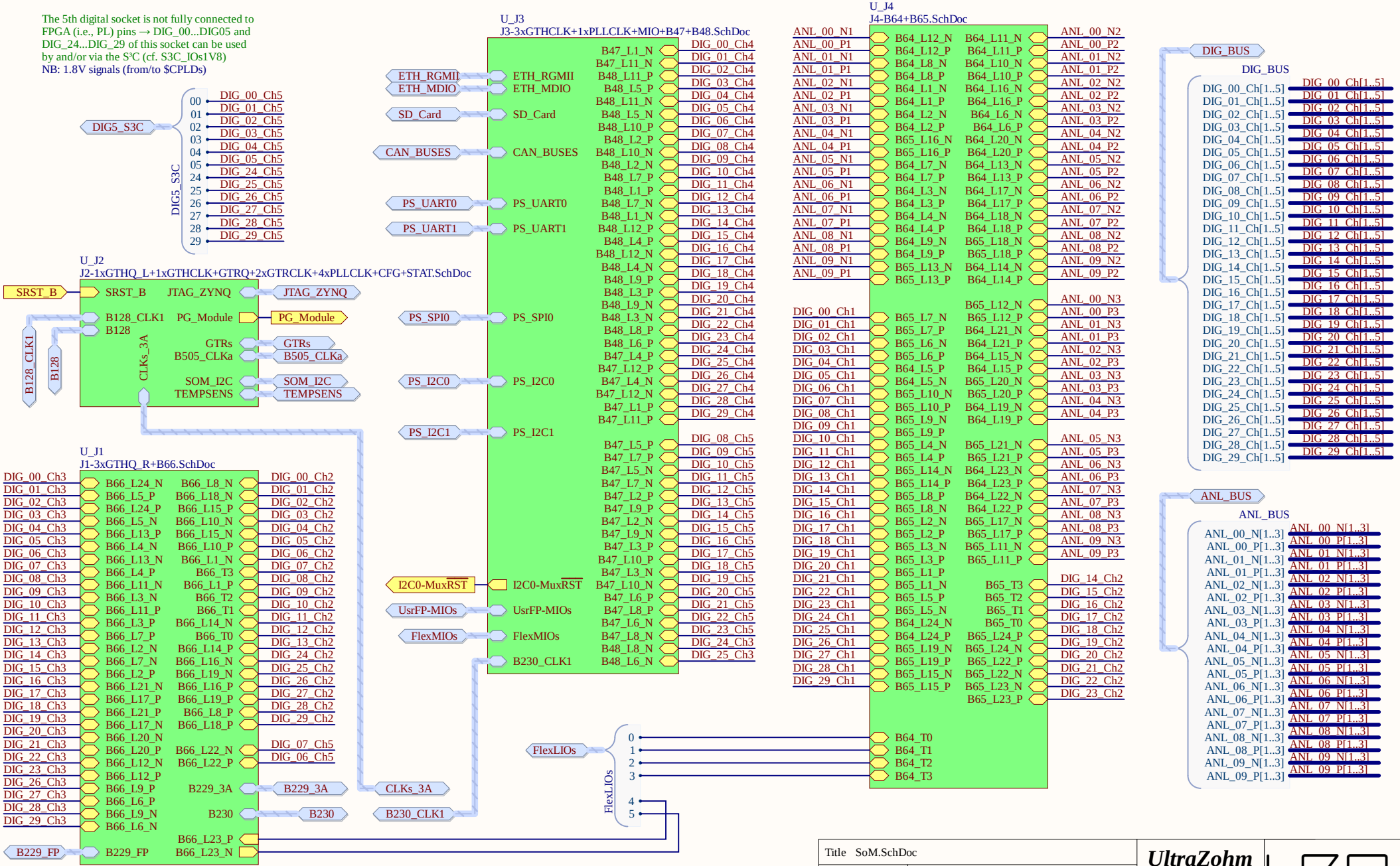
UltraZohm Carrier Board

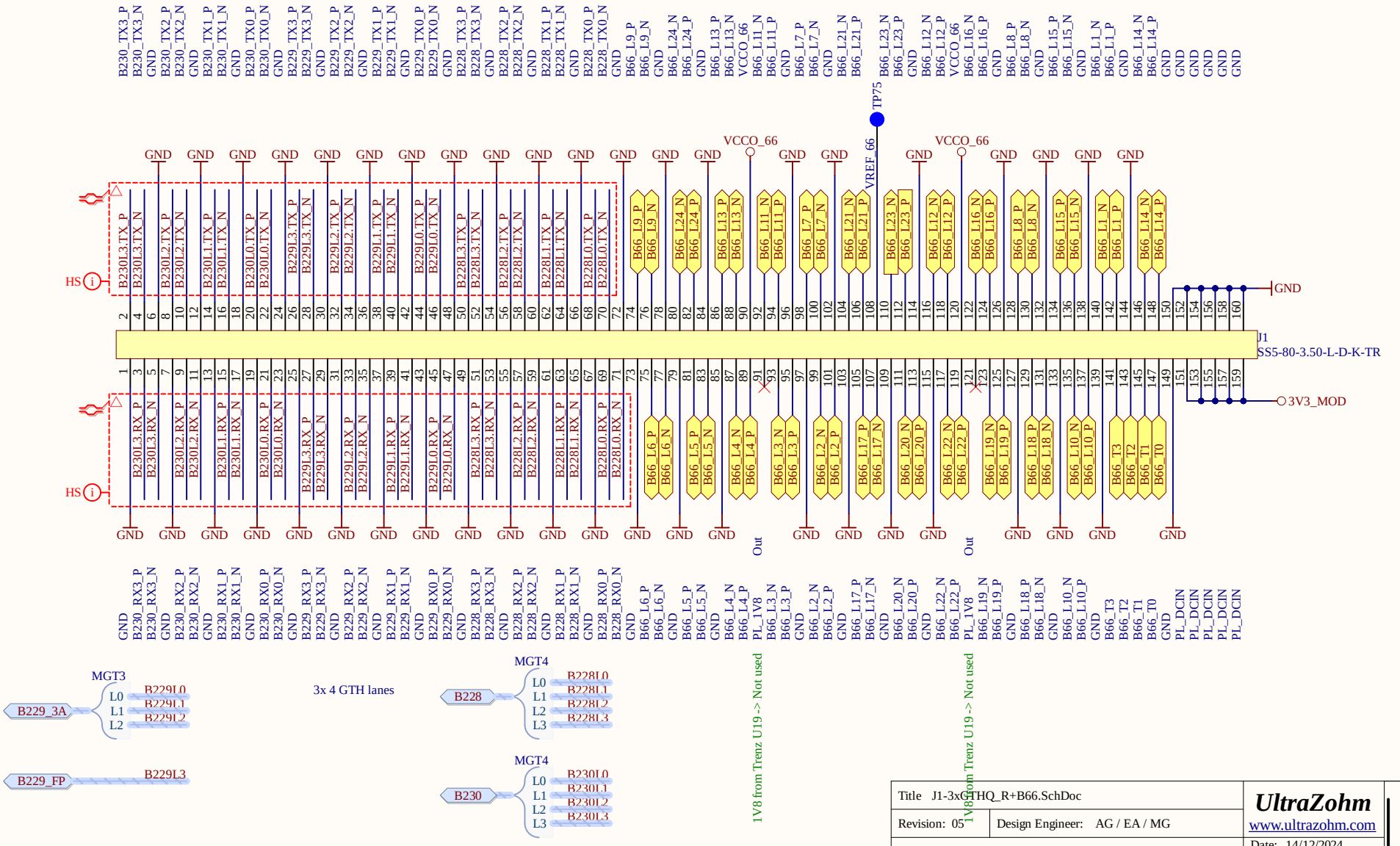
For more information visit: www.ultrazohm.com



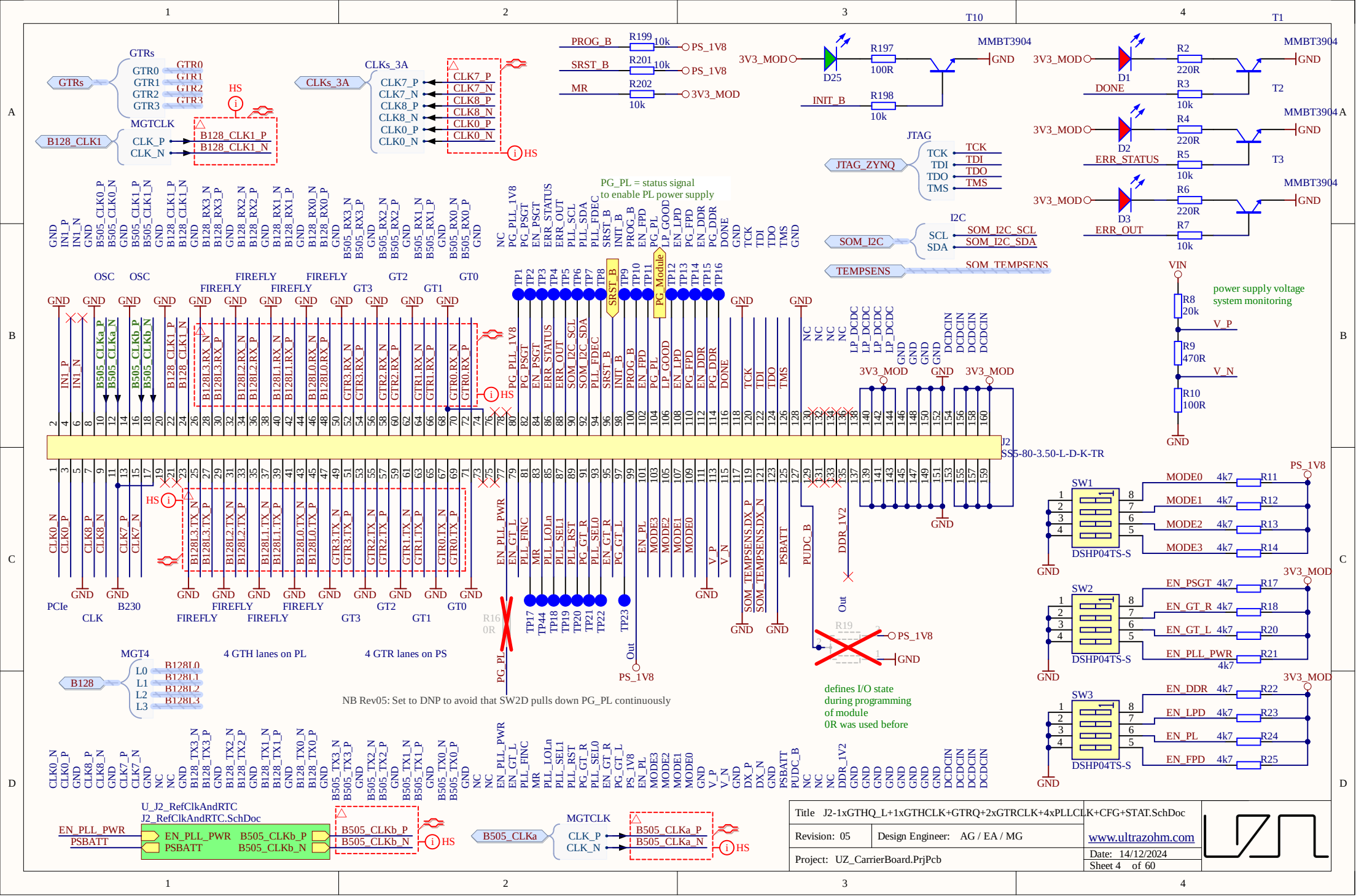
The 5th digital socket is not fully connected to FPGA (i.e., PL) pins → DIG_00...DIG05 and DIG_24...DIG_29 of this socket can be used by and/or via the S³C (cf. S3C_IOs1V8)
NB: 1.8V signals (from/to $CPLDs)

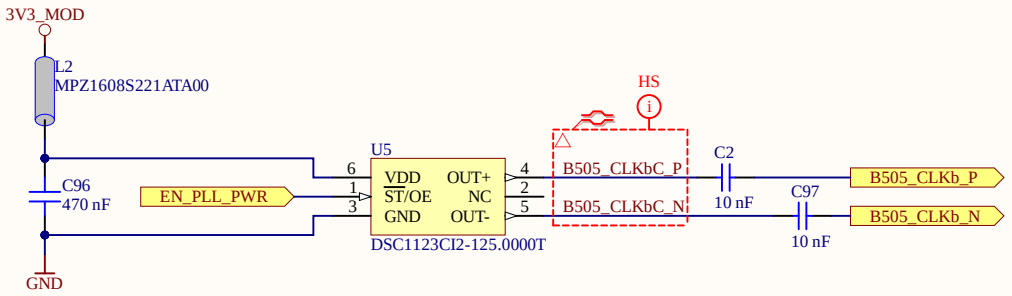


Title SoM.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	Date: 14/12/2024
Project: UZ_CarrierBoard.PrjPcb		Sheet 2 of 60

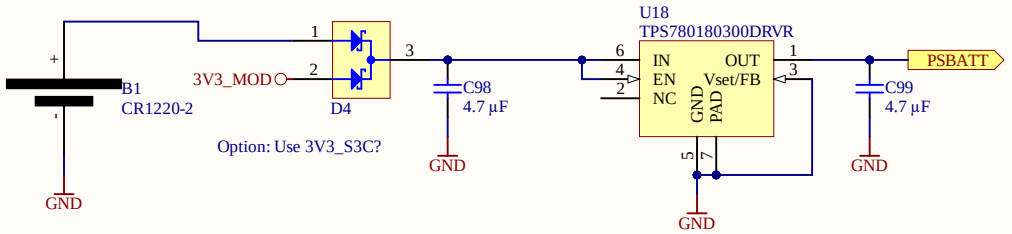


Title J1-3xGTHQ_R+B66.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024 Sheet 3 of 60

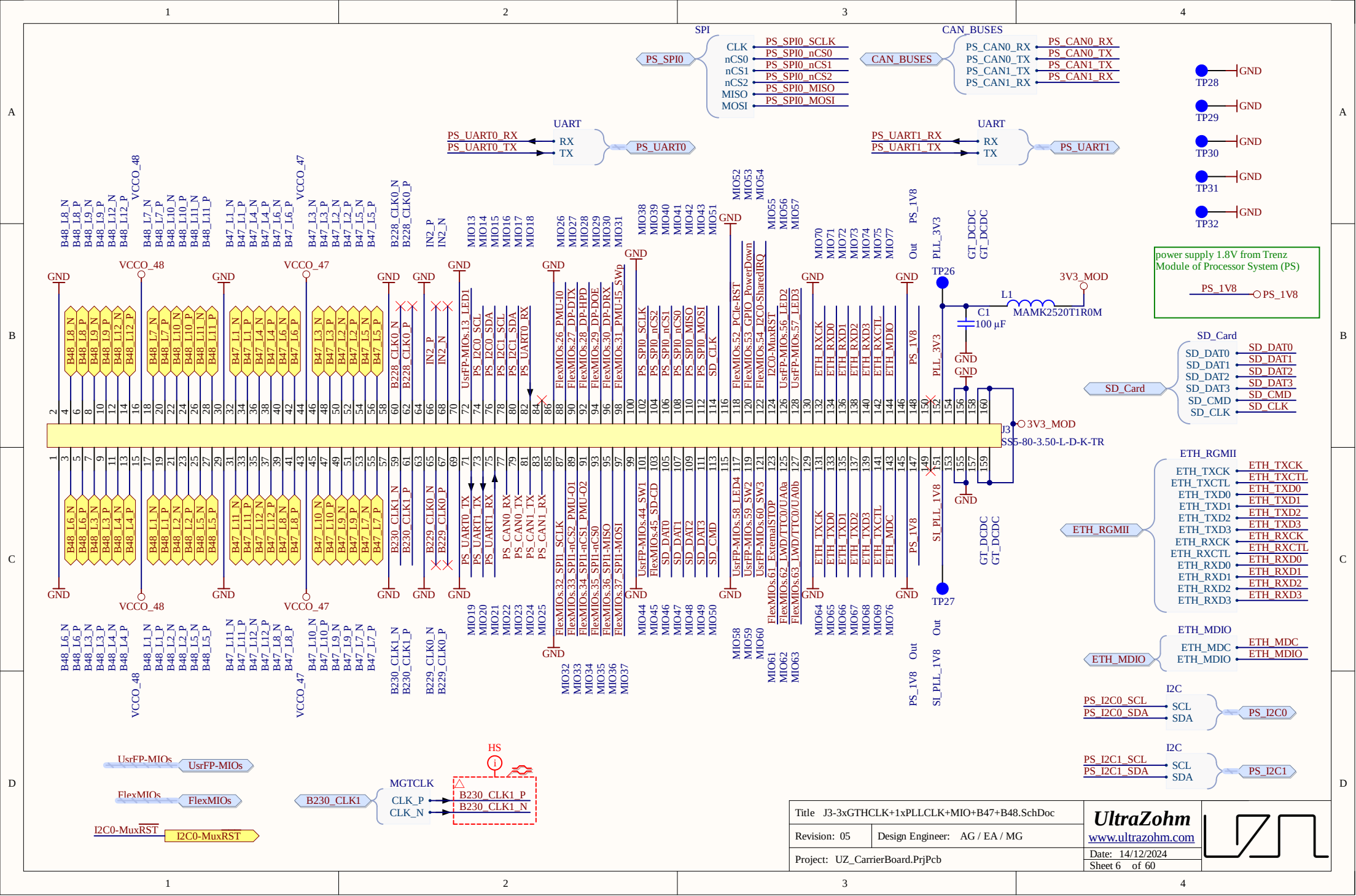

GTRs
GTR0
GTR1
GTR2
GTR3
MGTCLK
CLK_P
CLK_N
B128_CLK1
B128_CLK1_P
B128_CLK1_N
HS
CLKs_3A
CLK7_P
CLK7_N
CLK8_P
CLK8_N
CLK0_P
CLK0_N
PROG_B
SRST_B
MR
R199 10k
R201 10k
R202 10k
PS_1V8
3V3_MOD
JTAG
TCK
TDI
TDO
TMS
JTAG_ZYNQ
I2C
SCL
SDA
SOM_I2C
SOM_I2C_SCL
SOM_I2C_SDA
TEMPSENS
SOM_TEMPSENS
D25
R197 100R
INIT_B
R198 10k
MMBT3904
GND
D1
R2 220R
DONE
R3 10k
T2
D2
R4 220R
ERR_STATUS
R5 10k
T3
D3
R6 220R
ERR_OUT
R7 10k
PG_PL = status signal
to enable PL power supply
OSC
FIREFLY
GT3
GT2
GT1
GT0
PG_Module
J2
SS5-80-3.50-L-D-K-TR
VIN
R8 20k
R9 470R
R10 100R
V_P
V_N
power supply voltage
system monitoring
DSHP04TS-S
SW1
SW2
SW3
MODE0 4k7 R11
MODE1 4k7 R12
MODE2 4k7 R13
MODE3 4k7 R14
EN_PSGT 4k7 R17
EN_GT_R 4k7 R18
EN_GT_L 4k7 R20
EN_PLL_PWR 4k7 R21
EN_DDR 4k7 R22
EN_LPD 4k7 R23
EN_PL 4k7 R24
EN_FPD 4k7 R25
PCIe
CLK
B230
MGT4
B128
L0
L1
L2
L3
4 GTH lanes on PL
4 GTR lanes on PS
R16 0R
PG_PL
R19
Out
DDR_1V2
PUDC_B
defines I/O state
during programming
of module
0R was used before
NB Rev05: Set to DNP to avoid that SW2D pulls down PG_PL continuously
U_J2_RefClkAndRTC
J2_RefClkAndRTC.SchDoc
EN_PLL_PWR
PSBATT
B505_CLKb_P
B505_CLKb_N
B505_CLKa
B505_CLKa_P
B505_CLKa_N
Title J2-1xGTHQ_L+1xGTHCLK+GTRQ+2xGTRCLK+4xPLLCLK+CFG+STAT.SchDoc
Revision: 05
Design Engineer: AG / EA / MG
www.ultrazohm.com
Project: UZ_CarrierBoard.PrjPcb
Date: 14/12/2024
Sheet 4 of 60

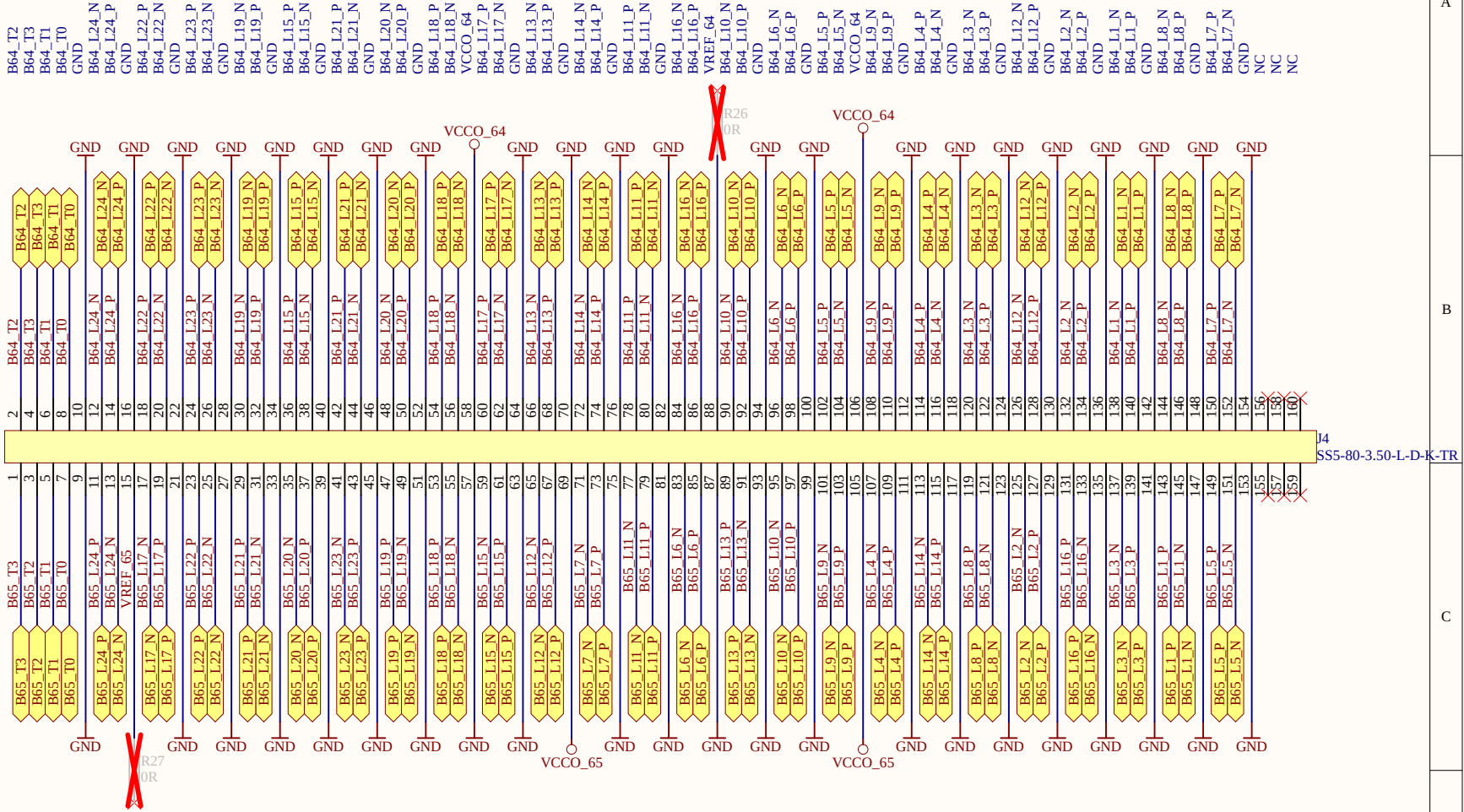


Cf. AR#75318 (we might want to drop to 1.5V to remain within the I-spec'd range)

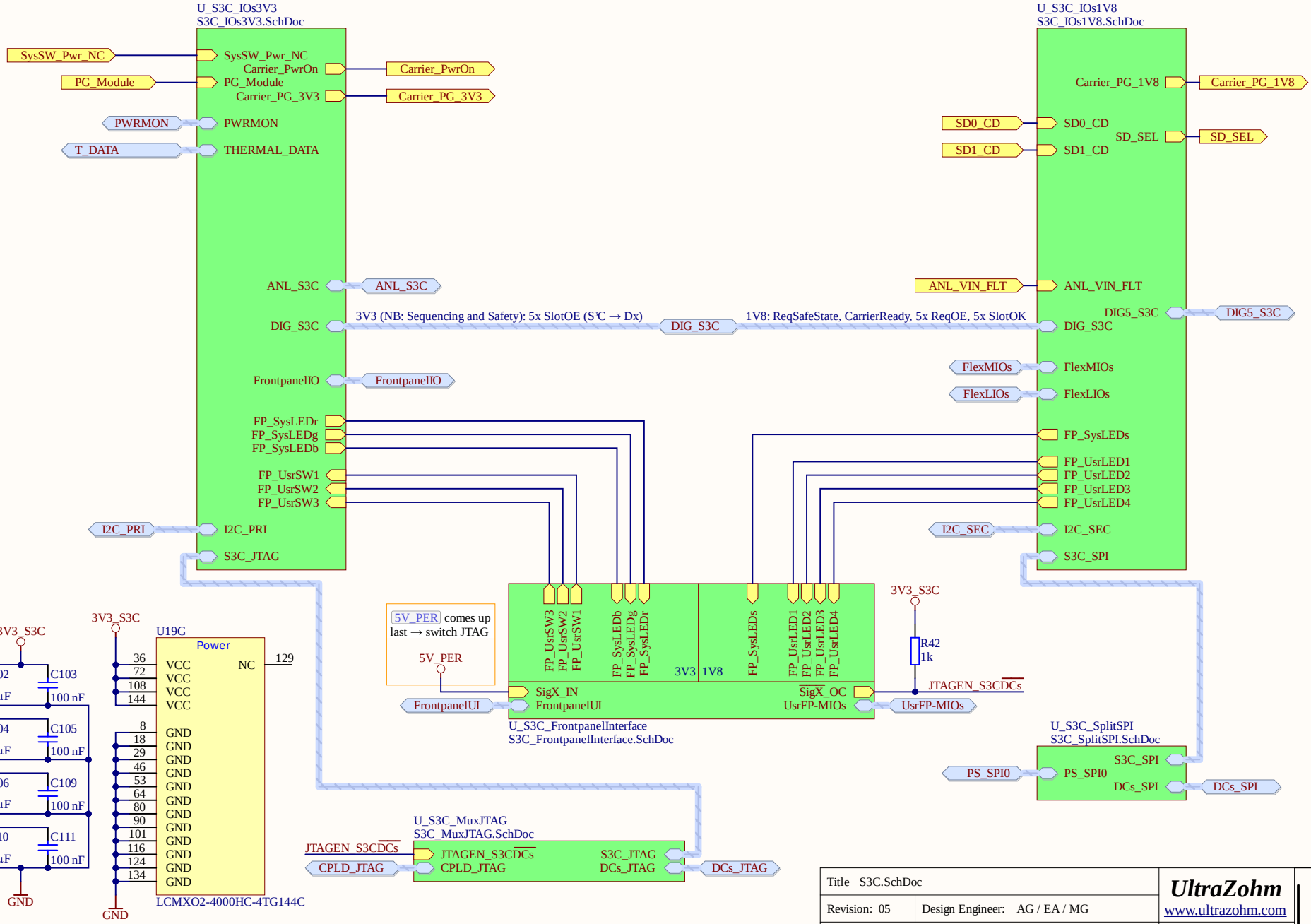


Title J2_RefClkAndRTC.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 5 of 60	

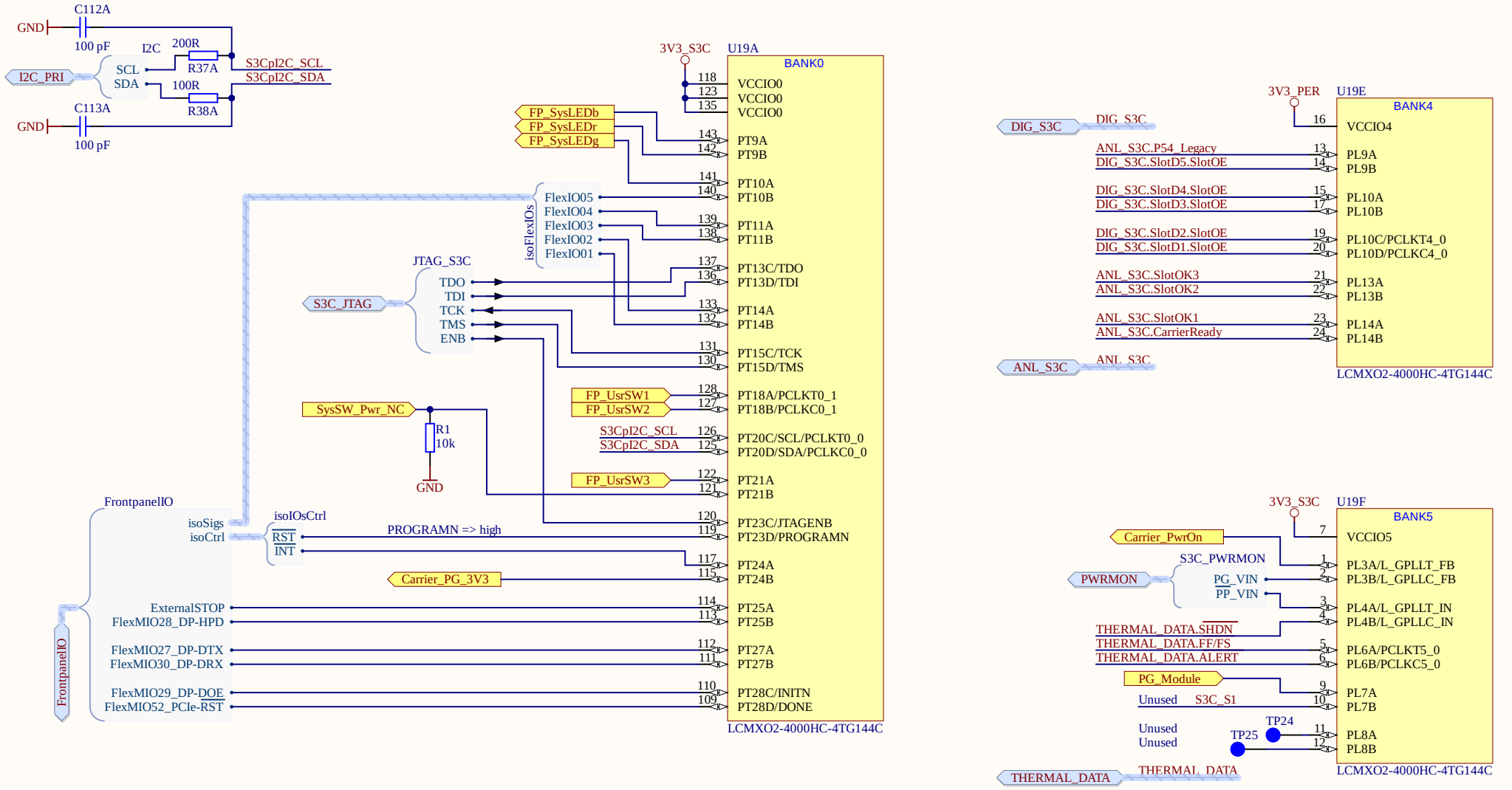

SPI
PS_SPI0
CLK
nCS0
nCS1
nCS2
MISO
MOSI
PS_SPI0_SCLK
PS_SPI0_nCS0
PS_SPI0_nCS1
PS_SPI0_nCS2
PS_SPI0_MISO
PS_SPI0_MOSI
CAN_BUSES
PS_CAN0_RX
PS_CAN0_TX
PS_CAN1_TX
PS_CAN1_RX
UART
PS_UART0
PS_UART1
RX
TX
TP28
TP29
TP30
TP31
TP32
GND
power supply 1.8V from Trenz Module of Processor System (PS)
TP26
TP27
L1
MAMK2520T1R0M
C1
100 µF
3V3_MOD
J3
SS5-80-3.50-L-D-K-TR
SD_Card
ETH_RGMII
ETH_MDIO
I2C
PS_I2C0
PS_I2C1
HS
MGTCLK
B230_CLK1
UsrFP-MIOs
FlexMIOs
I2C0-MuxRST
Title J3-3xGTHCLK+1xPLLCLK+MIO+B47+B48.SchDoc
Revision: 05
Design Engineer: AG / EA / MG
Project: UZ_CarrierBoard.PrjPcb
UltraZohm
www.ultrazohm.com
Date: 14/12/2024
Sheet 6 of 60



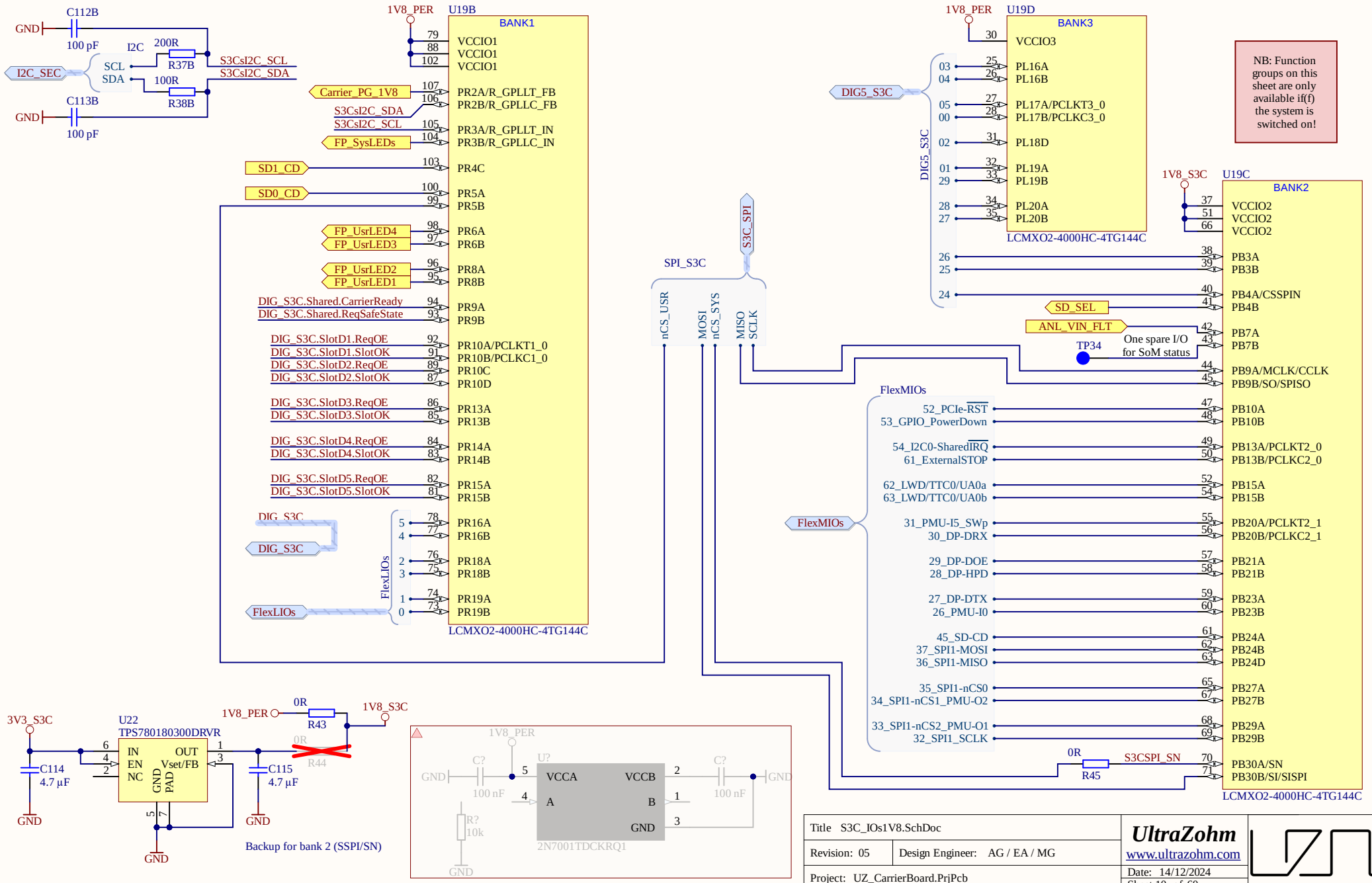
Title J4-B64+B65.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024 Sheet 7 of 60

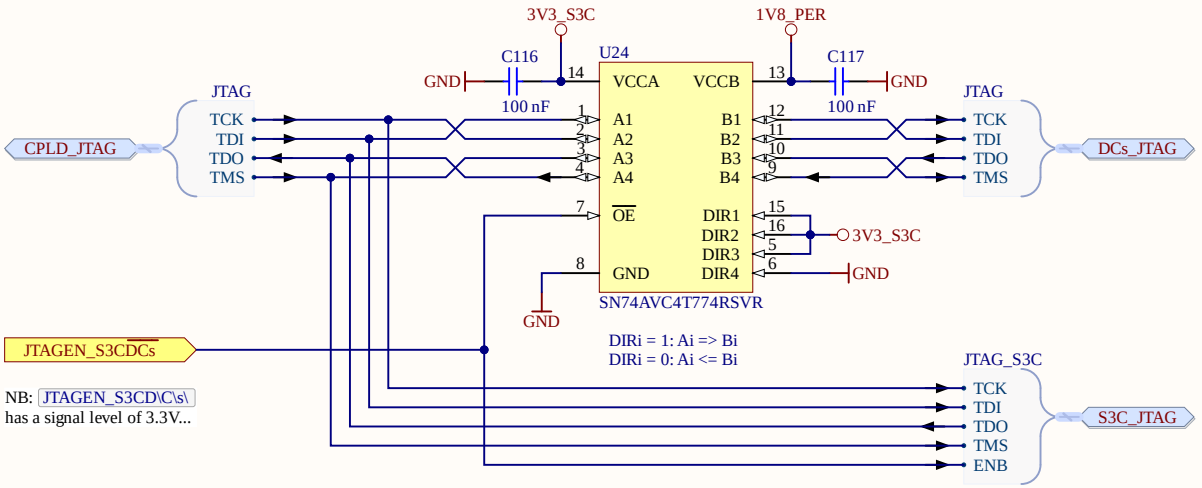


Title S3C.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	Date: 14/12/2024
Project: UZ_CarrierBoard.PrjPcb		Sheet 8 of 60

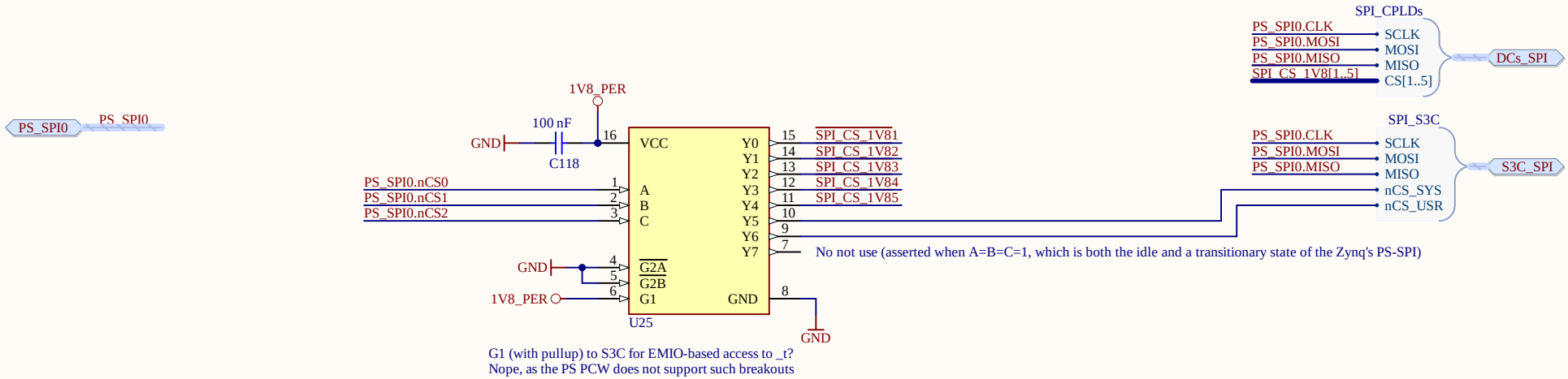


Title S3C_IOs3V3.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 9 of 60	

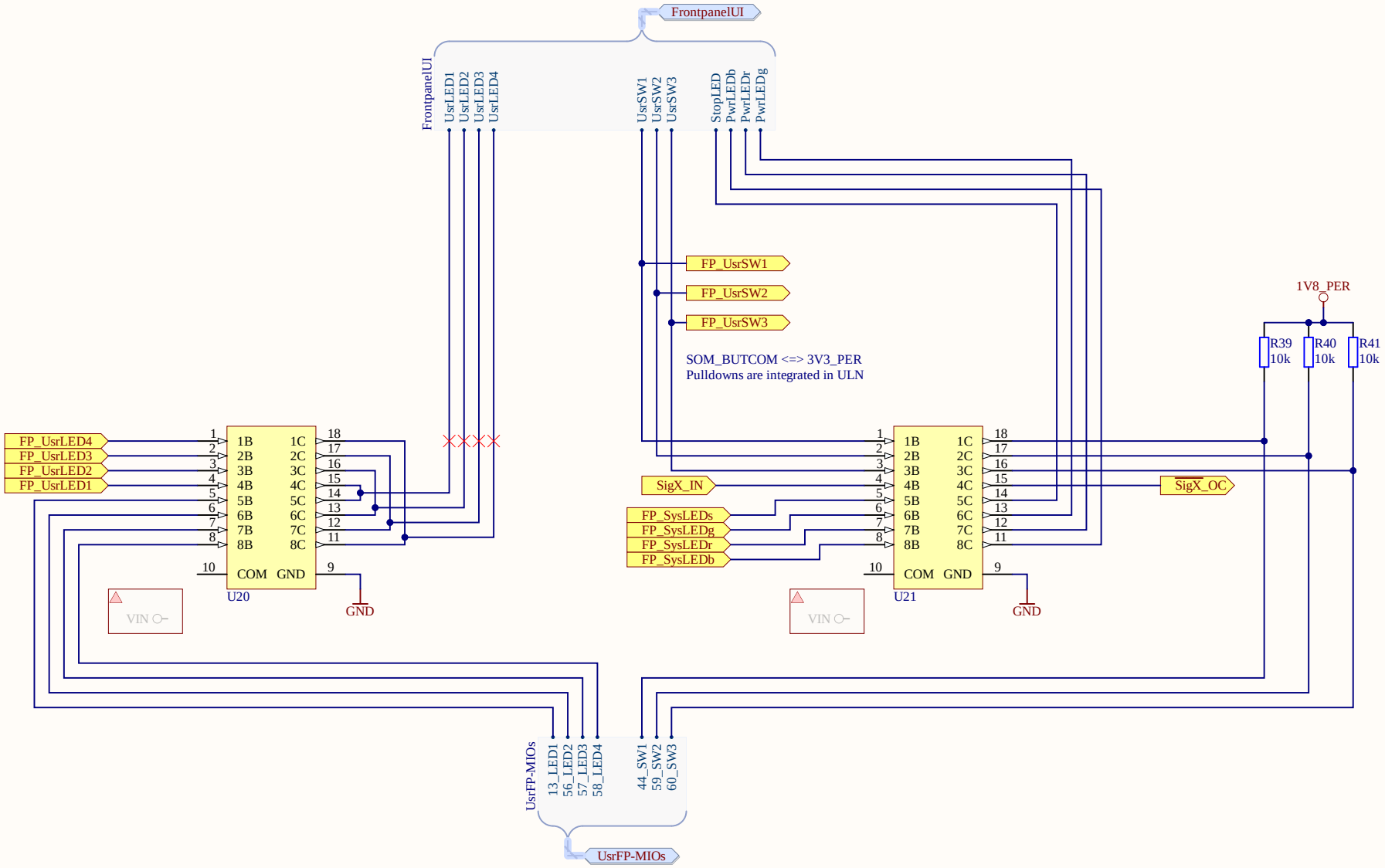

C112B
GND
100 pF
I2C
200R
R37B
S3CsI2C_SCL
I2C_SEC
SCL
SDA
100R
R38B
S3CsI2C_SDA
C113B
GND
100 pF
1V8_PER
U19B
BANK1
79 VCCIO1
88 VCCIO1
102 VCCIO1
Carrier_PG_1V8
107 PR2A/R_GPLLT_FB
106 PR2B/R_GPLLC_FB
S3CsI2C_SDA
S3CsI2C_SCL
105 PR3A/R_GPLLT_IN
104 PR3B/R_GPLLC_IN
FP_SysLEDs
SD1_CD
103 PR4C
SD0_CD
100 PR5A
99 PR5B
FP_UsrLED4
98 PR6A
FP_UsrLED3
97 PR6B
FP_UsrLED2
96 PR8A
FP_UsrLED1
95 PR8B
DIG_S3C.Shared.CarrierReady
94 PR9A
DIG_S3C.Shared.ReqSafeState
93 PR9B
DIG_S3C.SlotD1.ReqOE
92 PR10A/PCLKT1_0
DIG_S3C.SlotD1.SlotOK
91 PR10B/PCLKC1_0
DIG_S3C.SlotD2.ReqOE
89 PR10C
DIG_S3C.SlotD2.SlotOK
87 PR10D
DIG_S3C.SlotD3.ReqOE
86 PR13A
DIG_S3C.SlotD3.SlotOK
85 PR13B
DIG_S3C.SlotD4.ReqOE
84 PR14A
DIG_S3C.SlotD4.SlotOK
83 PR14B
DIG_S3C.SlotD5.ReqOE
82 PR15A
DIG_S3C.SlotD5.SlotOK
81 PR15B
DIG_S3C
DIG_S3C
5 78 PR16A
4 77 PR16B
2 76 PR18A
3 75 PR18B
1 74 PR19A
0 73 PR19B
FlexLIOs
FlexLIOs
LCMXO2-4000HC-4TG144C
1V8_PER
U19D
BANK3
30 VCCIO3
DIG5_S3C
03 25 PL16A
04 26 PL16B
05 27 PL17A/PCLKT3_0
00 28 PL17B/PCLKC3_0
02 31 PL18D
01 32 PL19A
29 33 PL19B
28 34 PL20A
27 35 PL20B
DIG5_S3C
LCMXO2-4000HC-4TG144C
NB: Function groups on this sheet are only available if(f) the system is switched on!
1V8_S3C
U19C
BANK2
37 VCCIO2
51 VCCIO2
66 VCCIO2
S3C_SPI
SPI_S3C
nCS_USR
MOSI
nCS_SYS
MISO
SCLK
26 38 PB3A
25 39 PB3B
24 40 PB4A/CSSPIN
41 PB4B
SD_SEL
ANL_VIN_FLT
42 PB7A
One spare I/O for SoM status
TP34
43 PB7B
44 PB9A/MCLK/CCLK
45 PB9B/SO/SPISO
FlexMIOs
52_PCIe-RST 47 PB10A
53_GPIO_PowerDown 48 PB10B
54_I2C0-SharedIRQ 49 PB13A/PCLKT2_0
61_ExternalSTOP 50 PB13B/PCLKC2_0
62_LWD/TTC0/UA0a 52 PB15A
63_LWD/TTC0/UA0b 54 PB15B
FlexMIOs
31_PMU-I5_SWp 55 PB20A/PCLKT2_1
30_DP-DRX 56 PB20B/PCLKC2_1
29_DP-DOE 57 PB21A
28_DP-HPD 58 PB21B
27_DP-DTX 59 PB23A
26_PMU-I0 60 PB23B
45_SD-CD 61 PB24A
37_SPI1-MOSI 62 PB24B
36_SPI1-MISO 63 PB24D
35_SPI1-nCS0 65 PB27A
34_SPI1-nCS1_PMU-O2 67 PB27B
33_SPI1-nCS2_PMU-O1 68 PB29A
32_SPI1_SCLK 69 PB29B
0R
S3CSPI_SN
R45
70 PB30A/SN
71 PB30B/SI/SISPI
LCMXO2-4000HC-4TG144C
3V3_S3C
U22
TPS780180300DRVR
IN
EN
NC
OUT
Vset/FB
GND PAD
C114
4.7 µF
GND
1V8_PER
0R
R43
1V8_S3C
0R
R44
C115
4.7 µF
GND
GND
Backup for bank 2 (SSPI/SN)
1V8_PER
U?
C?
100 nF
GND
VCCA
VCCB
A
B
GND
2N7001TDCKRQ1
R?
10k
GND
C?
100 nF
GND
Title S3C_IOs1V8.SchDoc
Revision: 05
Design Engineer: AG / EA / MG
Project: UZ_CarrierBoard.PrjPcb
UltraZohm
www.ultrazohm.com
Date: 14/12/2024
Sheet 10 of 60



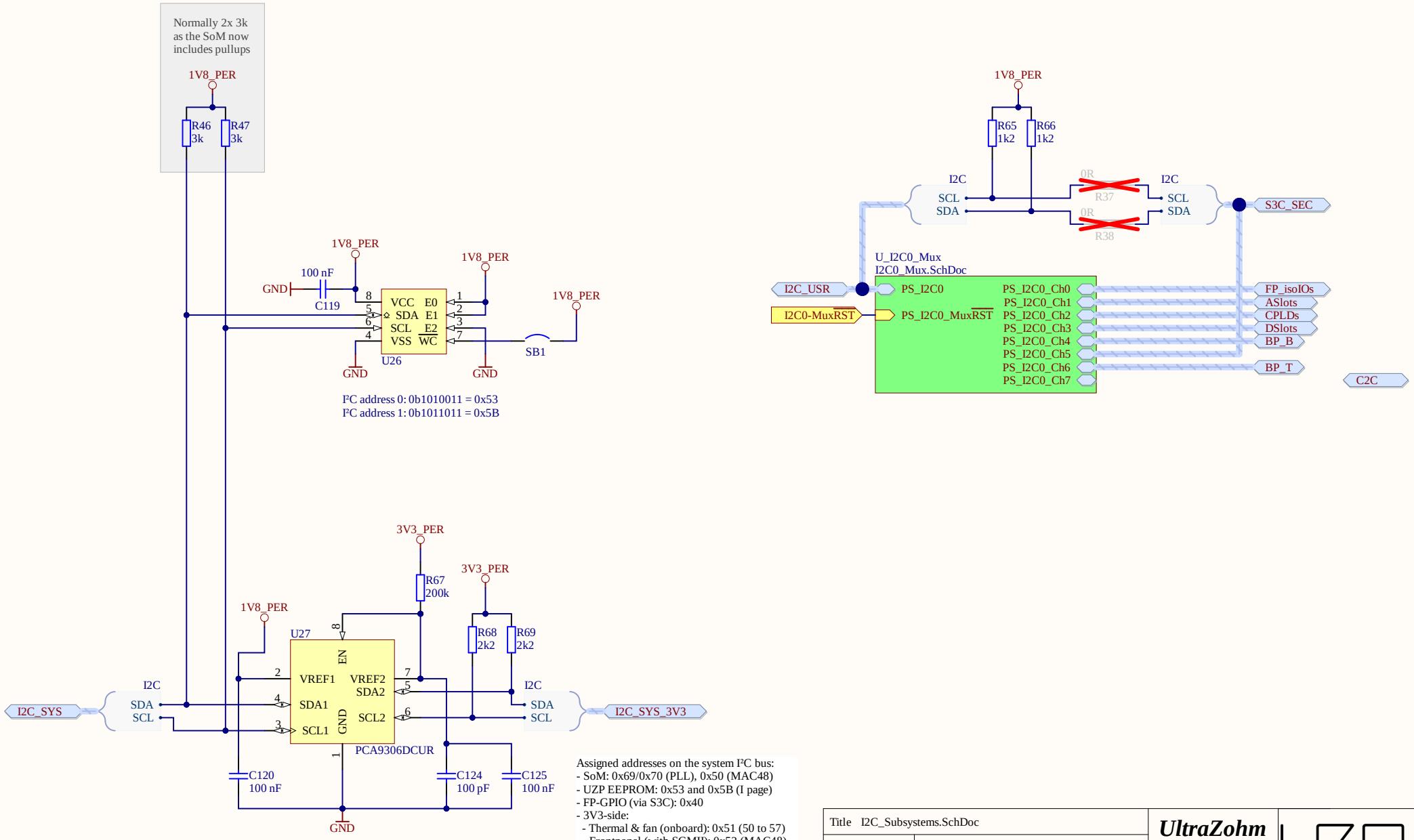
Title S3C_MuxJTAG.SchDoc		**UltraZohm**	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 11 of 60	



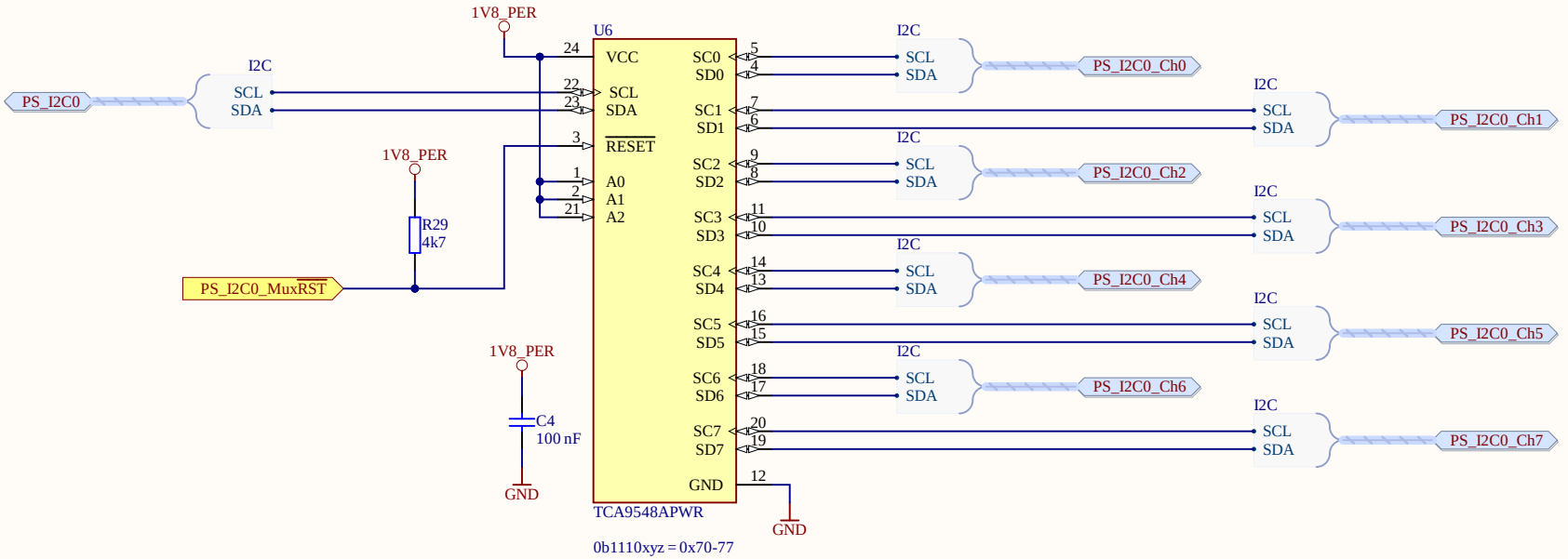
Title S3C_SplitSPI.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 12 of 60	



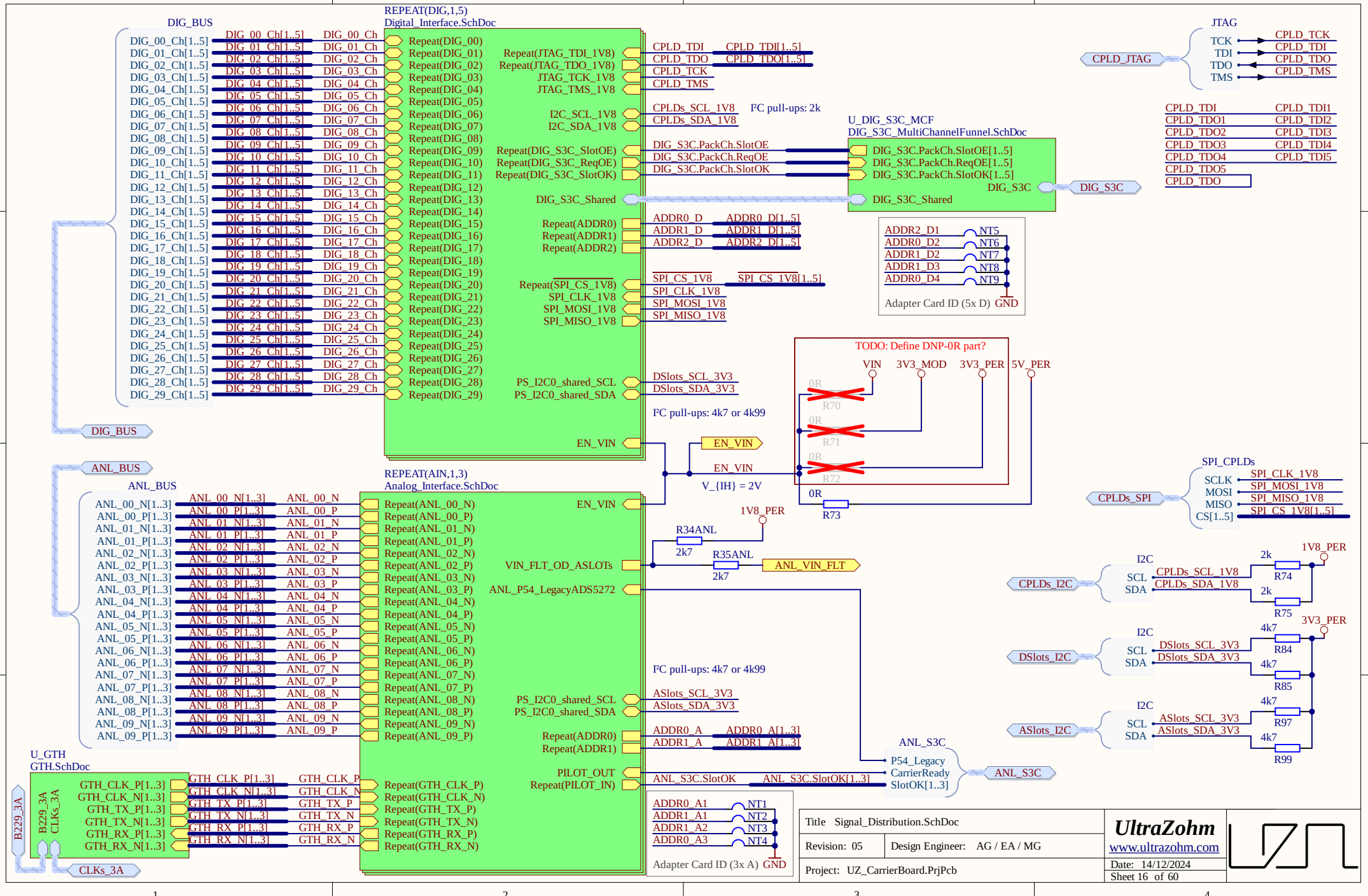
Title S3C_FrontpanelInterface.SchDoc		**UltraZohm** www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	Date: 14/12/2024
Project: UZ_CarrierBoard.PrjPcb		Sheet 13 of 60

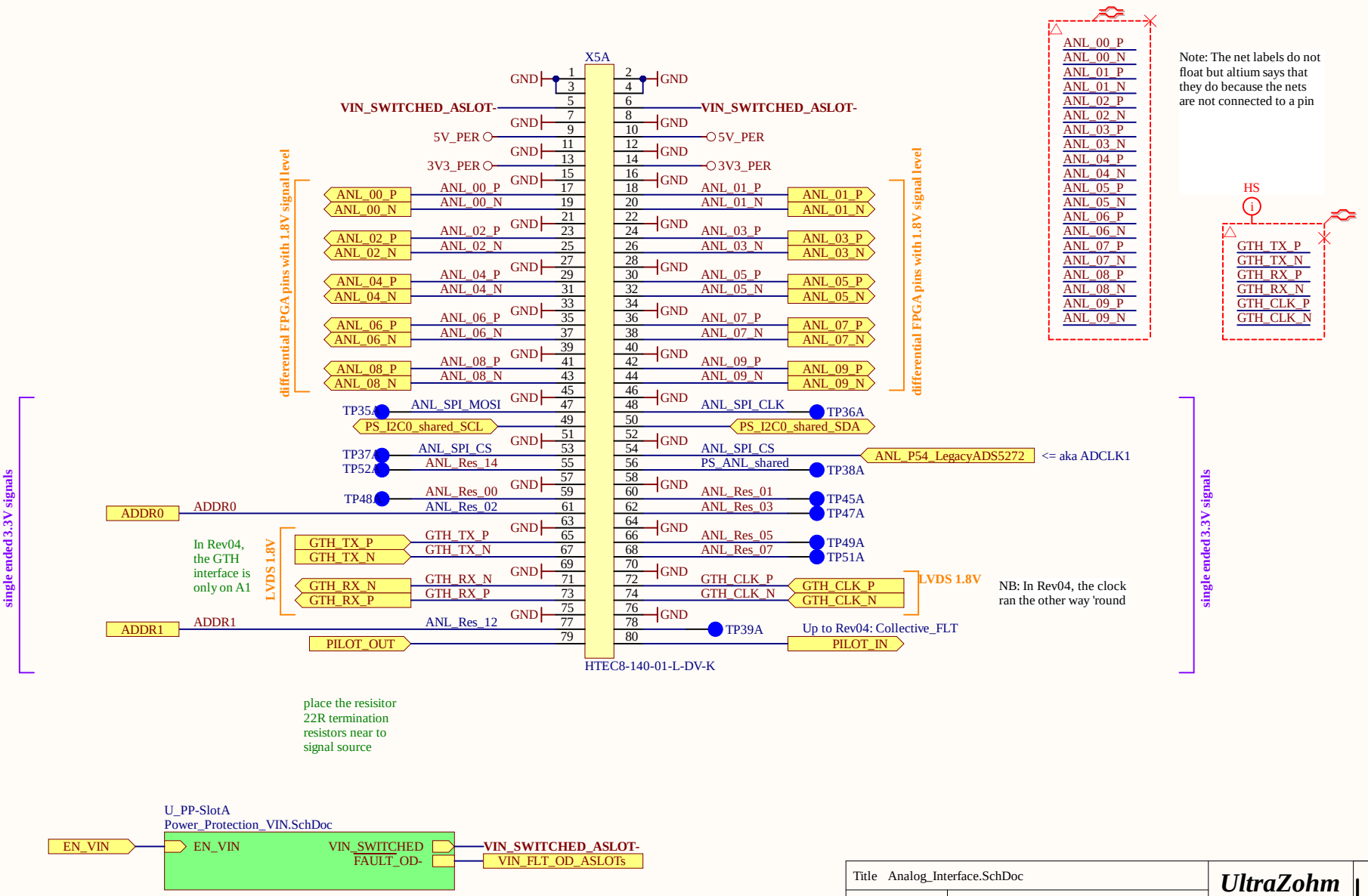


Title I2C_Subsystems.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	Date: 14/12/2024
Project: UZ_CarrierBoard.PrjPcb		Sheet 14 of 60

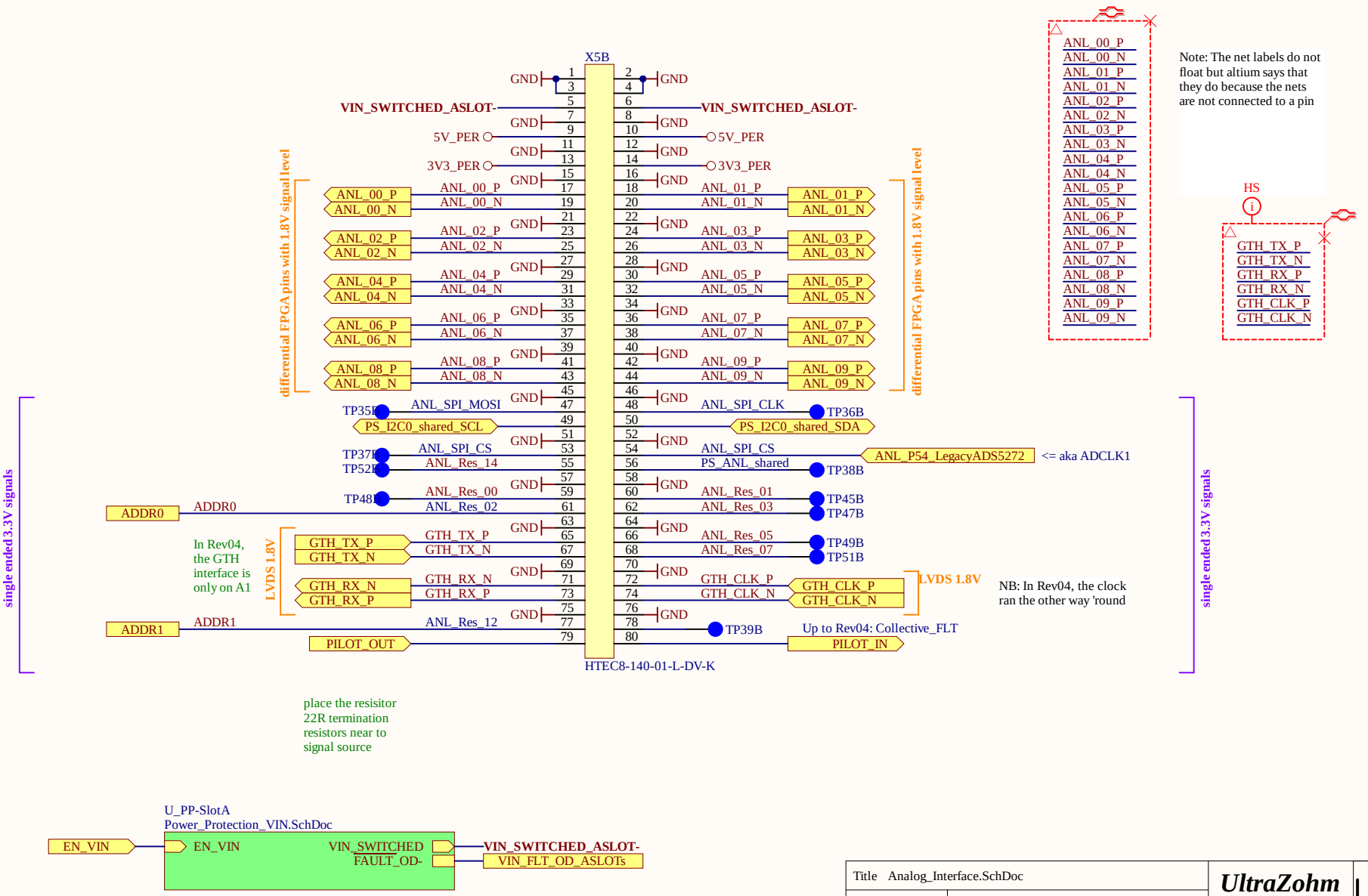


Title I2C0_Mux.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 15 of 60	

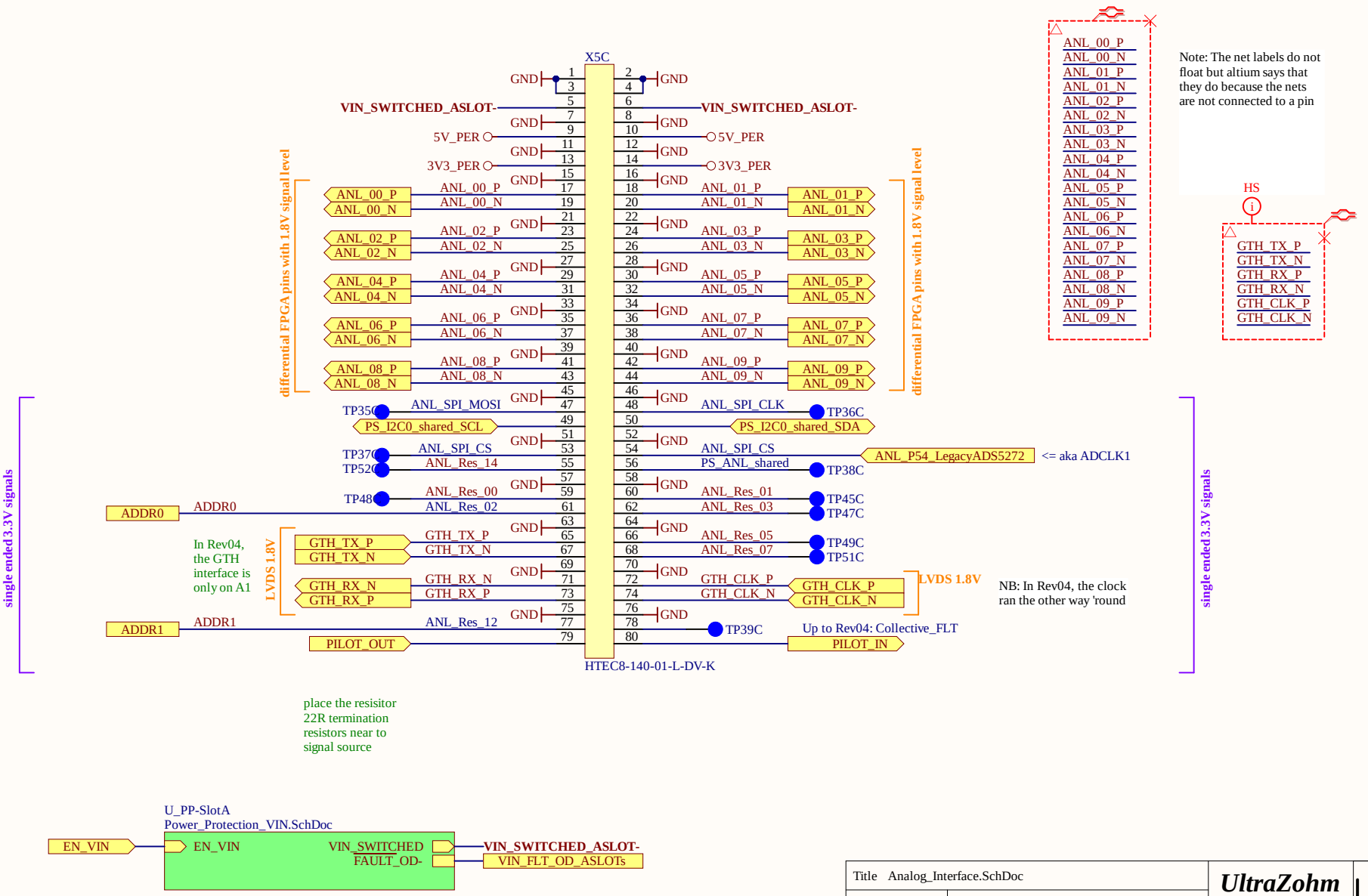

DIG_BUS
REPEAT(DIG,1,5)
Digital_Interface.SchDoc
JTAG
CPLD_JTAG
TCK
TDI
TDO
TMS
CPLD_TCK
CPLD_TDI
CPLD_TDO
CPLD_TMS
I²C pull-ups: 2k
CPLDs_SCL_1V8
CPLDs_SDA_1V8
U_DIG_S3C_MCF
DIG_S3C_MultiChannelFunnel.SchDoc
DIG_S3C.PackCh.SlotOE
DIG_S3C.PackCh.ReqOE
DIG_S3C.PackCh.SlotOK
DIG_S3C_Shared
DIG_S3C
CPLD_TDI1
CPLD_TDI2
CPLD_TDI3
CPLD_TDI4
CPLD_TDI5
CPLD_TDO1
CPLD_TDO2
CPLD_TDO3
CPLD_TDO4
CPLD_TDO5
ADDR0_D
ADDR1_D
ADDR2_D
SPI_CS_1V8
SPI_CLK_1V8
SPI_MOSI_1V8
SPI_MISO_1V8
ADDR2_D1
ADDR0_D2
ADDR1_D2
ADDR1_D3
ADDR0_D4
NT5
NT6
NT7
NT8
NT9
Adapter Card ID (5x D)
GND
TODO: Define DNP-0R part?
VIN
3V3_MOD
3V3_PER
5V_PER
R70
R71
R72
R73
0R
PS_I2C0_shared_SCL
PS_I2C0_shared_SDA
DSlots_SCL_3V3
DSlots_SDA_3V3
I²C pull-ups: 4k7 or 4k99
EN_VIN
V_{IH} = 2V
ANL_BUS
REPEAT(AIN,1,3)
Analog_Interface.SchDoc
1V8_PER
R34ANL
R35ANL
2k7
VIN_FLT_OD_ASLOTs
ANL_VIN_FLT
ANL_P54_LegacyADS5272
SPI_CPLDs
CPLDs_SPI
SCLK
MOSI
MISO
CS[1..5]
I2C
CPLDs_I2C
DSlots_I2C
ASlots_I2C
SCL
SDA
R74
R75
R84
R85
R97
R99
2k
4k7
3V3_PER
ASlots_SCL_3V3
ASlots_SDA_3V3
ADDR0_A
ADDR1_A
PILOT_OUT
ANL_S3C.SlotOK
ANL_S3C
P54_Legacy
CarrierReady
SlotOK[1..3]
U_GTH
GTH.SchDoc
GTH_CLK_P[1..3]
GTH_CLK_N[1..3]
GTH_TX_P[1..3]
GTH_TX_N[1..3]
GTH_RX_P[1..3]
GTH_RX_N[1..3]
B229_3A
CLKs_3A
ADDR0_A1
ADDR1_A1
ADDR1_A2
ADDR0_A3
NT1
NT2
NT3
NT4
Adapter Card ID (3x A)
Title Signal_Distribution.SchDoc
Revision: 05
Design Engineer: AG / EA / MG
Project: UZ_CarrierBoard.PrjPcb
UltraZohm
www.ultrazohm.com
Date: 14/12/2024
Sheet 16 of 60



Title Analog_Interface.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 17.1of 60	

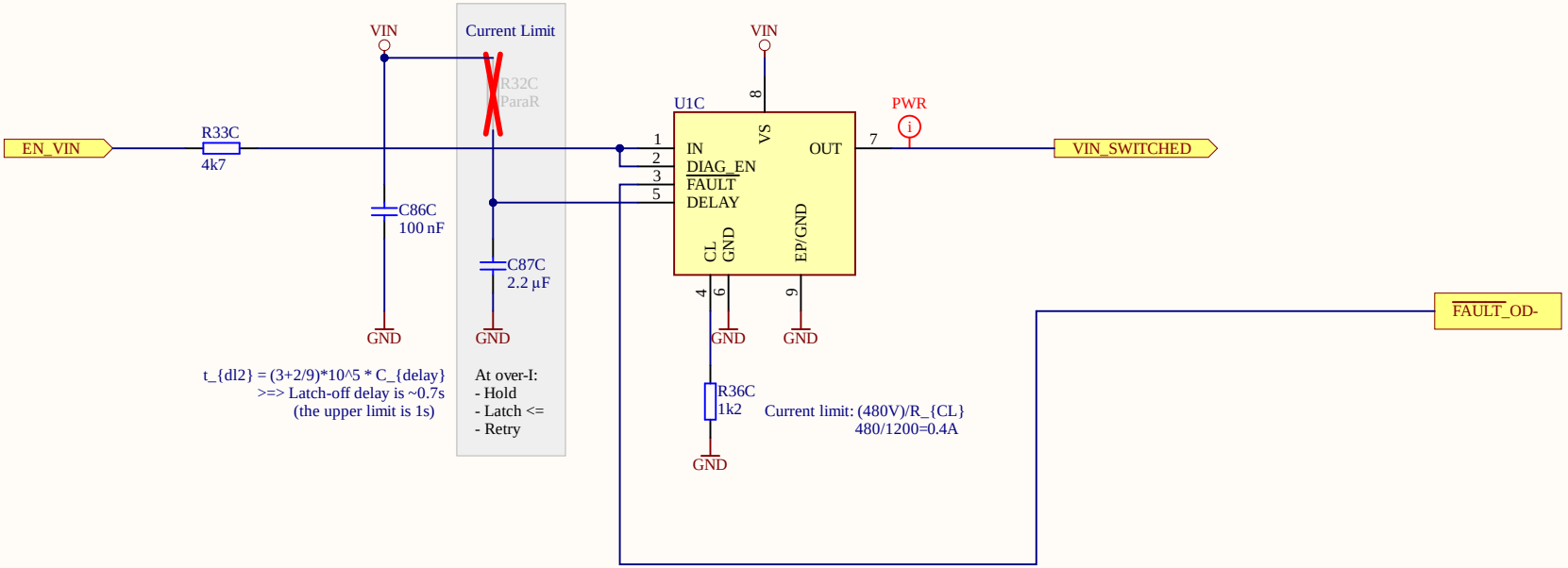


Title Analog_Interface.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 17.2 of 60	



Title Analog_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024 Sheet 17.3of 60

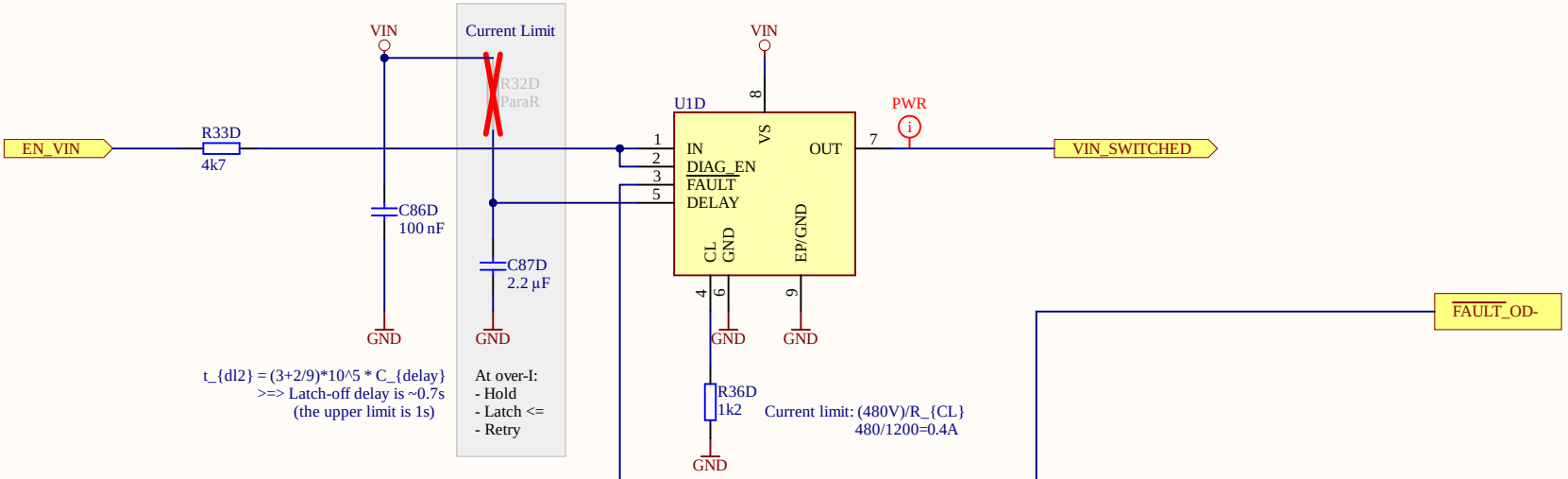
TODO Rev06: Rename ChaClass



I(off) is in the µA range if IN=DIAG_EN=0

Title Power_Protection_VIN.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 17 of 60	

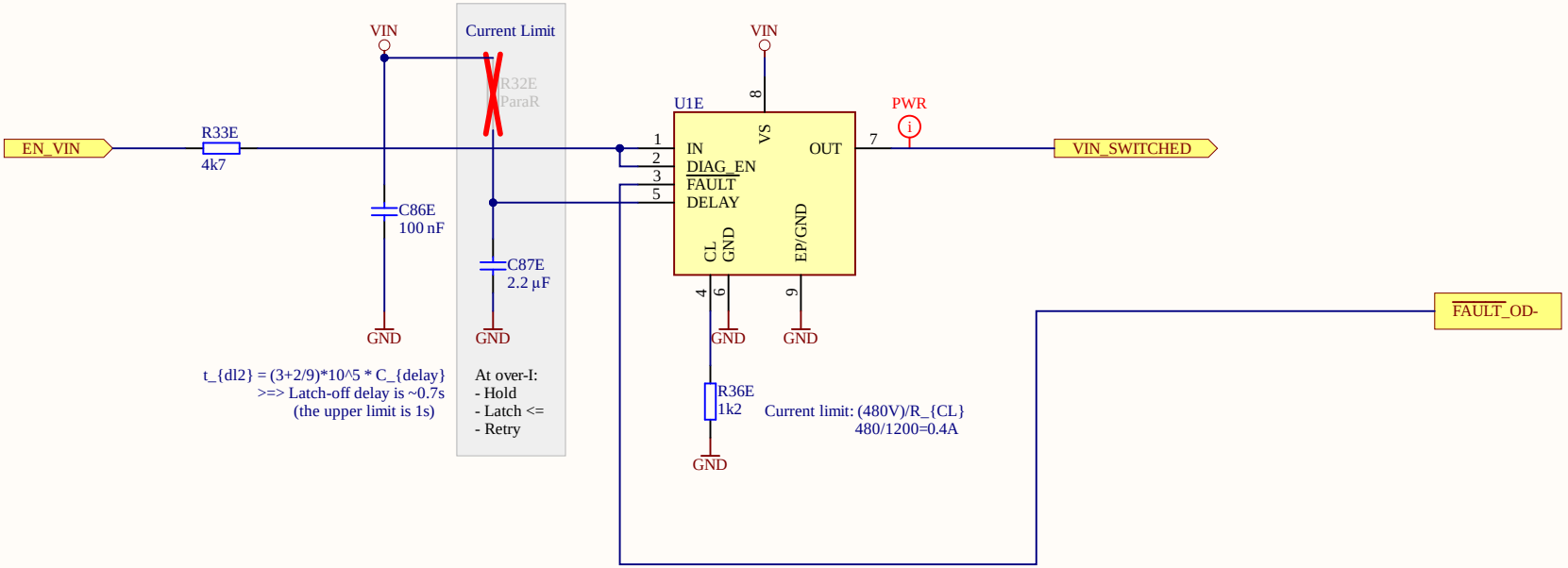
TODO Rev06: Rename ChaClass



I(off) is in the µA range if IN=DIAG_EN=0

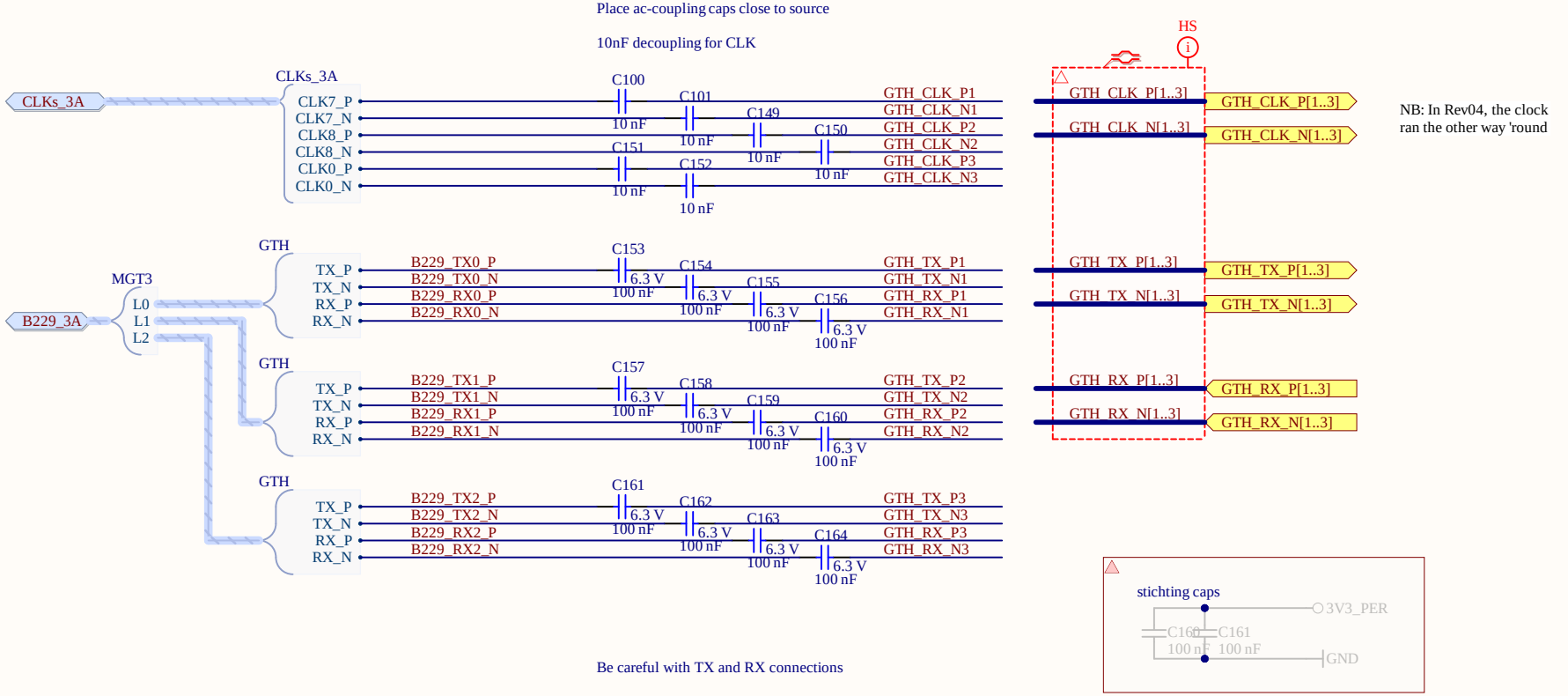
Title Power_Protection_VIN.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 17 of 60	

TODO Rev06: Rename ChaClass

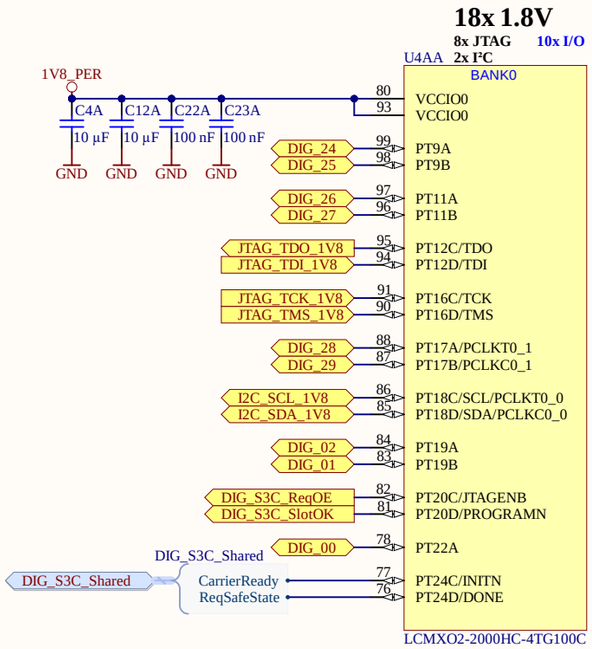


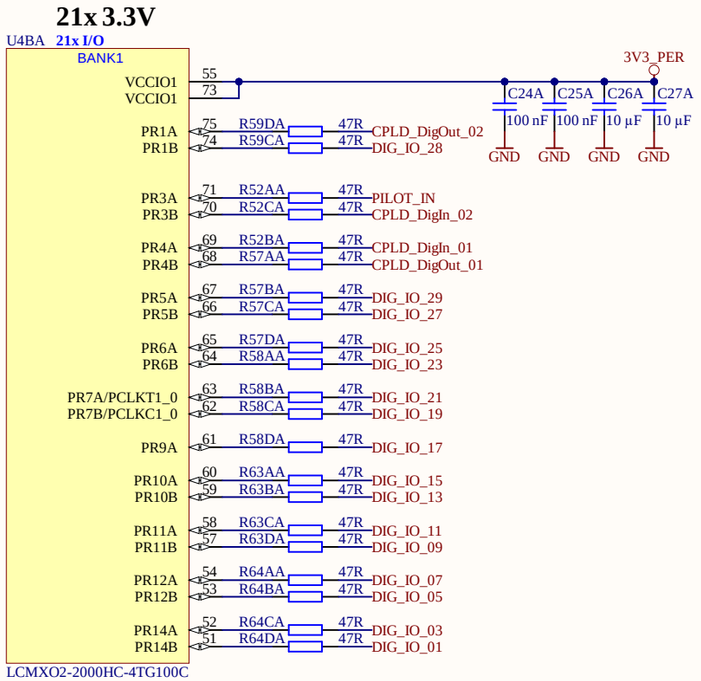
I(off) is in the µA range if IN=DIAG_EN=0

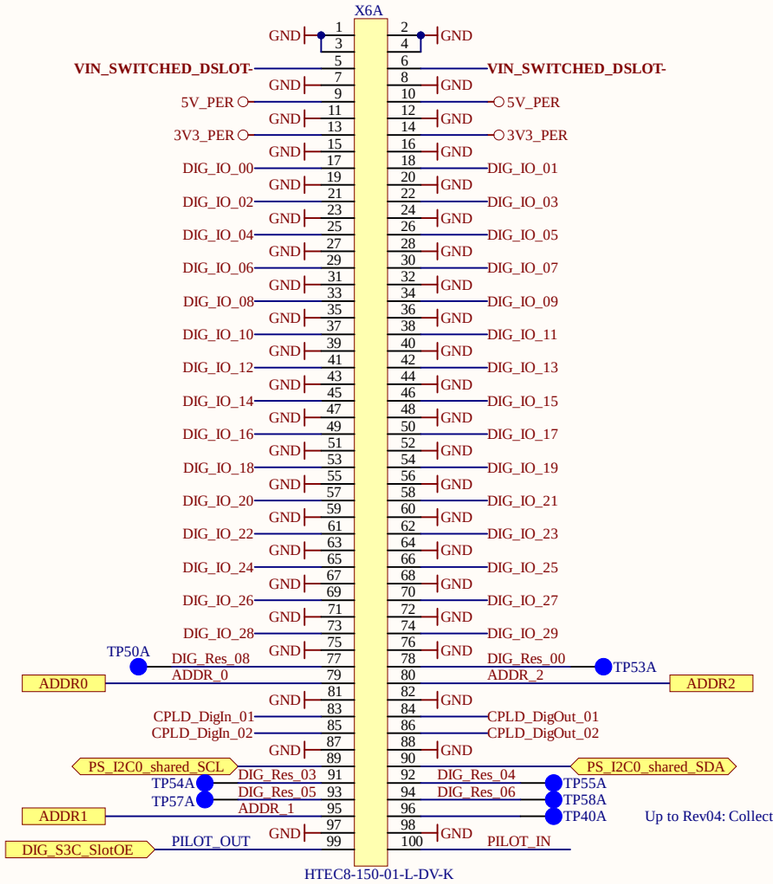
Title Power_Protection_VIN.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 17.3of 60	

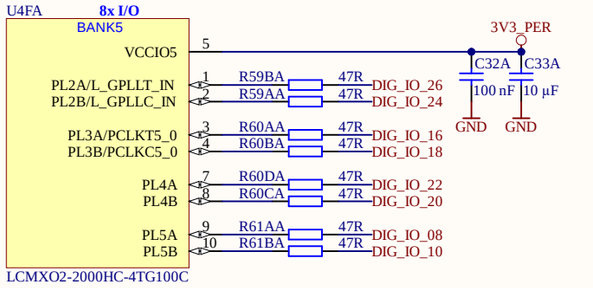


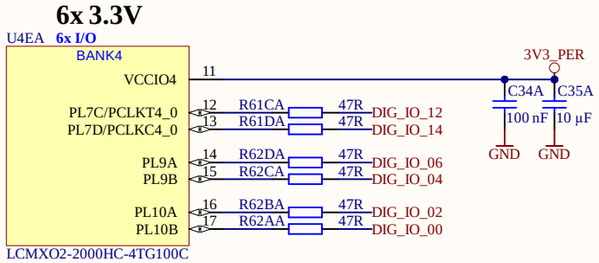
Title GTH.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 18 of 60	



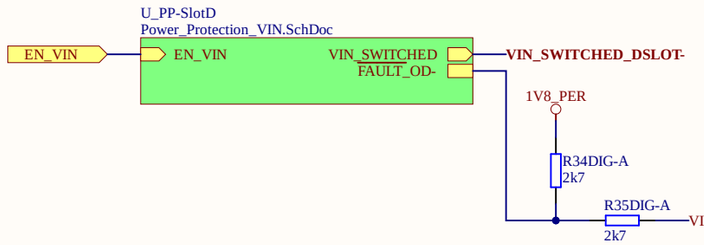




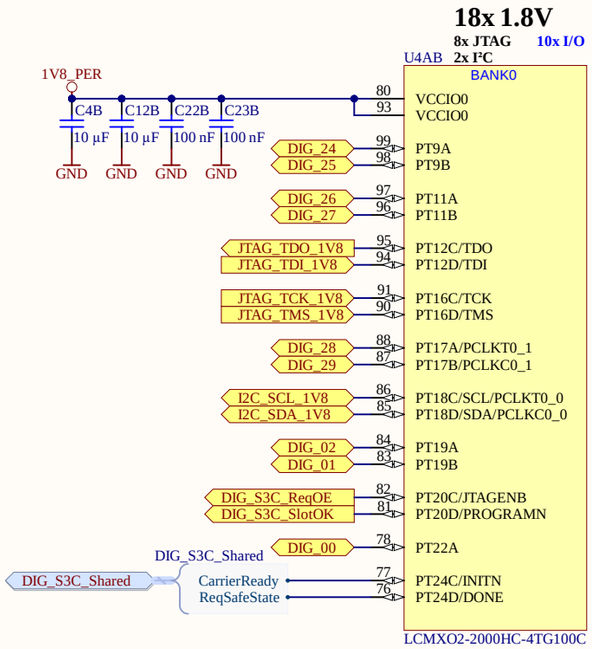


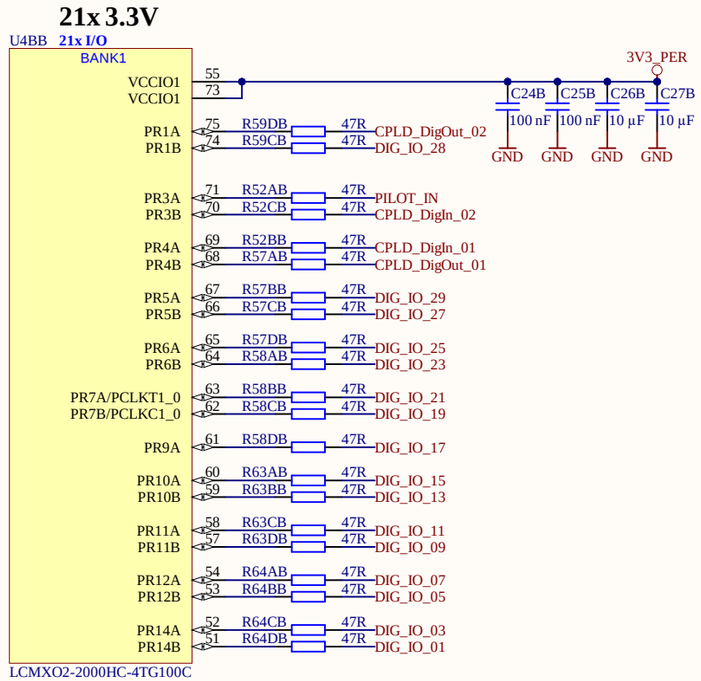


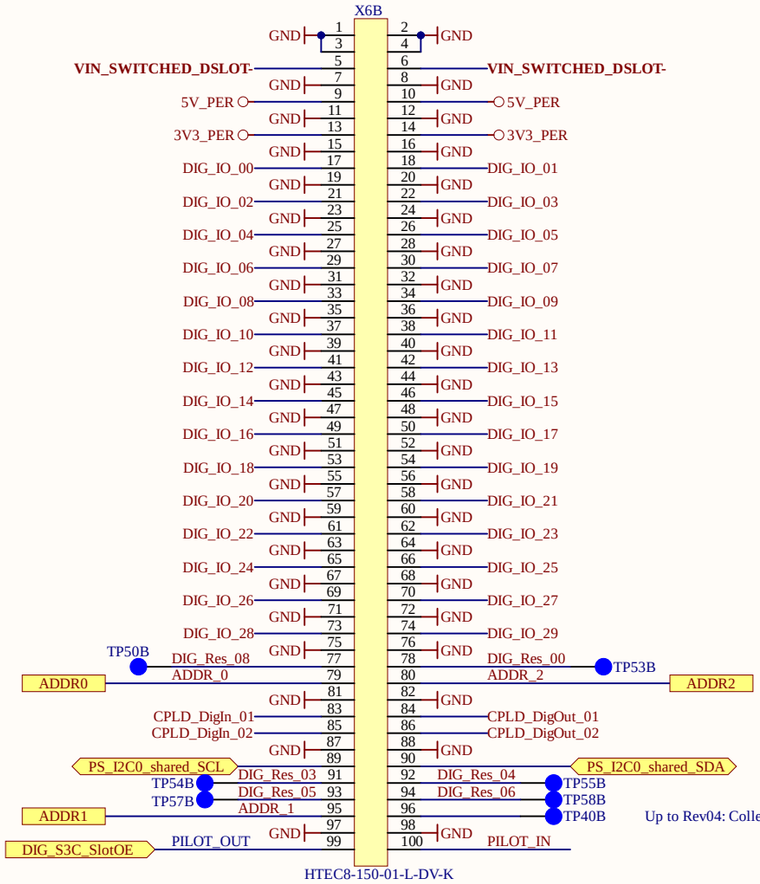
VIN for slot switched by System Controller

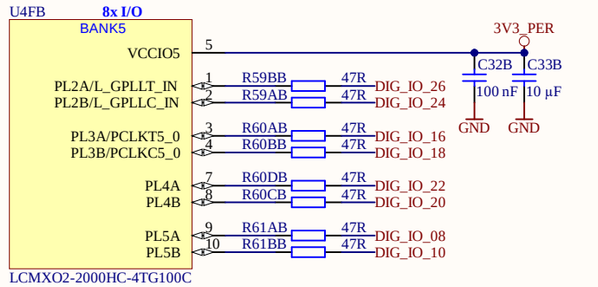


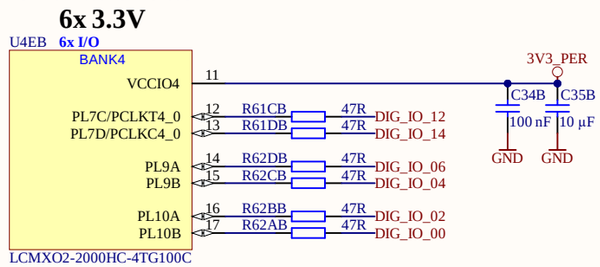
Title Digital_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	Date: 14/12/2024
Project: UZ_CarrierBoard.PrjPcb		Sheet 19.1of 60

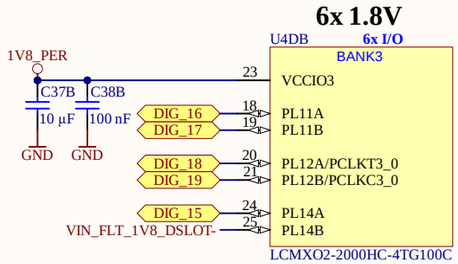


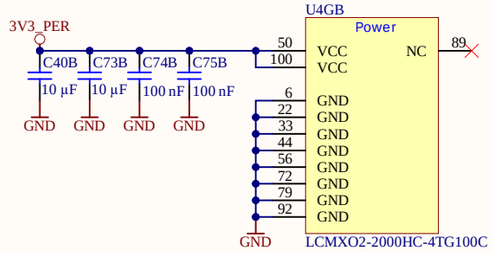


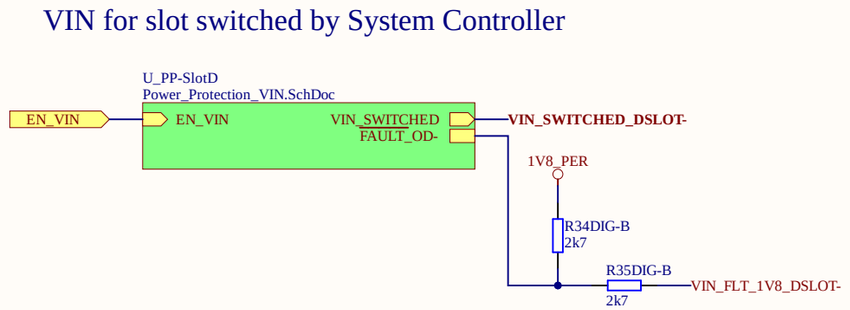




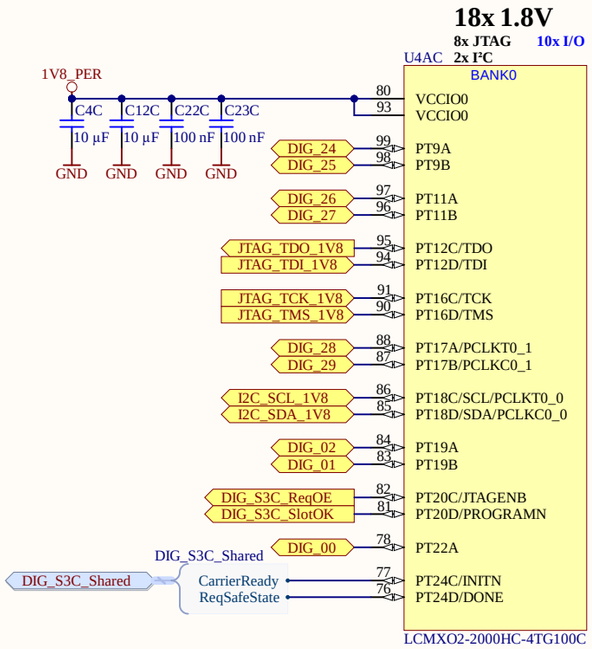


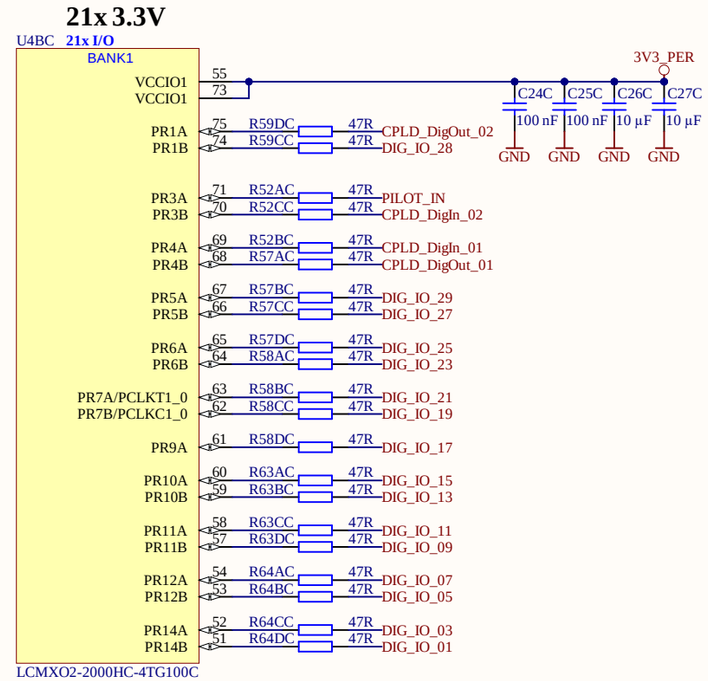


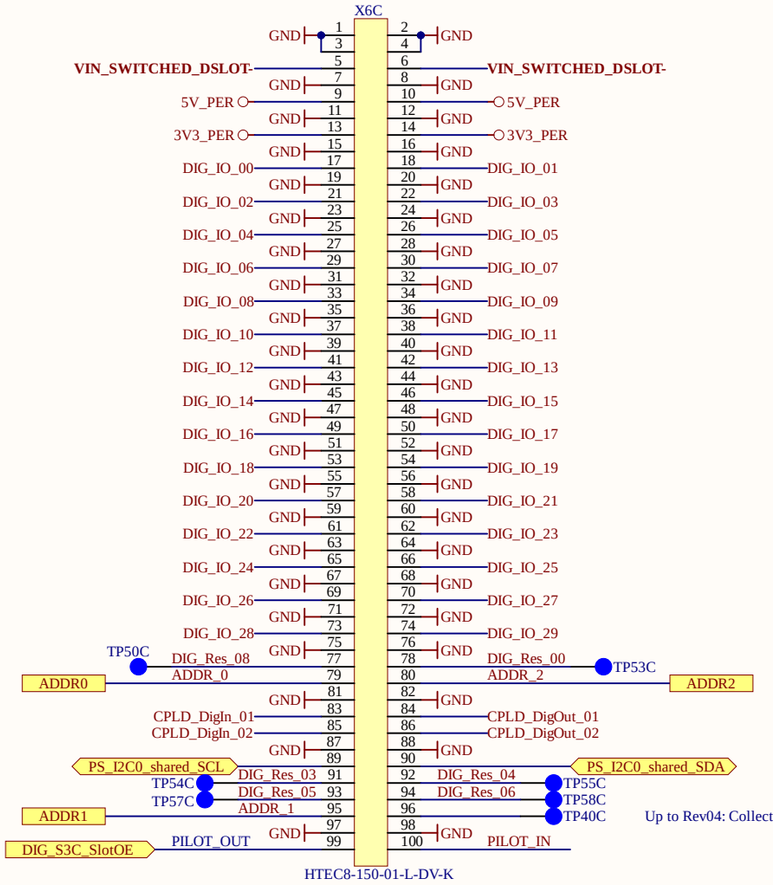


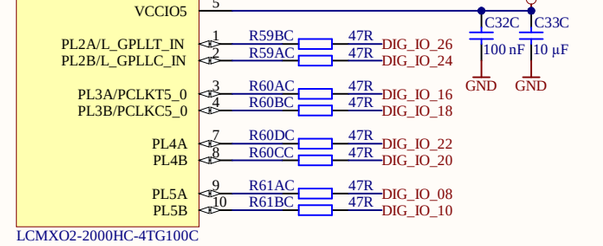


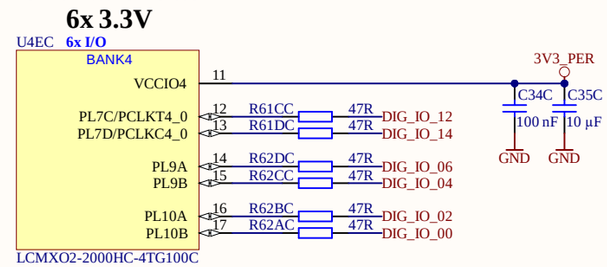
Title Digital_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	Date: 14/12/2024
Project: UZ_CarrierBoard.PrjPcb		Sheet 19 of 60

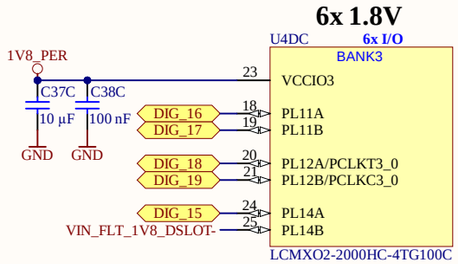


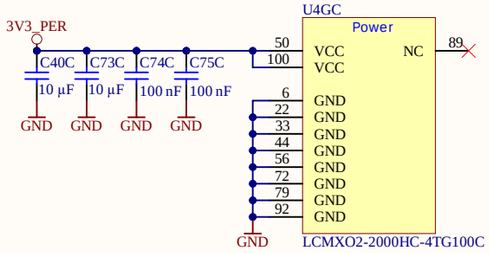




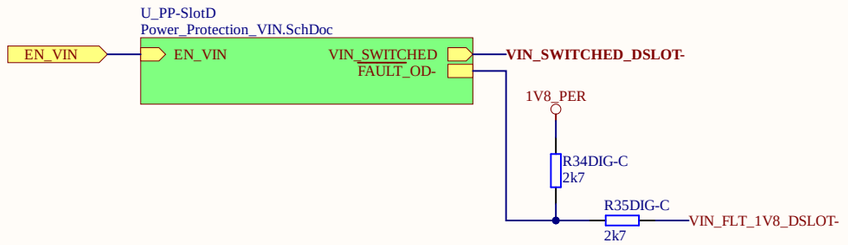




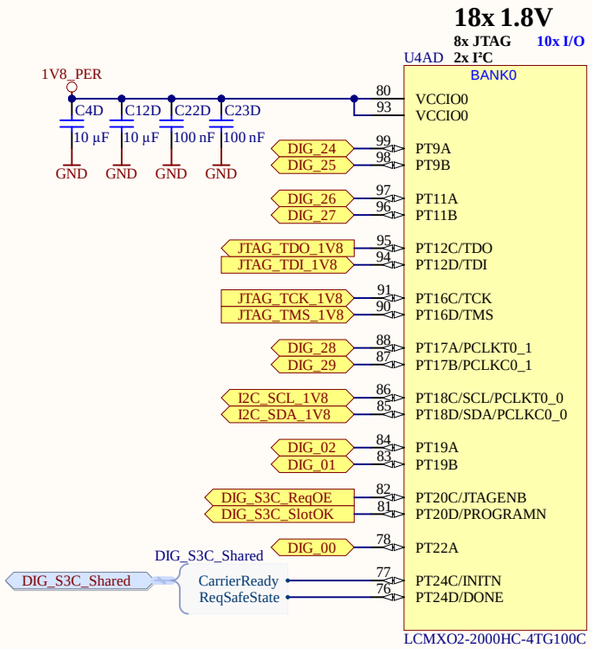


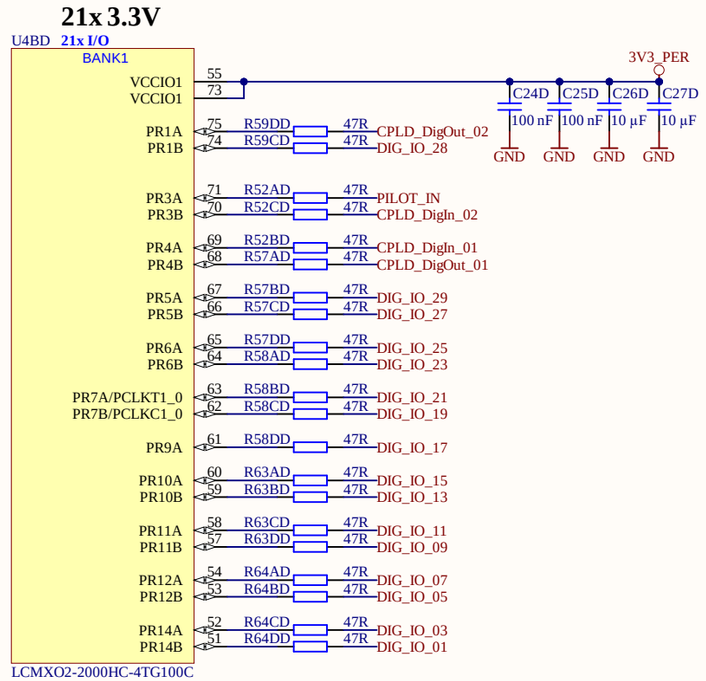


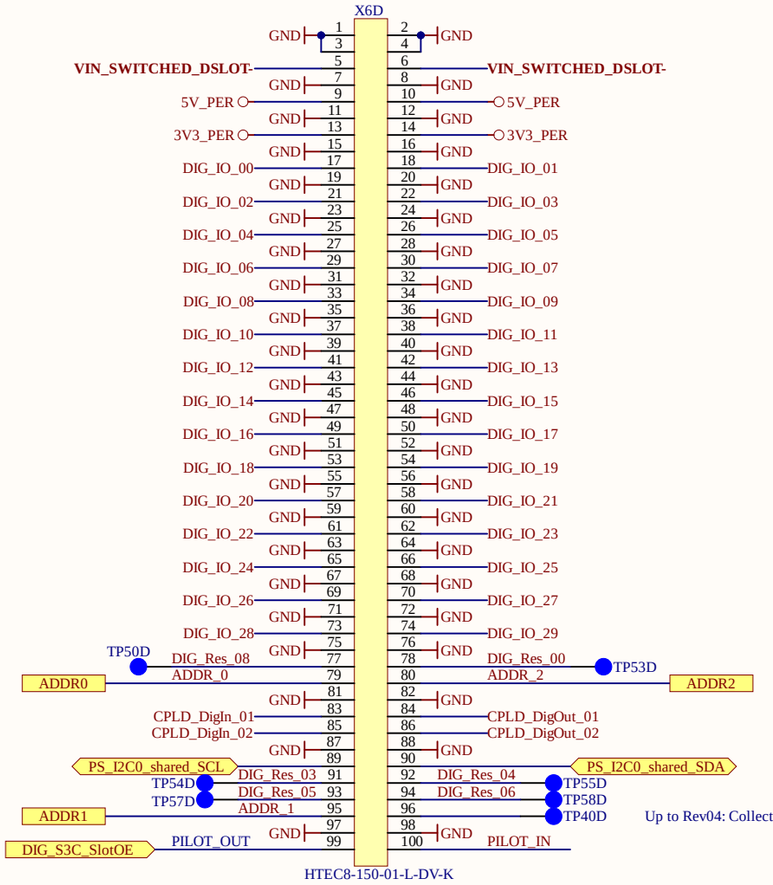
VIN for slot switched by System Controller

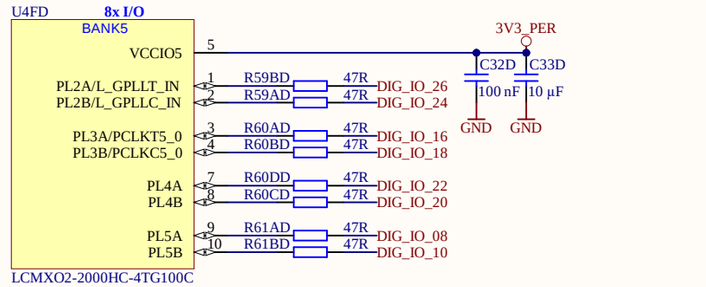


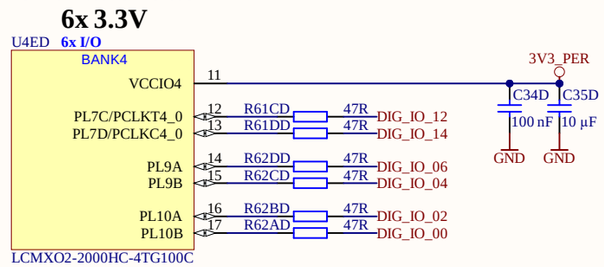
Title Digital_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	Date: 14/12/2024
Project: UZ_CarrierBoard.PrjPcb		Sheet 19 of 60

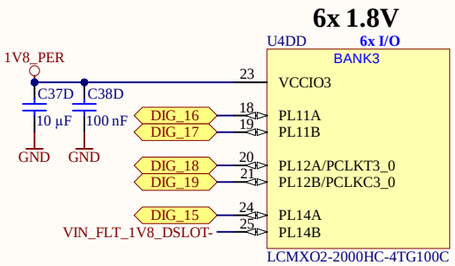


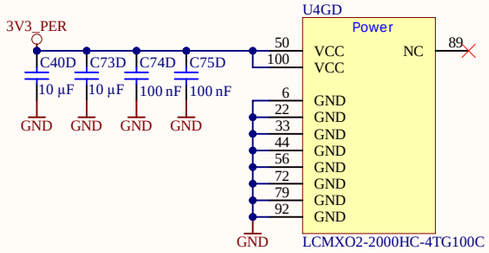




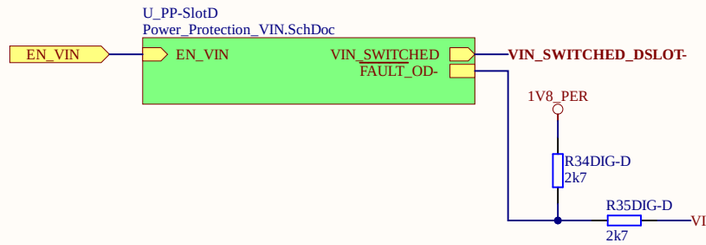




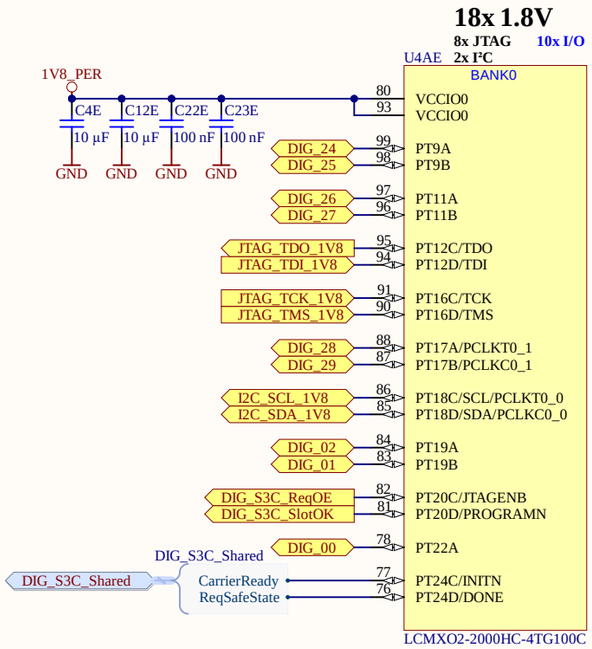


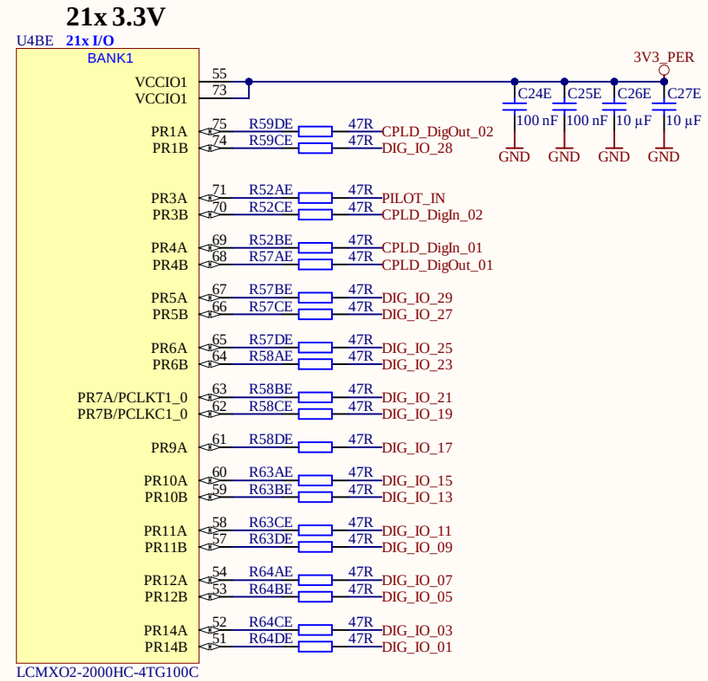


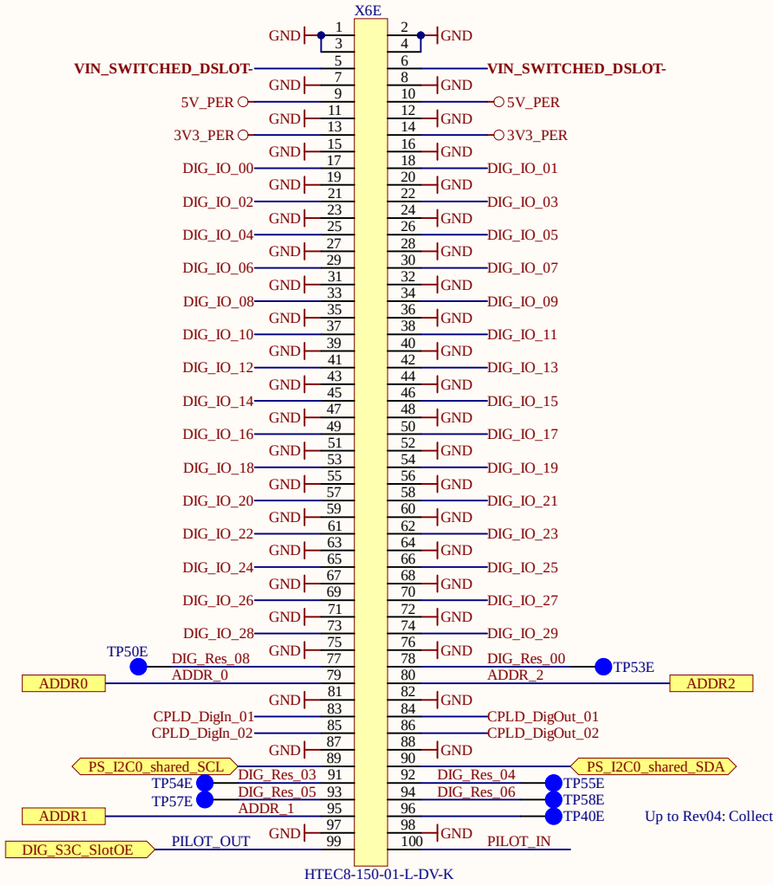
VIN for slot switched by System Controller

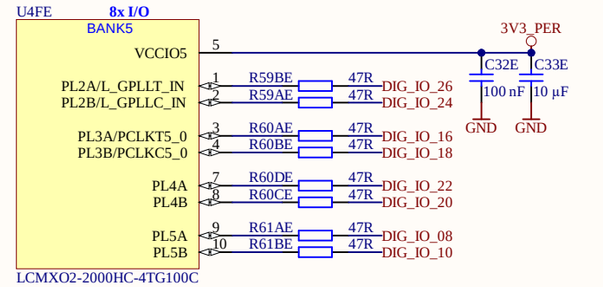


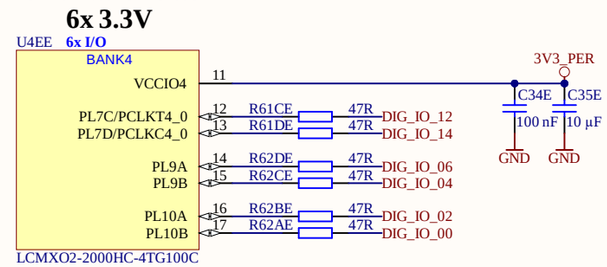
Title Digital_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	Date: 14/12/2024
Project: UZ_CarrierBoard.PrjPcb		Sheet 19.4of 60

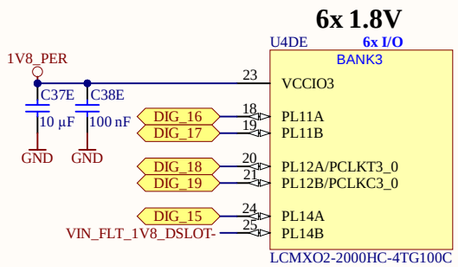


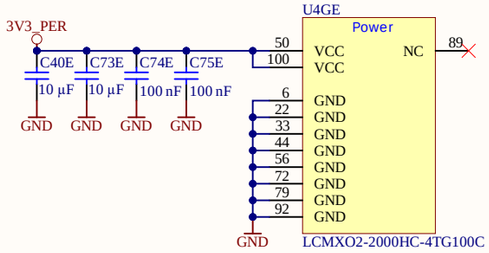




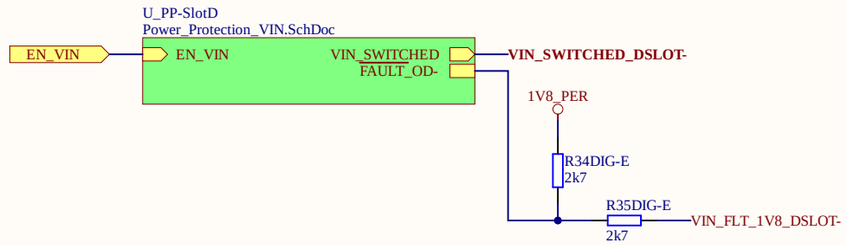






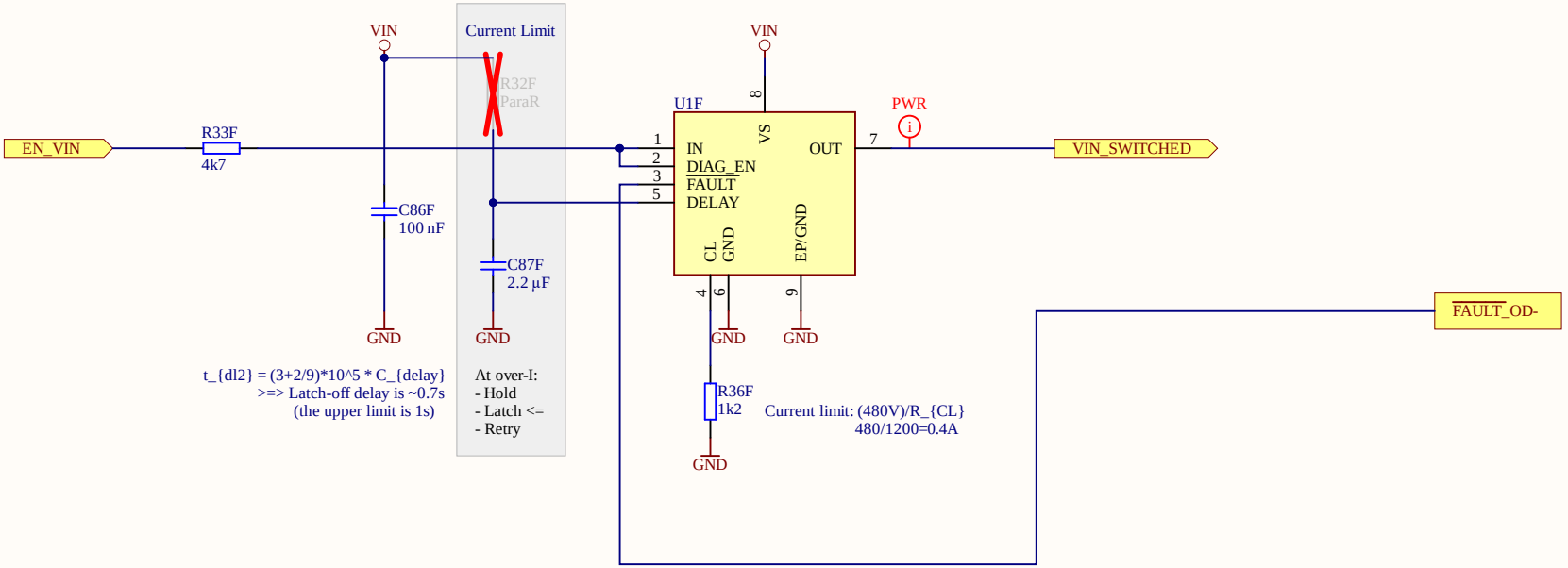


VIN for slot switched by System Controller



Title Digital_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	Date: 14/12/2024
Project: UZ_CarrierBoard.PrjPcb		Sheet 19.5of 60

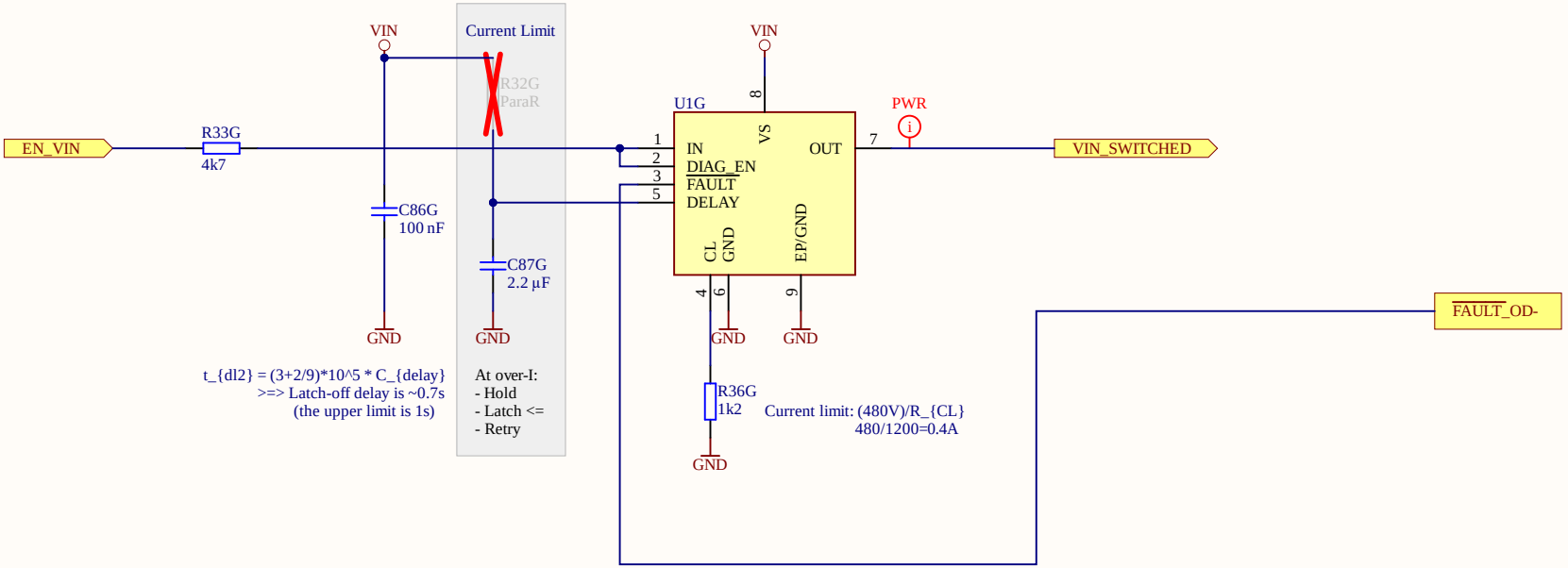
TODO Rev06: Rename ChaClass



I(off) is in the µA range if IN=DIAG_EN=0

Title Power_Protection_VIN.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 19 of 60	

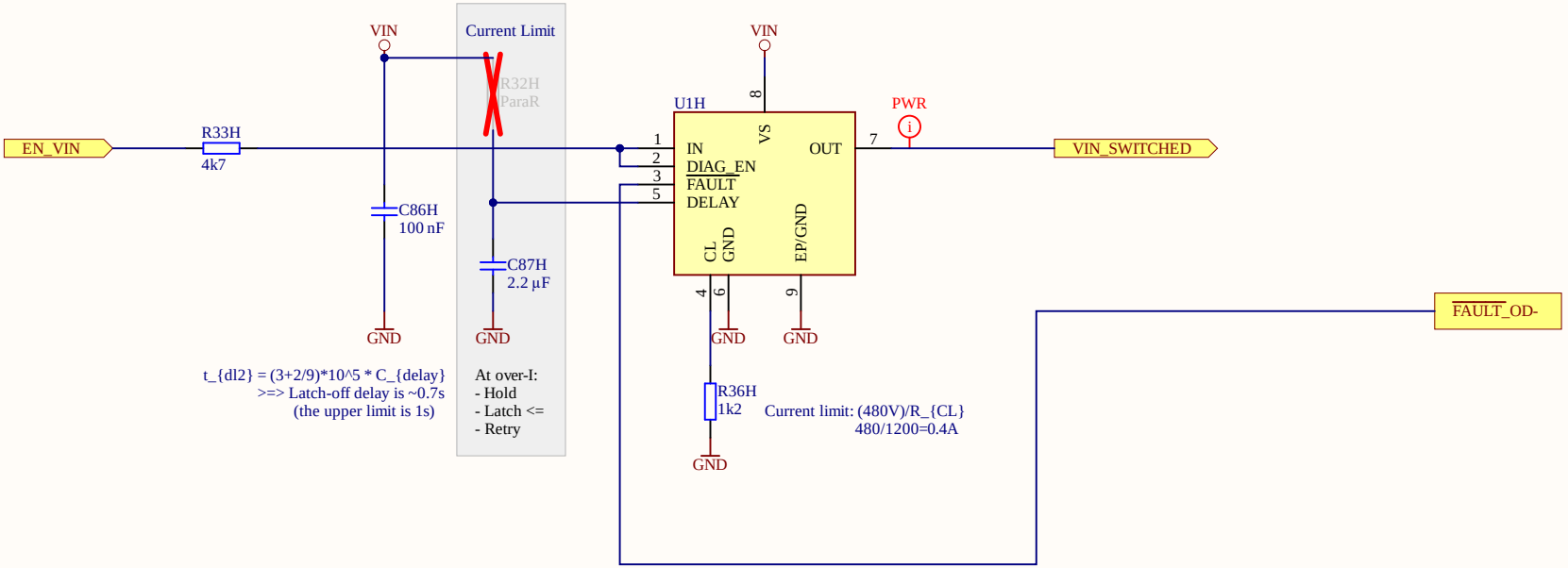
TODO Rev06: Rename ChaClass



I(off) is in the µA range if IN=DIAG_EN=0

Title Power_Protection_VIN.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 19 of 60	

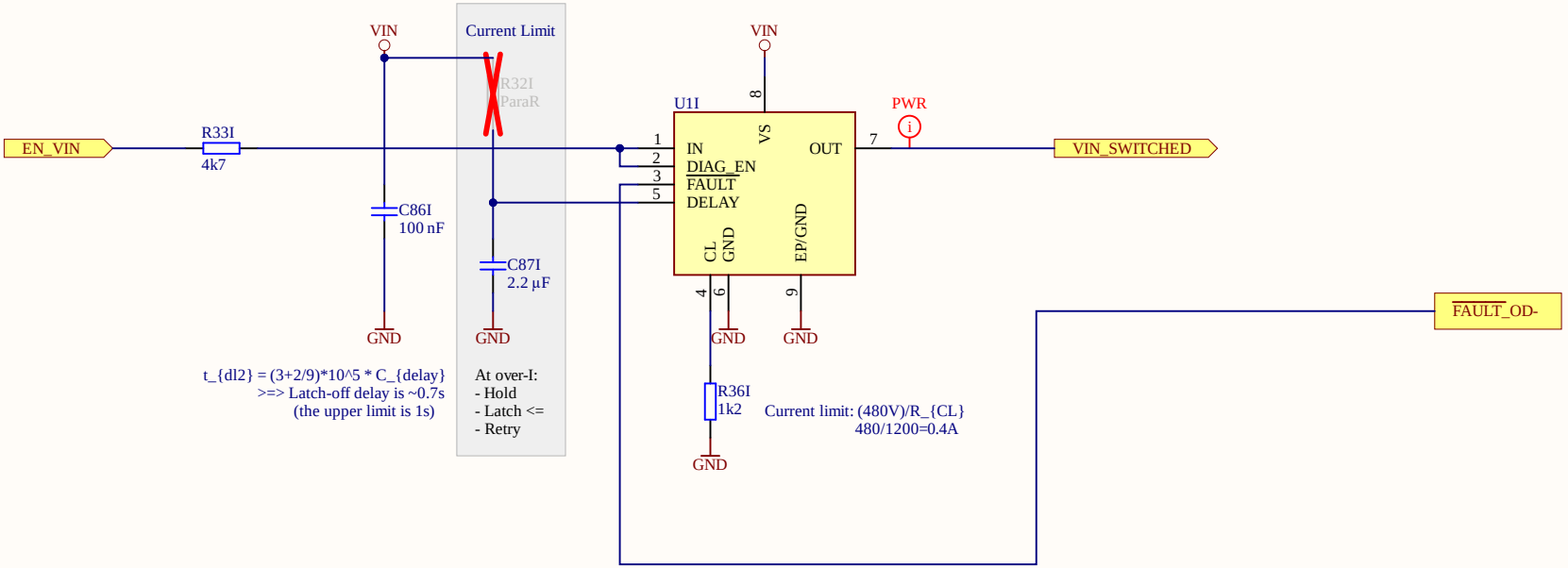
TODO Rev06: Rename ChaClass



I(off) is in the µA range if IN=DIAG_EN=0

Title Power_Protection_VIN.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 19.3 of 60	

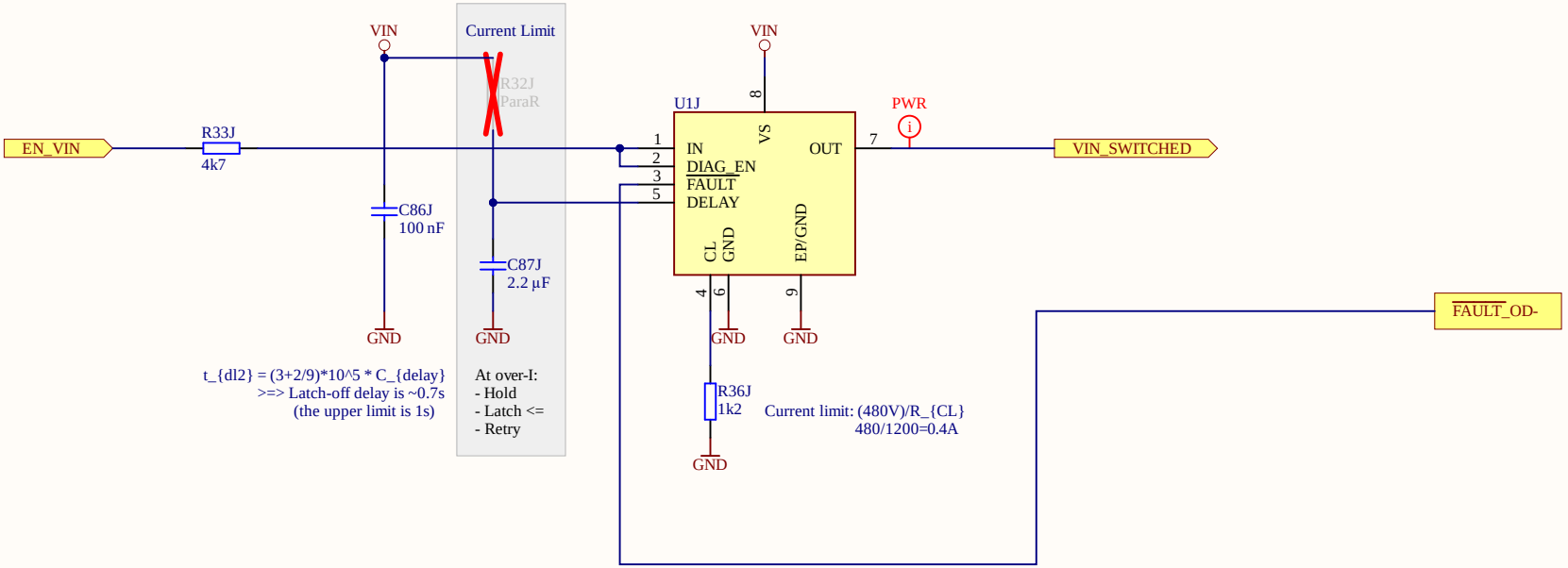
TODO Rev06: Rename ChaClass



I(off) is in the µA range if IN=DIAG_EN=0

Title Power_Protection_VIN.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 19.4 of 60	

TODO Rev06: Rename ChaClass



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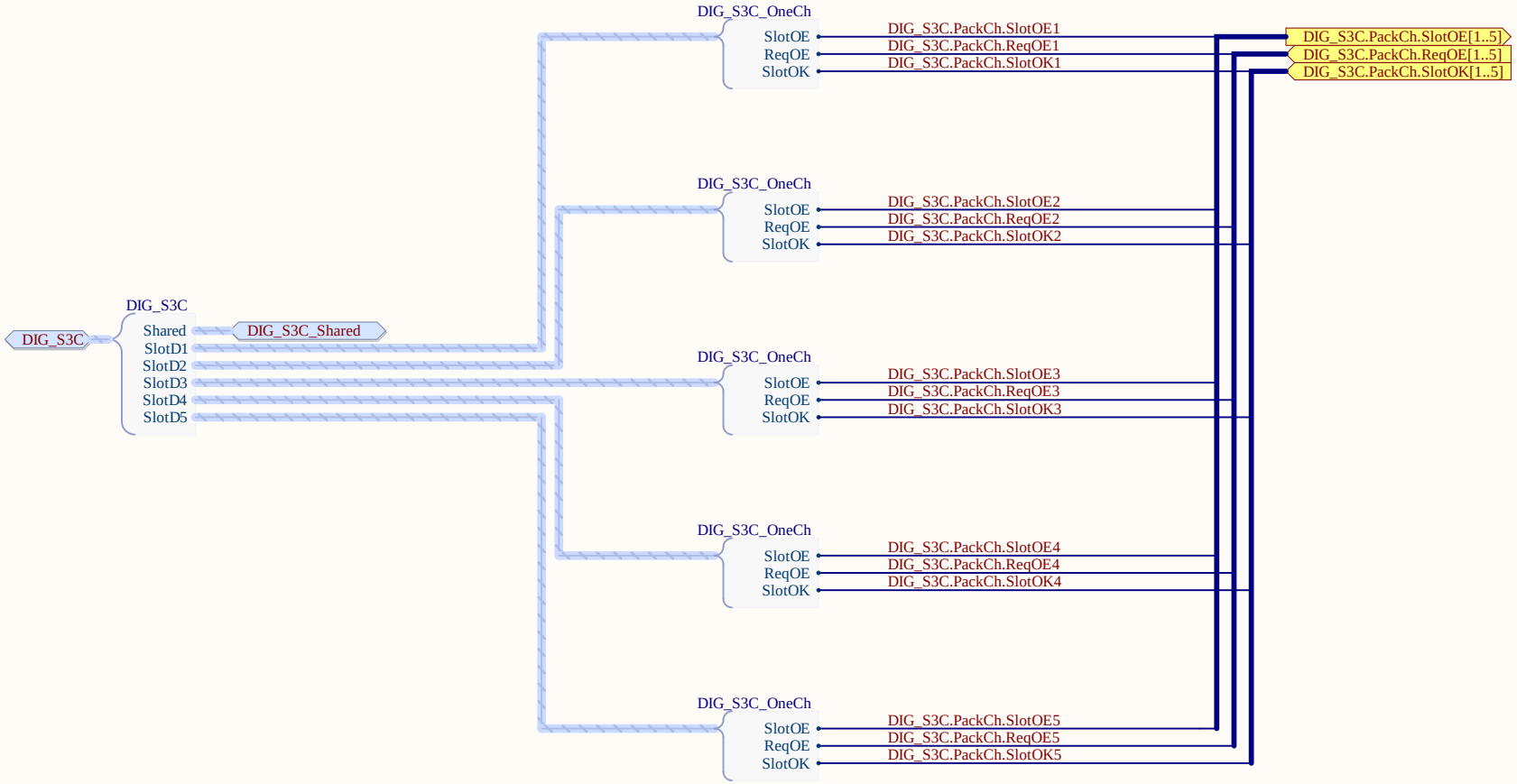
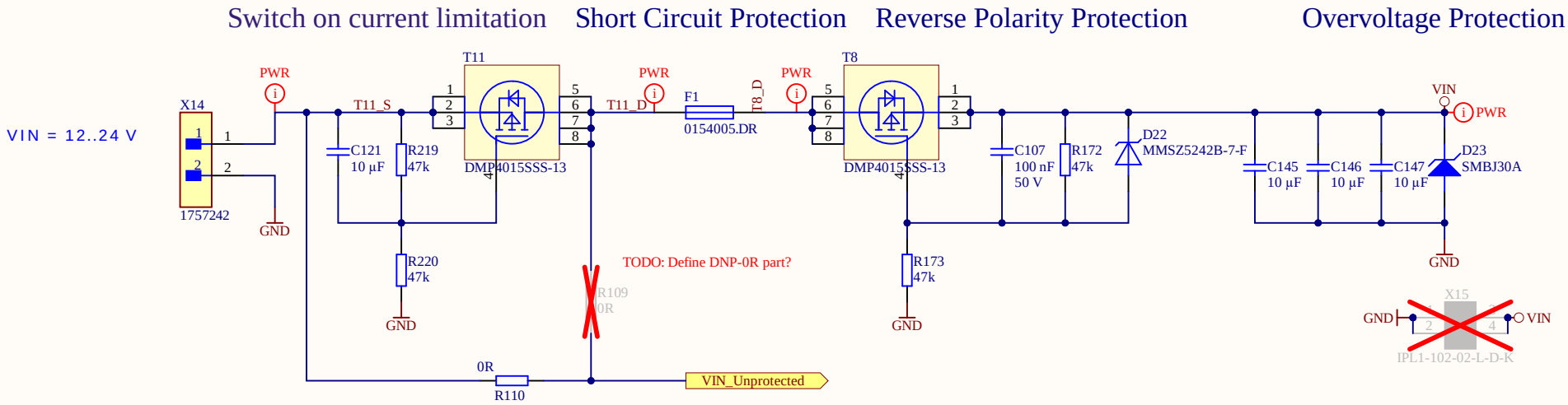
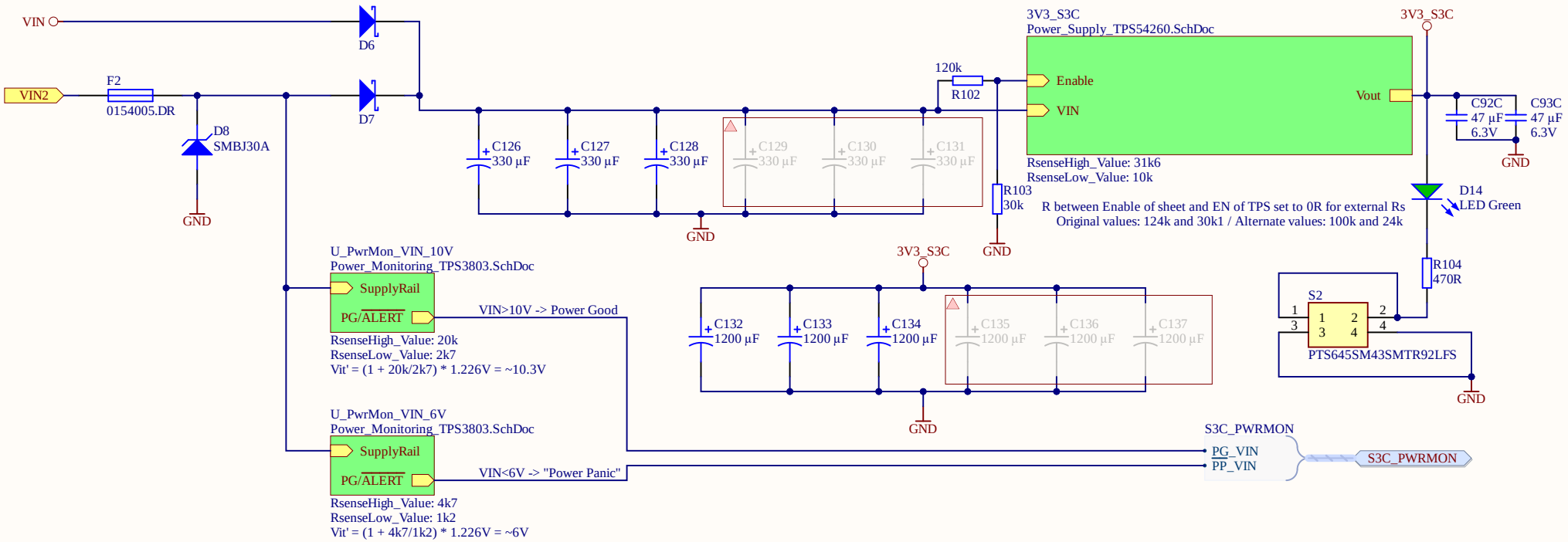
Title Power_Protection_VIN.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 19.5 of 60	



Title DIG_S3C_MultiChannelFunnel.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 20 of 60	

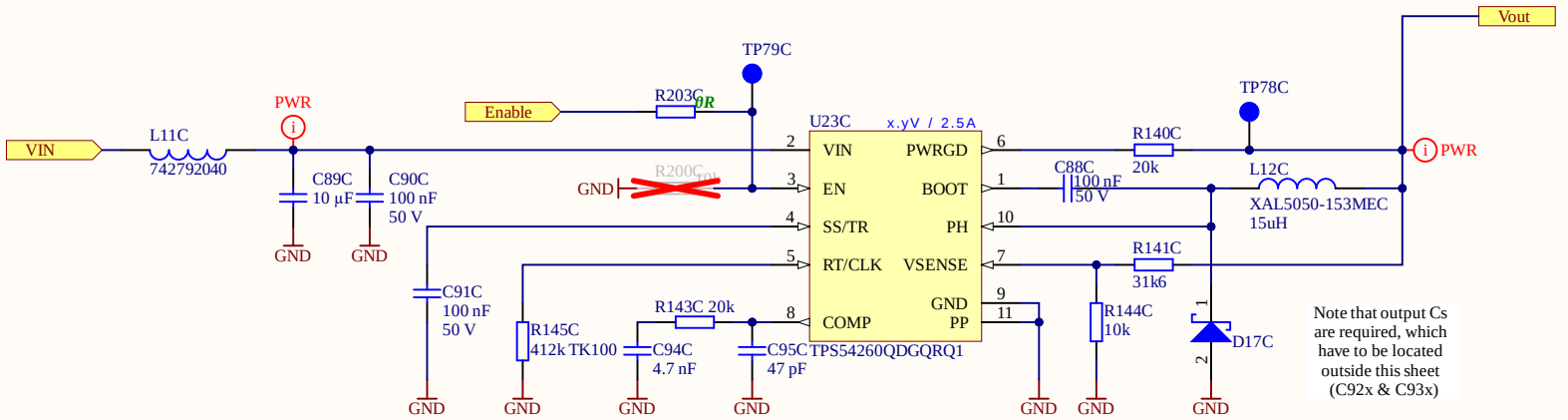


Title Power_Supply_Input.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 21 of 60	



Additional sources:
- Co-monitor VIN (by wire-OR-ing to S3C_PWRMON)
- LMZ/... (U10 / U11 / U12) : No integrated PG output
- TPS (U23 A to C): PWRGD (OD, up to 5.5V), valid from 1.5/3V input voltage
- SoM
  - PG_PL (aka PG_Module): OD, on-SoM pull-up to PL_DCIN (aka 3V3_MOD)
  - Some more PG_* signals
  - PLL_LOLn

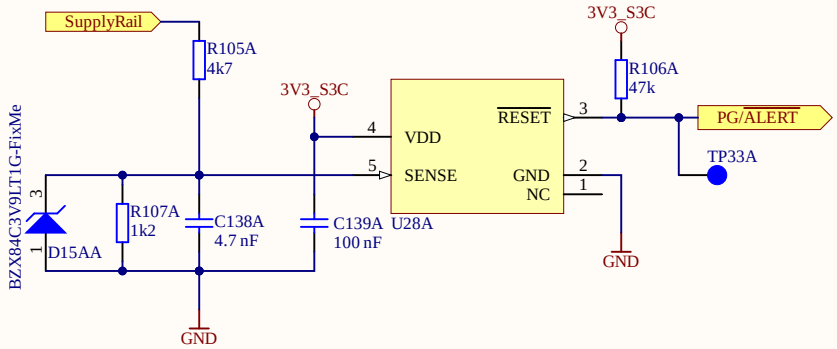
Title S3C_SupplyAndMonitoring.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	Date: 14/12/2024
Project: UZ_CarrierBoard.PrjPcb		Sheet 22 of 60



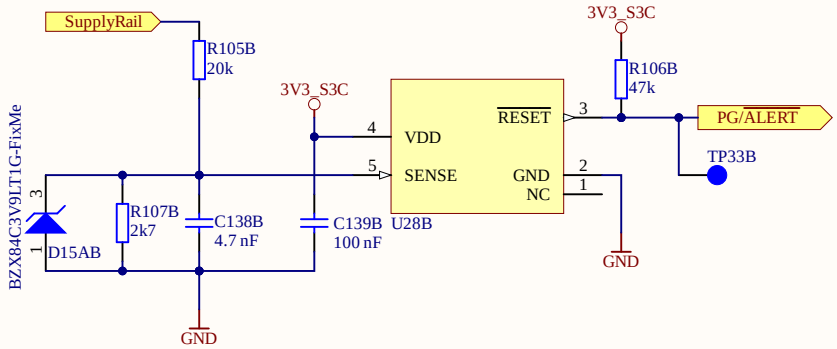
TODO: Externalize R145

	1V8	3V3	12V
RsenseHigh (R141)			
Value	2k	31k6	51k
MPN	UZgen_R_0603_2k	UZgen_R_0603_31k6	UZgen_R_0603_51k
RsenseLow (R144)			
Value	1k6	10k	3k6
MPN	UZgen_R_0603_1k6	UZgen_R_0603_10k	UZgen_R_0603_3k6

Title Power_Supply_TPS54260.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024 Sheet 23 of 60

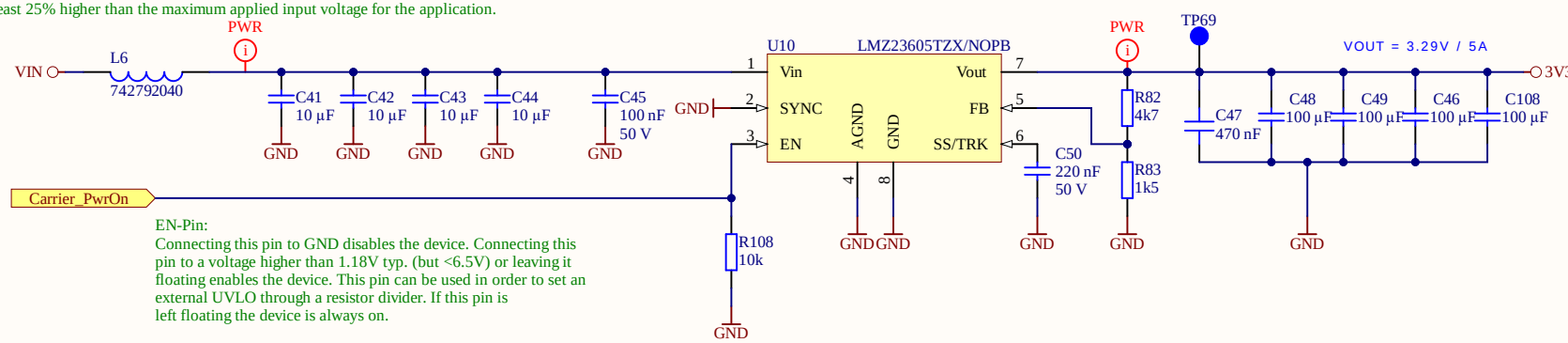


Title Power_Monitoring_TPS3803.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 24.1of 60	



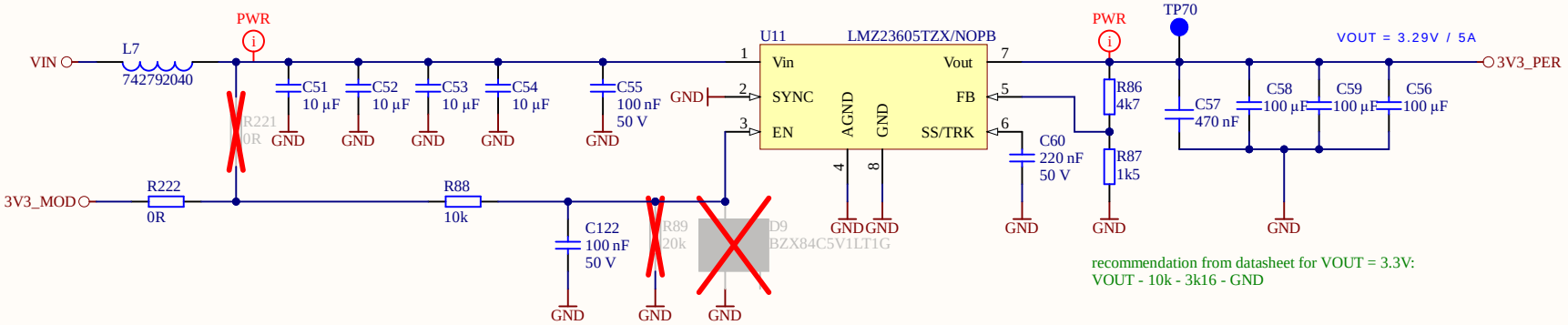
Title Power_Monitoring_TPS3803.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 24.2 of 60	

Notes: preferred to use 2x 22µF/50V capacitors at Vin, but this design uses 35V caps due to worse availability at distributors.
Datasheet: recommended minimum input capacitance is 22 µF (including derating) ceramic with voltage rating
at least 25% higher than the maximum applied input voltage for the application.



power supply for:
- Trenz module (PL_1V8, PS_1V8, ...)

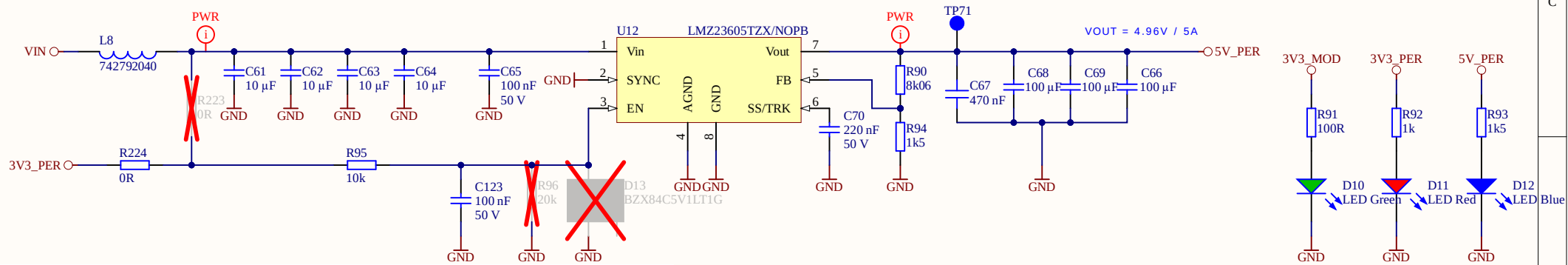
EN-Pin:
Connecting this pin to GND disables the device. Connecting this pin to a voltage higher than 1.18V typ. (but <6.5V) or leaving it floating enables the device. This pin can be used in order to set an external UVLO through a resistor divider. If this pin is left floating the device is always on.



power supply for:
- digital and analog sockets
- SD-Card
- Ethernet
- CAN

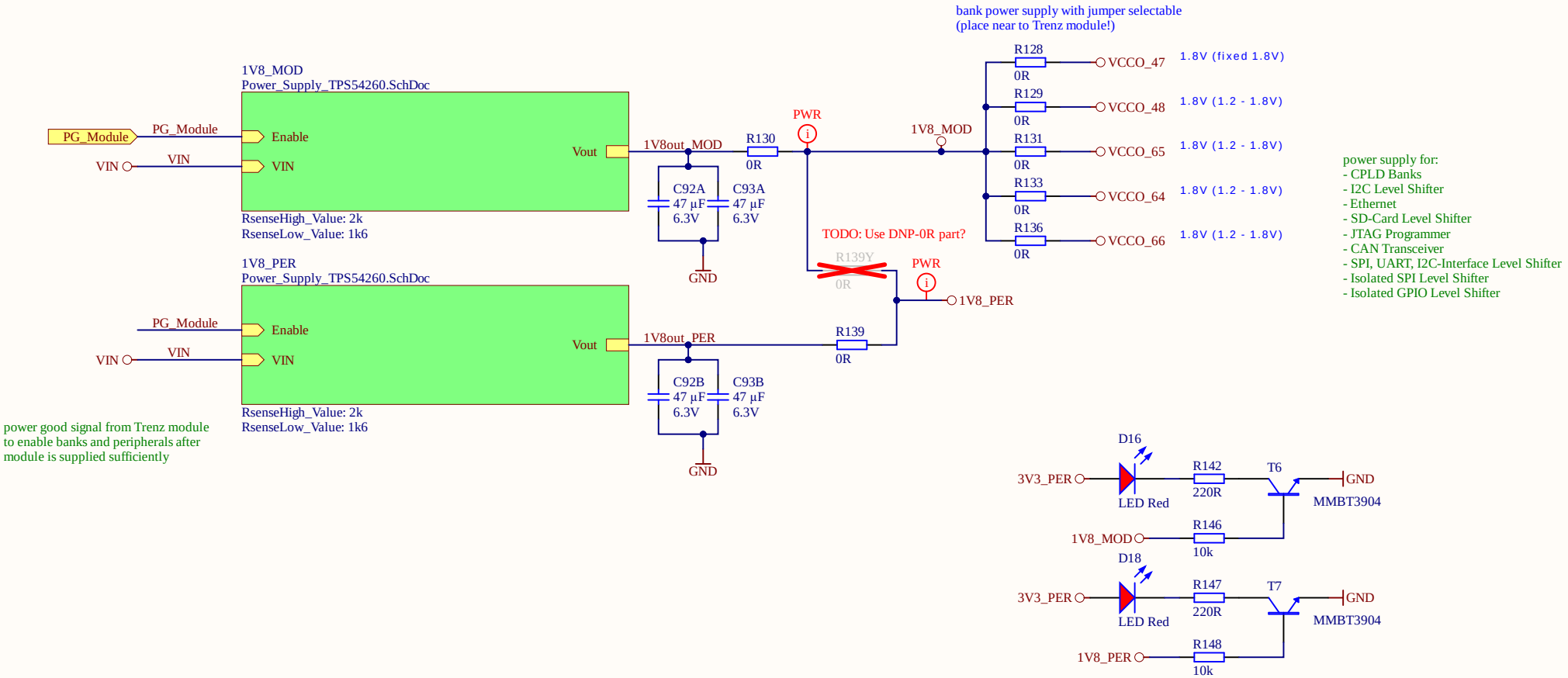
power supply for:
- digital and analog sockets

recommendation from datasheet for VOUT = 3.3V:
VOUT - 10k - 3k16 - GND

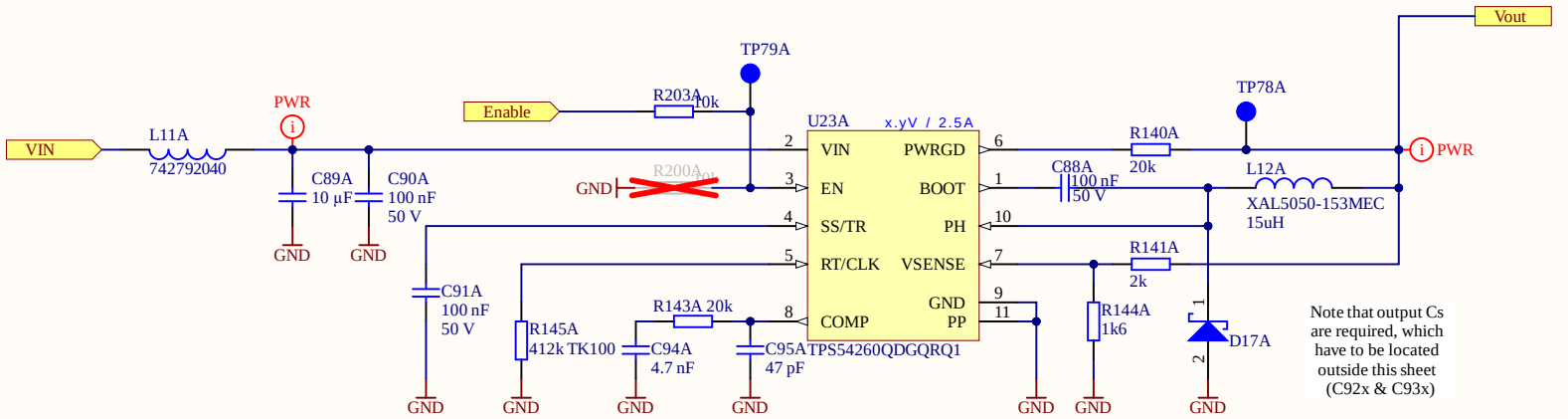


The delay time between the power supplies U10 U11 and U12 is determined by R88 C122 R95 and C123.
The delay time can be estimated as follows: t_on = -tau * ln(1-(U_en/U_max))
tau = R*C
U_en = 1,27V
U_max = output voltage of prior stage (e.g. 3V3)
Since the input current of the EN pin is about 21µA the real dealy time is a bit longer than the calculated value. With the values above there is a delay of about 5ms,

Title Power_Supply_1.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024 Sheet 25 of 60



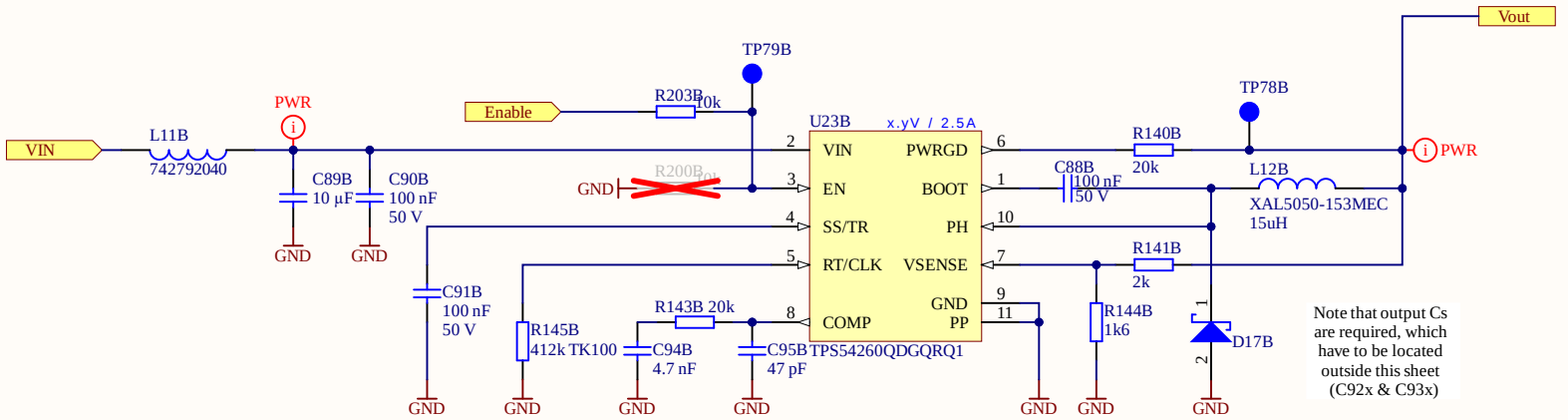
Title Power_Supply_2.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 26 of 60	



TODO: Externalize R145

	1V8	3V3	12V
RsenseHigh (R141)			
Value	2k	31k6	51k
MPN	UZgen_R_0603_2k	UZgen_R_0603_31k6	UZgen_R_0603_51k
RsenseLow (R144)			
Value	1k6	10k	3k6
MPN	UZgen_R_0603_1k6	UZgen_R_0603_10k	UZgen_R_0603_3k6

Title Power_Supply_TPS54260.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024 Sheet 26.1of 60

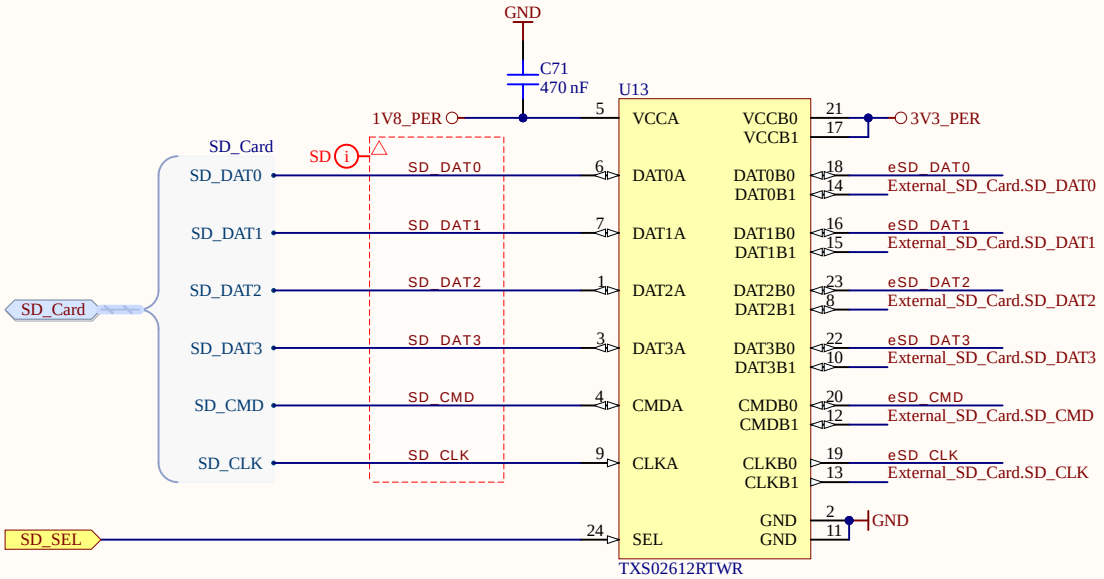


TODO: Externalize R145

	1V8	3V3	12V
RsenseHigh (R141)			
Value	2k	31k6	51k
MPN	UZgen_R_0603_2k	UZgen_R_0603_31k6	UZgen_R_0603_51k
RsenseLow (R144)			
Value	1k6	10k	3k6
MPN	UZgen_R_0603_1k6	UZgen_R_0603_10k	UZgen_R_0603_3k6

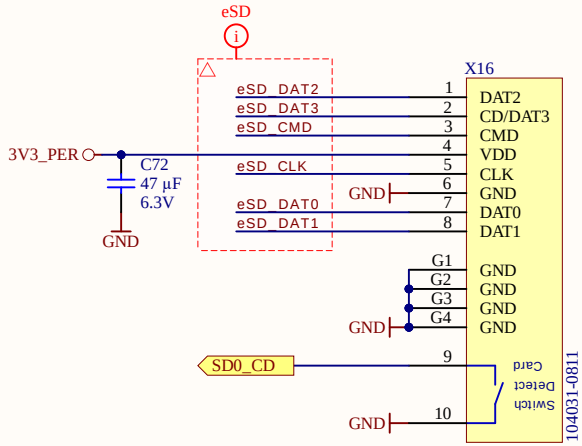
Title Power_Supply_TPS54260.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024 Sheet 26.2 of 60

Bidirectional Level Shifting 1.8V to 3.3V



SEL_SD on DGND to enable B0

SD Card Connector



External_SD_Card ExtSD

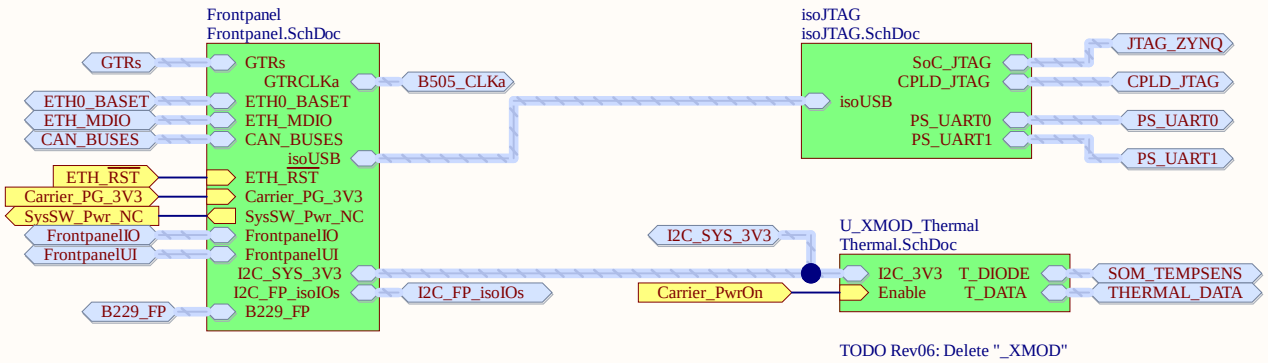
Title SD_Card.SchDoc		**UltraZohm** www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 27 of 60	

Config Pin 15 is high, so PHY address = 1
PHY is connected to GEM3 of Zynq via RGMII
MDIO is directly connected with GEM3 of Zynq.
This design is taken 1-1 fron Trenz TEBF0808.

In addition, the MDIO bus is shared with the other PHY; by de-soldering R31 and R39 on the frontpanel, its PHY can be disconnected from the bus.

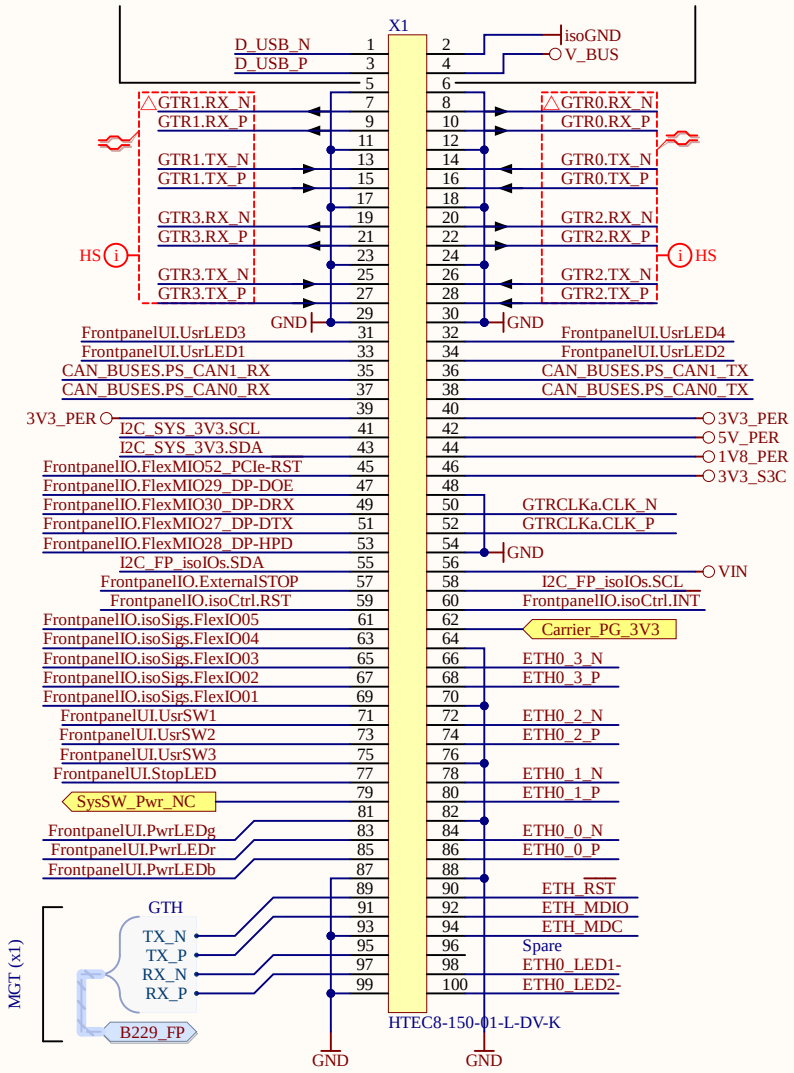
ETH-MDI
U2A
88E1512-A0-NNP2I000
TP42
TP43
R48 0R
R48L 0R
1V8_PER
GND
L3 MPZ1608S221ATA00
U3
OUT VCC GND OE/ST
SG-8018CB 25.000000MHz TJHSA
C3 470 nF
R49 33R
R210 10k
R50 4k99
ETH_BASET
R51 10k
R54 10k
T4 MMBT3904
T5 MMBT3904
U2C
C5 470 nF
C6 470 nF
C7 470 nF
C8 470 nF
C9 470 nF
C10 470 nF
C11 4.7 µF
C13 4.7 µF
C14 470 nF
C15 470 nF
C16 470 nF
C17 10 µF
C18 470 nF
C19 10 µF
C20 470 nF
C21 220 nF
L4 MPZ1608S221ATA00
3V3_PER
DVDD1V
AVDD18
AVDD3
R56 4k99
U2B
TSTPT
HSDACP
HSDACN
ETH_RGMII
ETH_MDIO
ETH_RST

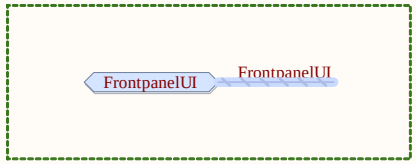
Title ETH-PHY.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 28 of 60	

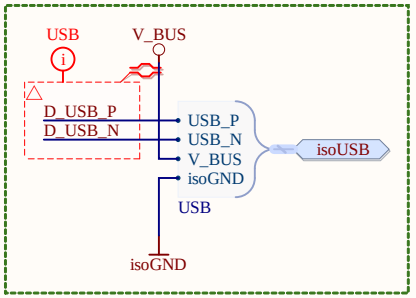


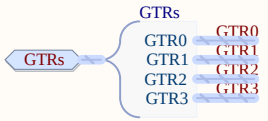
Title User_Connectors.SchDoc		**UltraZohm**	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 29 of 60	

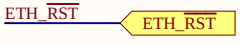
NB: VIN is always active - i.e., even if the system is (soft-)switched off

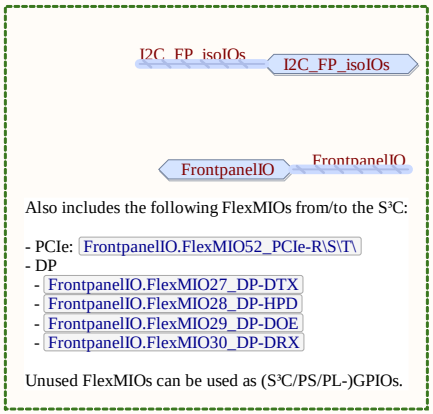


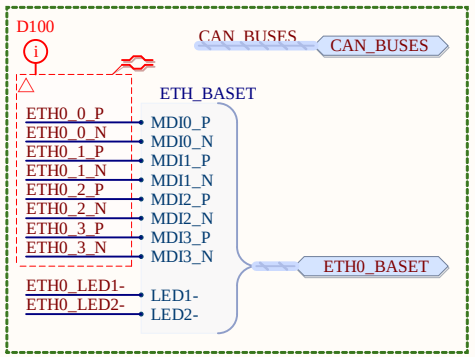








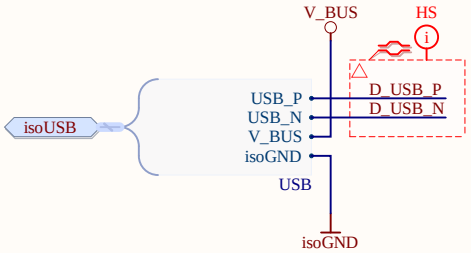


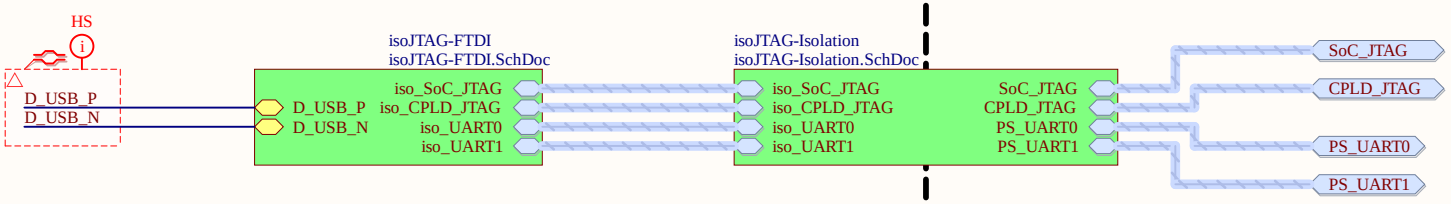


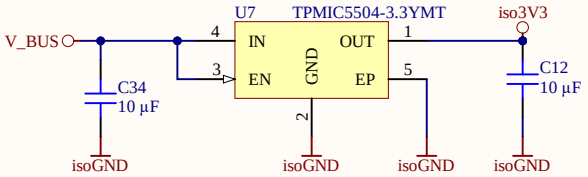
Title Frontpanel.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 30 of 60	

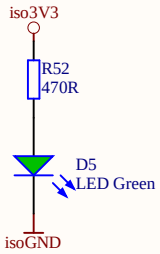
Isolated side

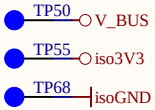
Processor side



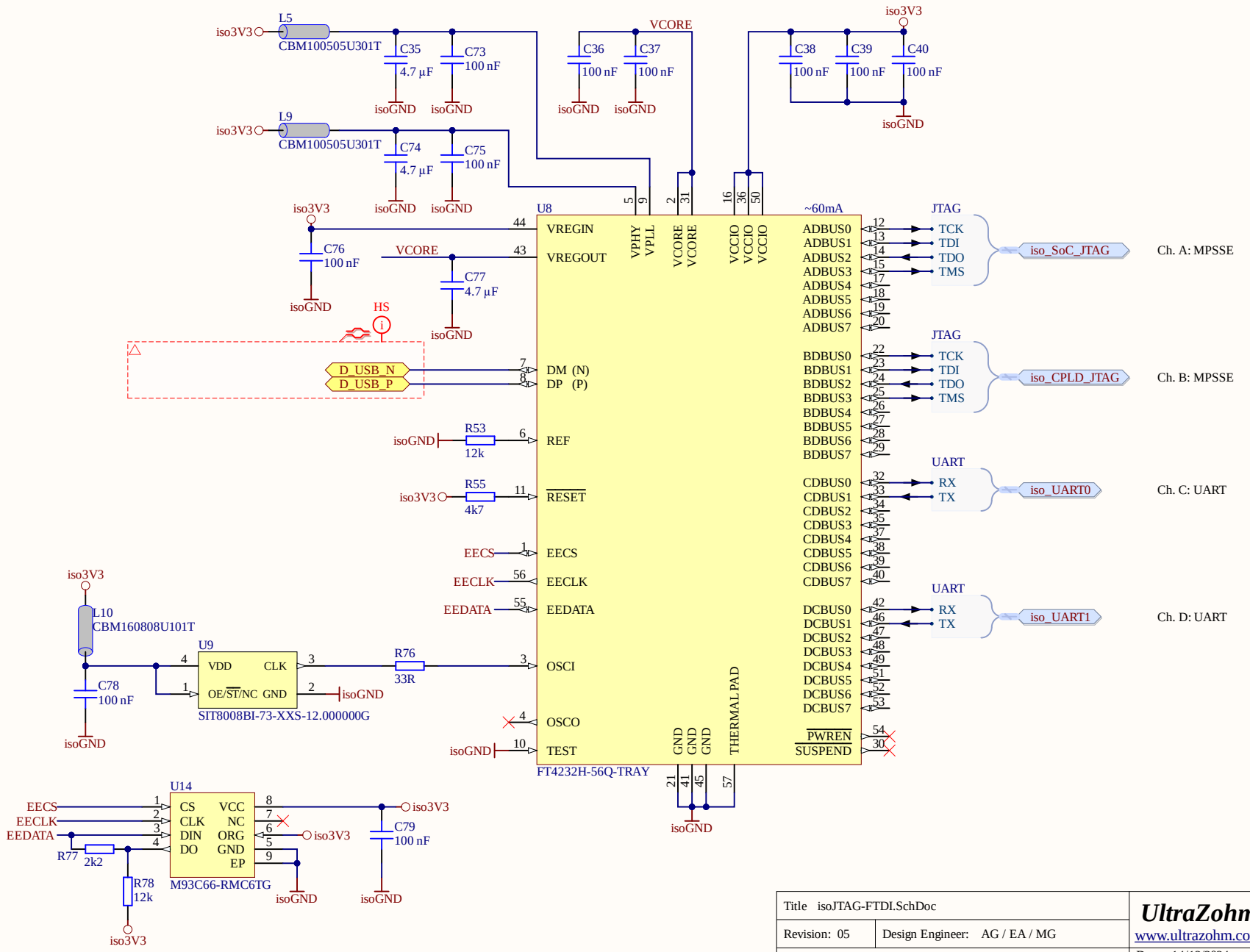




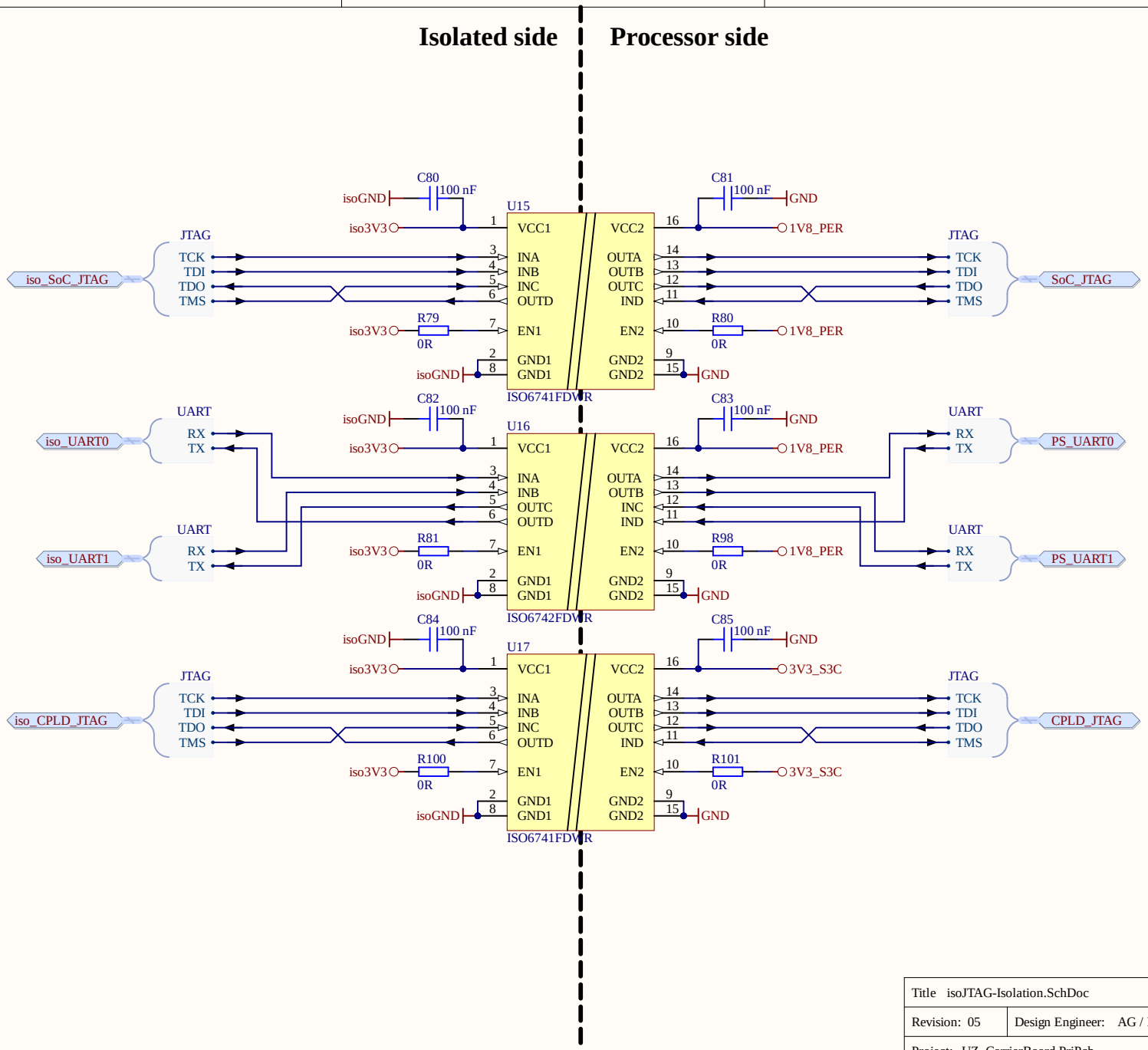




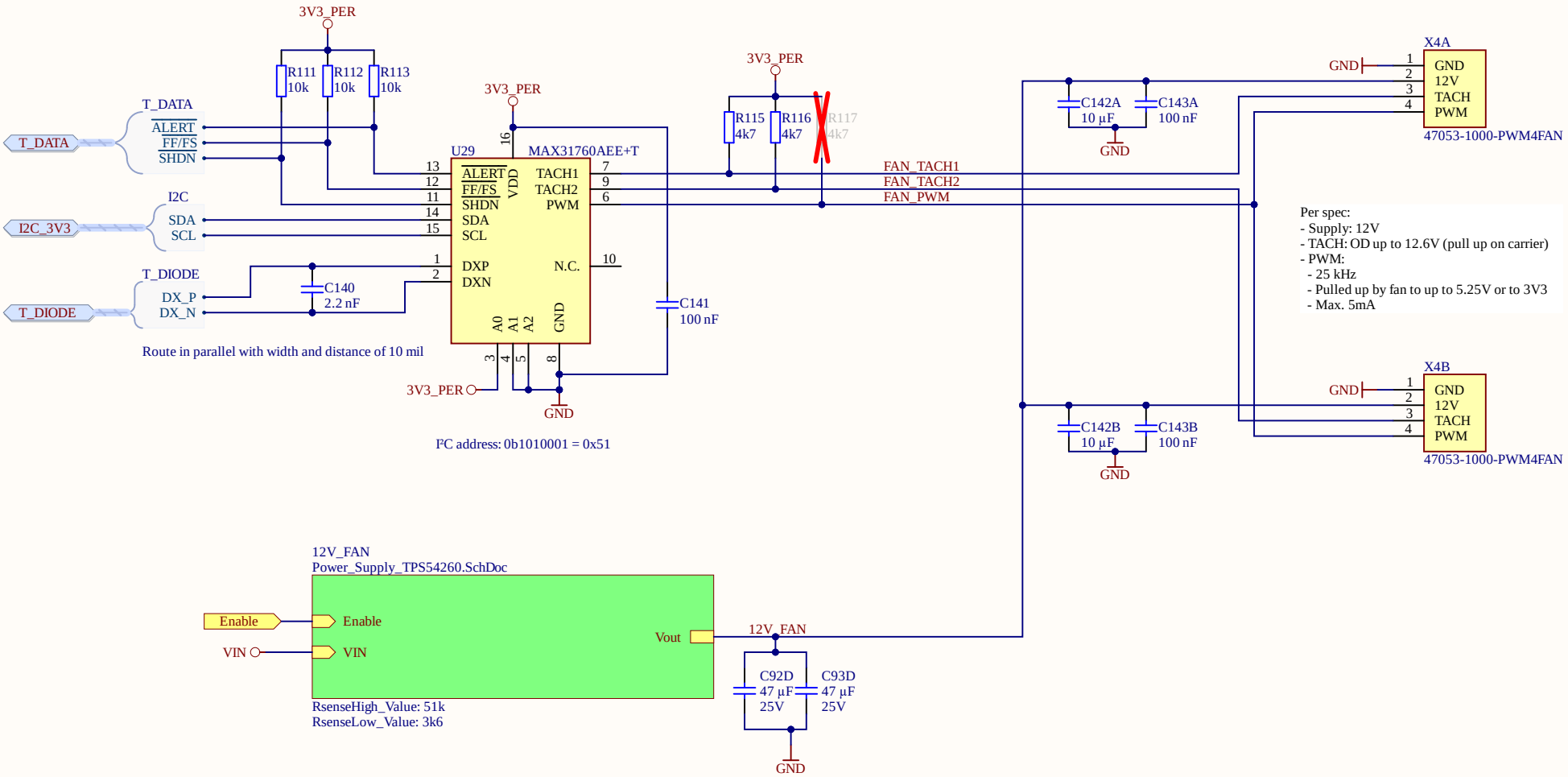
Title isoJTAG.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024 Sheet 31 of 60



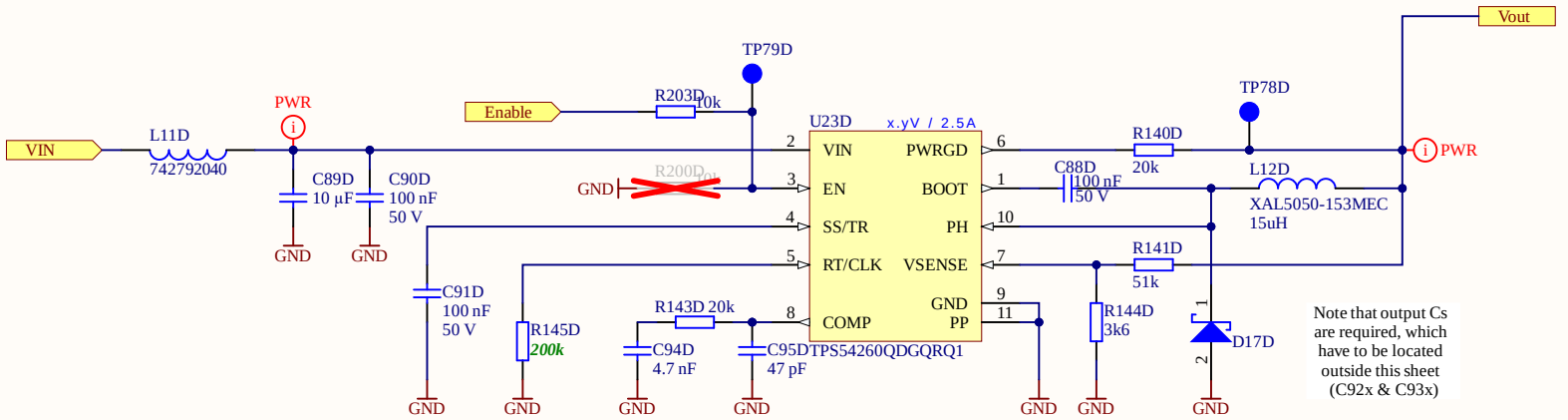
Title isoJTAG-FTDI.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 32 of 60	



Title isoJTAG-Isolation.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 33 of 60	



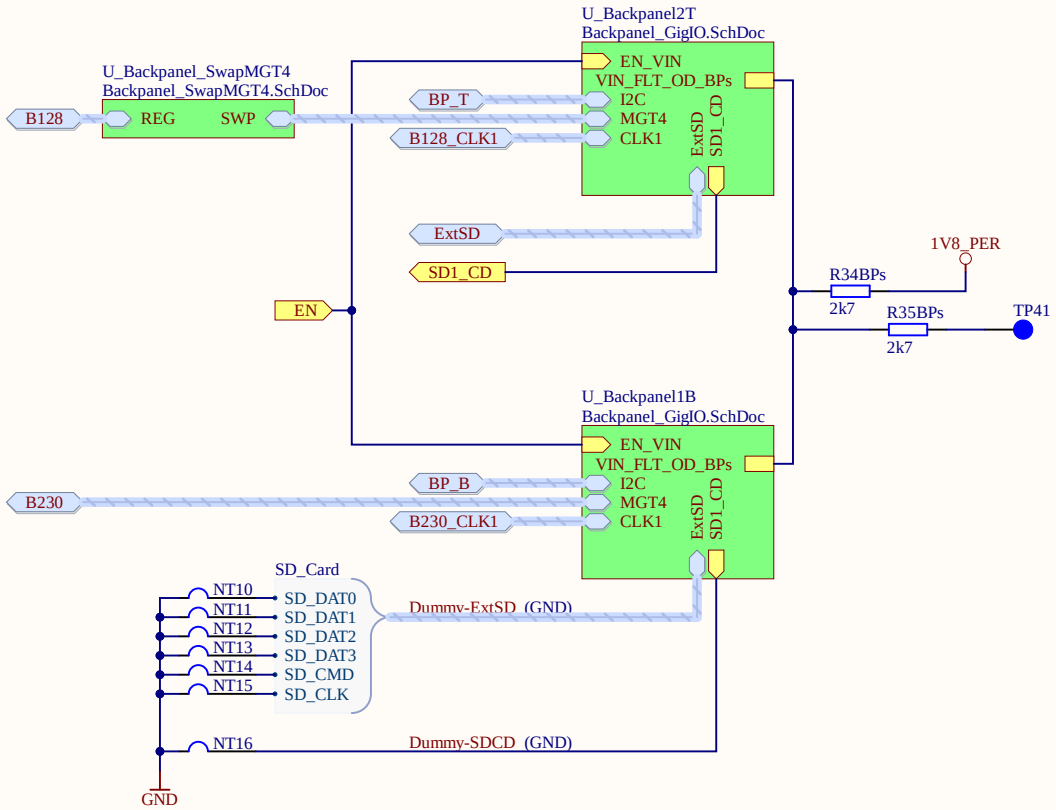
Title Thermal.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 34 of 60	



TODO: Externalize R145

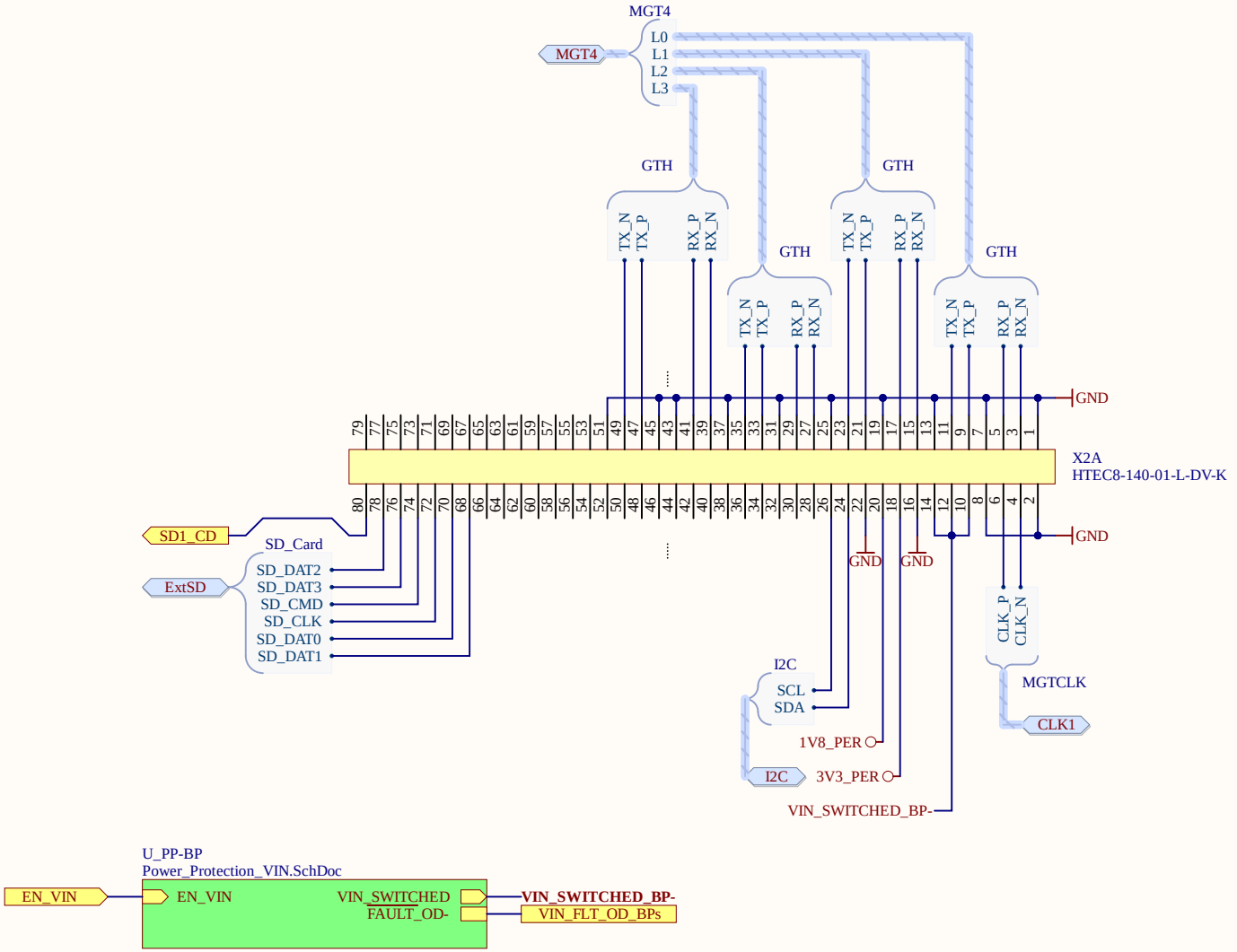
	1V8	3V3	12V
RsenseHigh (R141)			
Value	2k	31k6	51k
MPN	UZgen_R_0603_2k	UZgen_R_0603_31k6	UZgen_R_0603_51k
RsenseLow (R144)			
Value	1k6	10k	3k6
MPN	UZgen_R_0603_1k6	UZgen_R_0603_10k	UZgen_R_0603_3k6

Title Power_Supply_TPS54260.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024 Sheet 34.1of 60

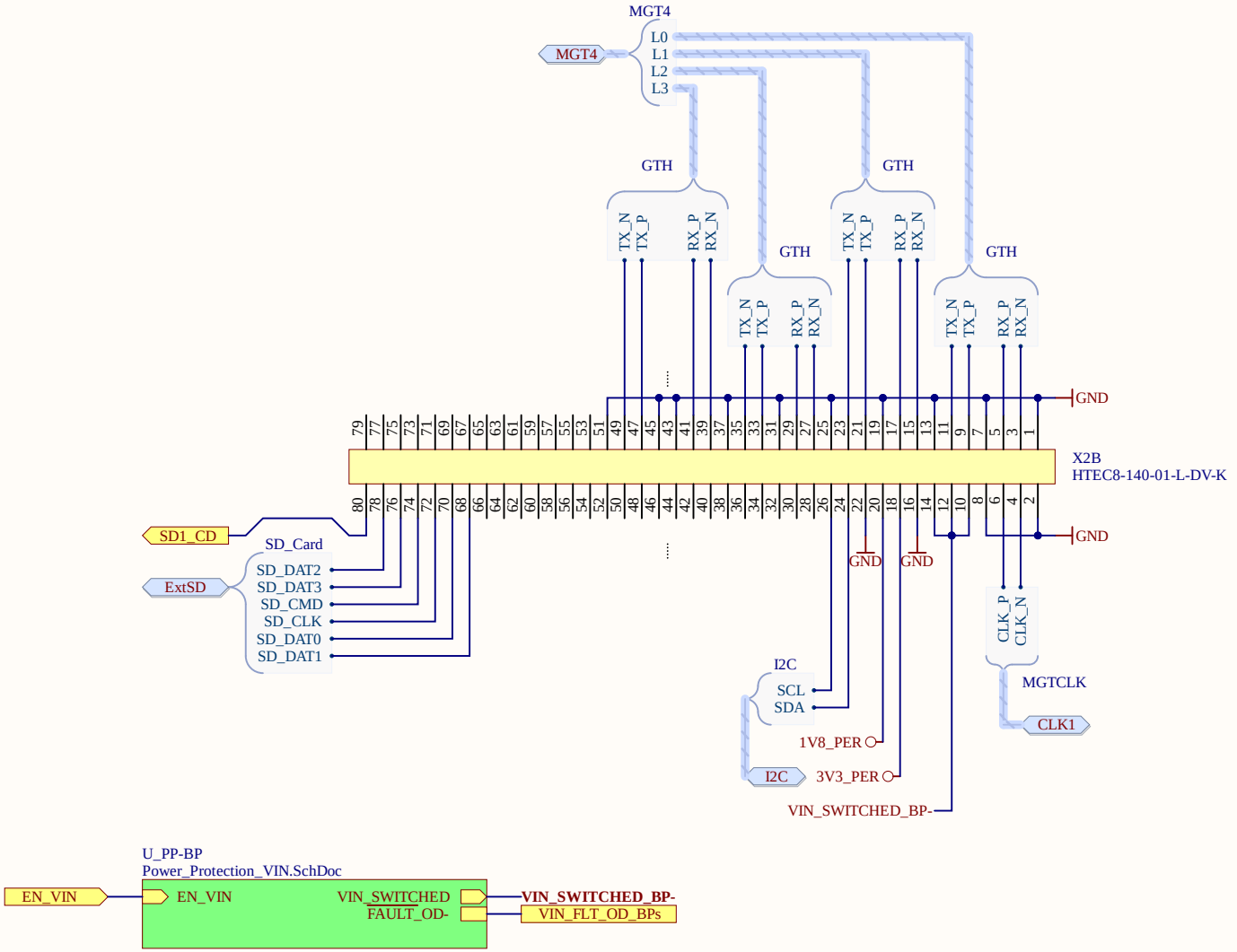


Title Backpanel.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024 Sheet 35 of 60

Title Backpanel_SwapMGT4.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 36 of 60	

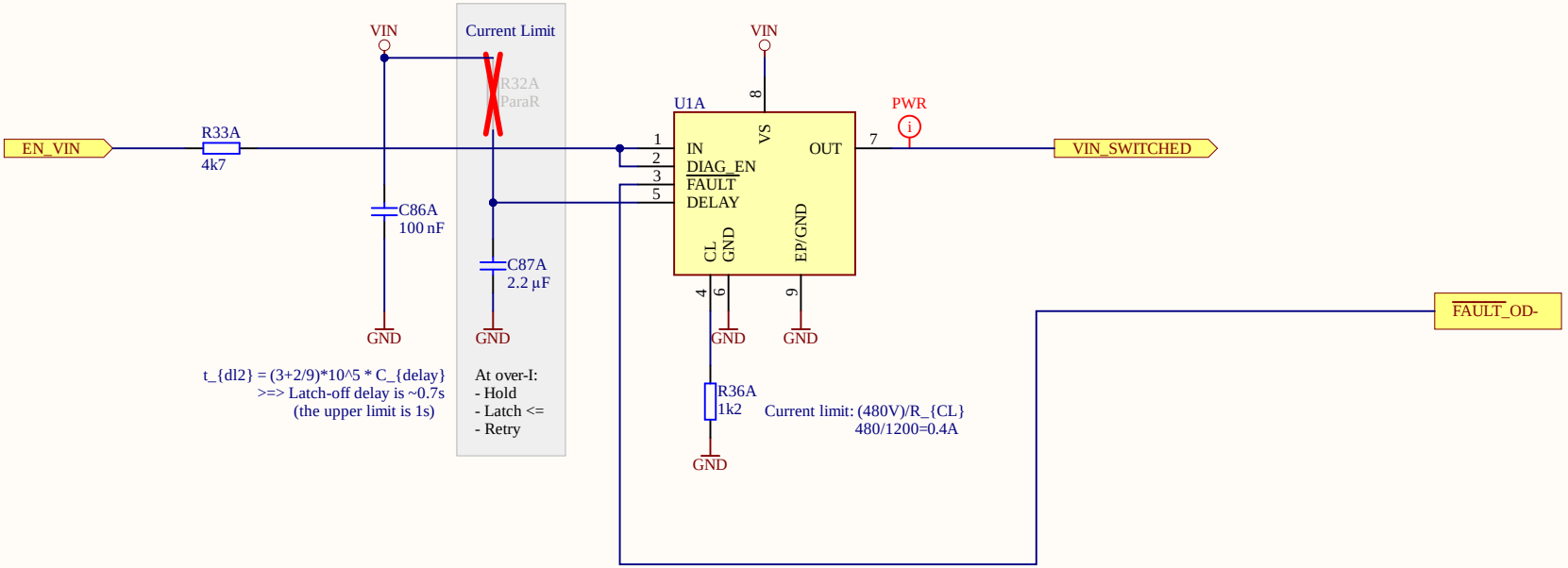


Title Backpanel_GigIO.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 37.1of 60	



Title Backpanel_GigIO.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 37.2of 60	

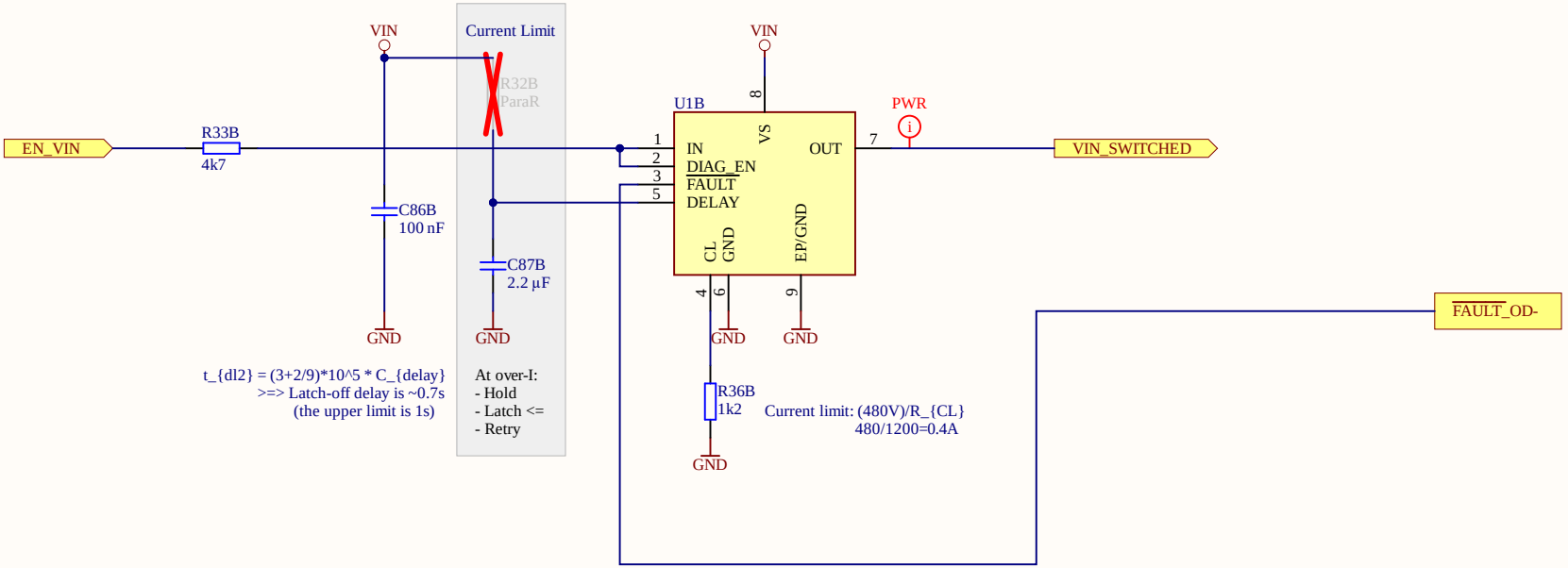
TODO Rev06: Rename ChaClass



I(off) is in the µA range if IN=DIAG_EN=0

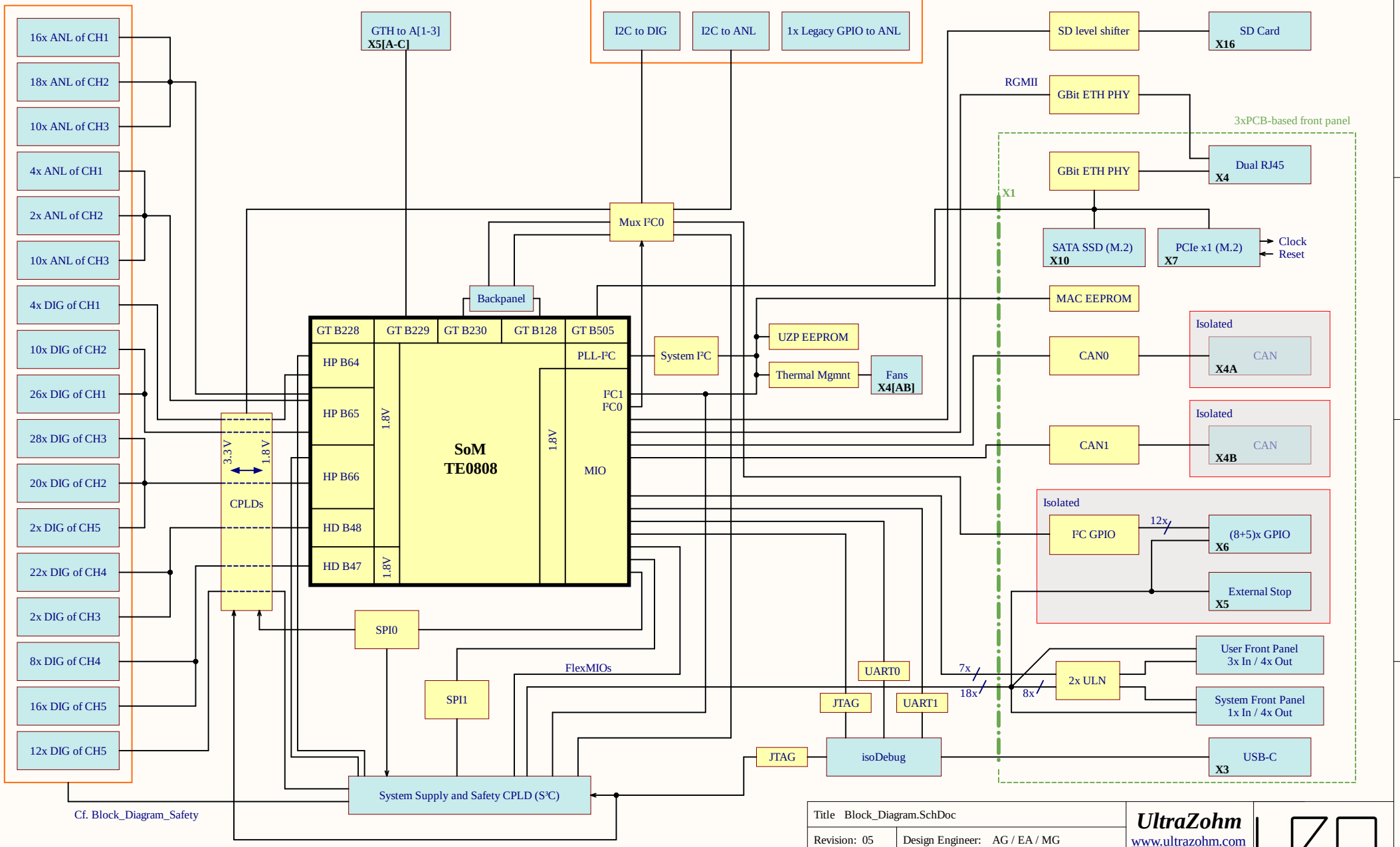
Title Power_Protection_VIN.SchDoc		UltraZohm	
Revision: 05	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 38.1of 60	

TODO Rev06: Rename ChaClass



I(off) is in the µA range if IN=DIAG_EN=0

Title Power_Protection_VIN.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 05	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024	
		Sheet 38.2 of 60	



Title Block_Diagram.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	Date: 14/12/2024
Project: UZ_CarrierBoard.PrjPcb		Sheet 39 of 60

Conceptual name:	Type:	Signal source -> sink:	Voltage:	Signal path/name:
5x Output_Enable (PILOT_OUT)	Per-Dx	S3C -> Slot-Conn.	3V3	DIG_S3C.SlotDi.SlotOE
1x FLT (Safe State Request; e.g., External Stop)	Shared	S3C -> Slot-Ctrl.	1V8	DIG_S3C.Shared.ReqSafeState
1x CarrierRdy	Shared	S3C -> Slot-Ctrl.	1V8	DIG_S3C.Shared.CarrierReady
5x !FLT	Per-Dx	Slot-Ctrl. -> S3C	1V8	DIG_S3C.SlotDi.SlotOK
5x OE	Per-Dx	Slot-Ctrl. -> S3C	1V8	DIG_S3C.SlotDi.ReqOE
(PILOT_IN; becomes FLT after fusion in slot c.)	(Local)	Slot-Conn. -> Slot-Ctrl.	3V3	(PILOT_INi and /PILOT_INi?)

System Controller (S³C) - The Overview...

- CPLD (Mach XO2): U19G
- Supply (3V3_S3C): U23 C via F2 / D7 or D6
- S³C banks on 3V3: U19A / U19E / U19F
- S³C banks on 1V8: U19B / U19C / U19D

Auxiliary circuitry (for D-slot-shared interfaces):
- JTAG multiplexing between S³C and Dx: U24
- CS generation of PS-SPI0 (same targets): U25

Sequencing- and safety-related remarks:
- The card-driven "OK" signal (PILOT_IN) plus the slot controller's internal state (de)assert OE
- The S³C receives 1 OE per slot, ANDs it with its internal state, and sets per-slot "OE"s (_OUT)

Output_Enable (PILOT_OUT)
FLT
CarrierRdy
!FLT
OE

Power Supply Supervisors (U28 A/B)
External Stop
SoC

D1-Slot Controller
D2-Slot Controller
D3-Slot Controller
D4-Slot Controller
D5-Slot Controller

PILOT_IN
2x
2x
D1-Slot
D2-Slot
D3-Slot
D4-Slot
D5-Slot

Title Block_Diagram_Safety.SchDoc		UltraZohm www.ultrazohm.com
Revision: 05	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 14/12/2024 Sheet 40 of 60