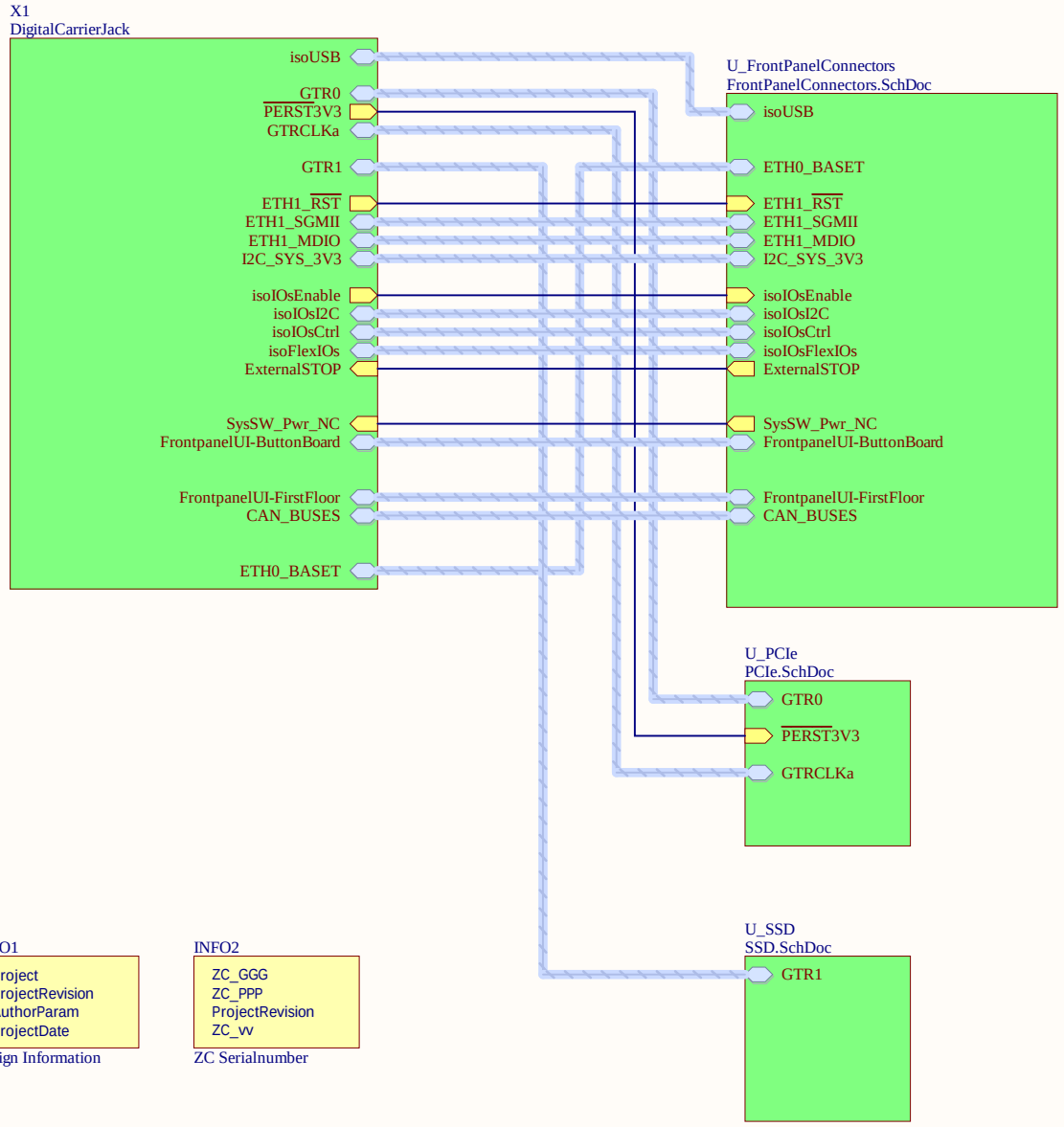


FIXMEs:
- JLC-ify & unmask i.IO protection

Choose size of UZ logo by choosing footprint...

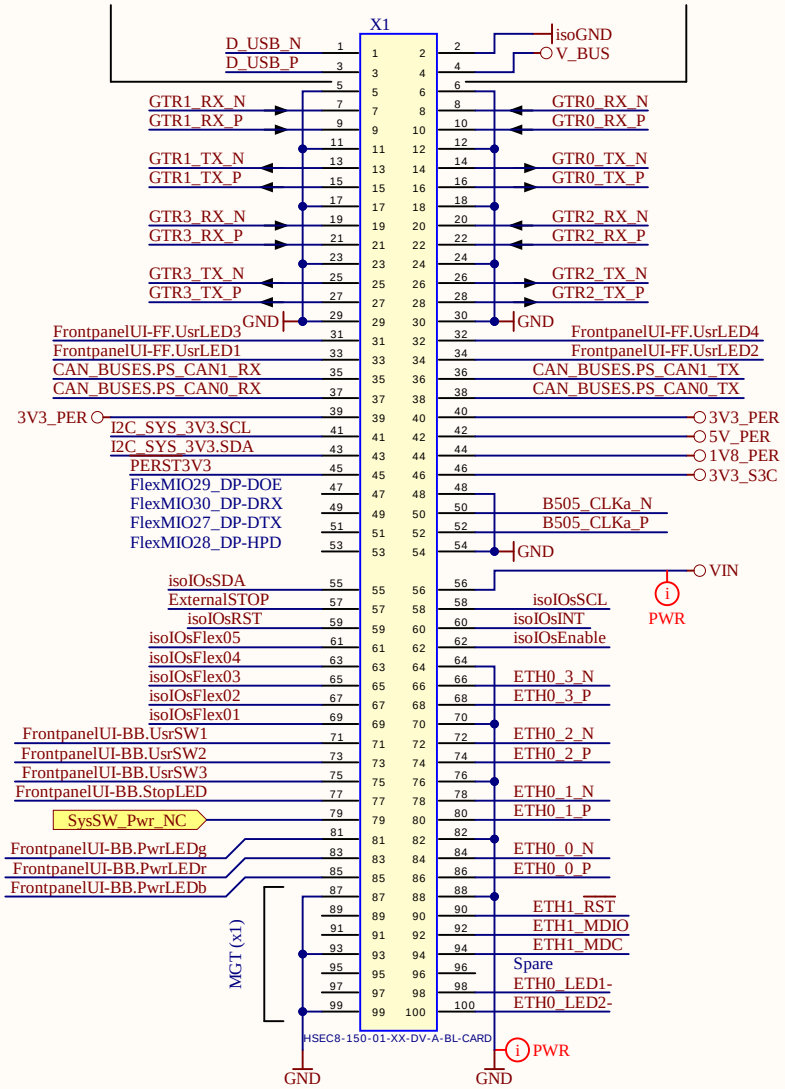
LOGO1

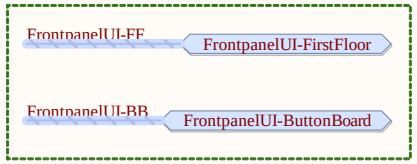
INFO1
Project
ProjectRevision
AuthorParam
ProjectDate
Design Information

INFO2
ZC_GGG
ZC_PPP
ProjectRevision
ZC_vv
ZC Serialnumber

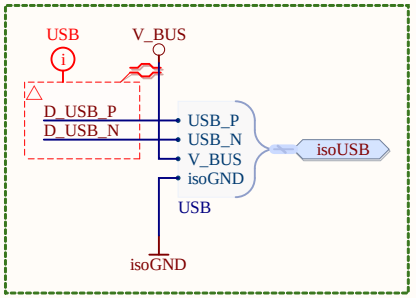
Title TopSheet.SchDoc		**UltraZohm**	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 1 of 34	

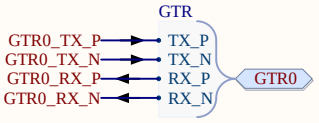
NB: VIN is always active - i.e., even if the system is (soft-)switched off

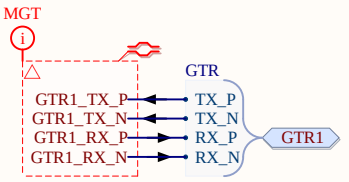


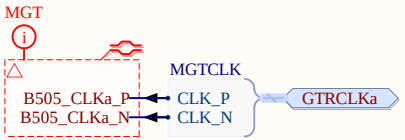


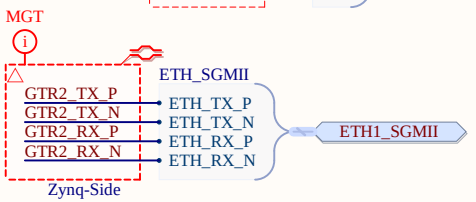
Currently not (yet?) instantiated function groups:
- DP option
- Anything else that one could implement using the 4 (S³C-connected) FlexMIOs 27 to 30 and/or I²C0 :-)

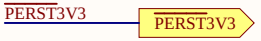


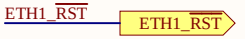


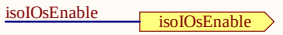


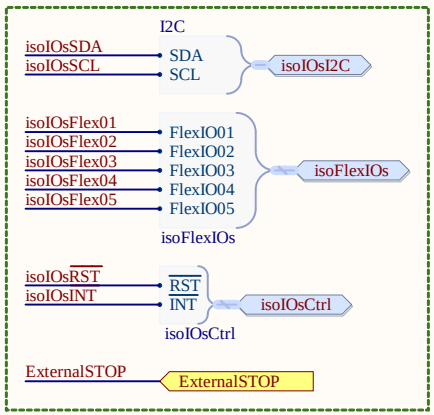


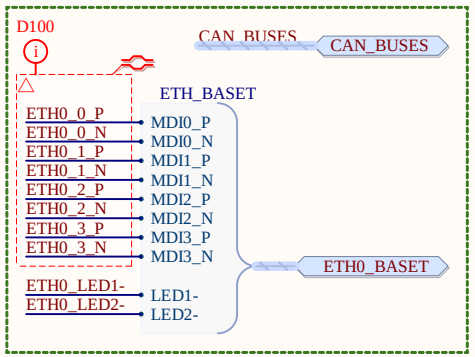




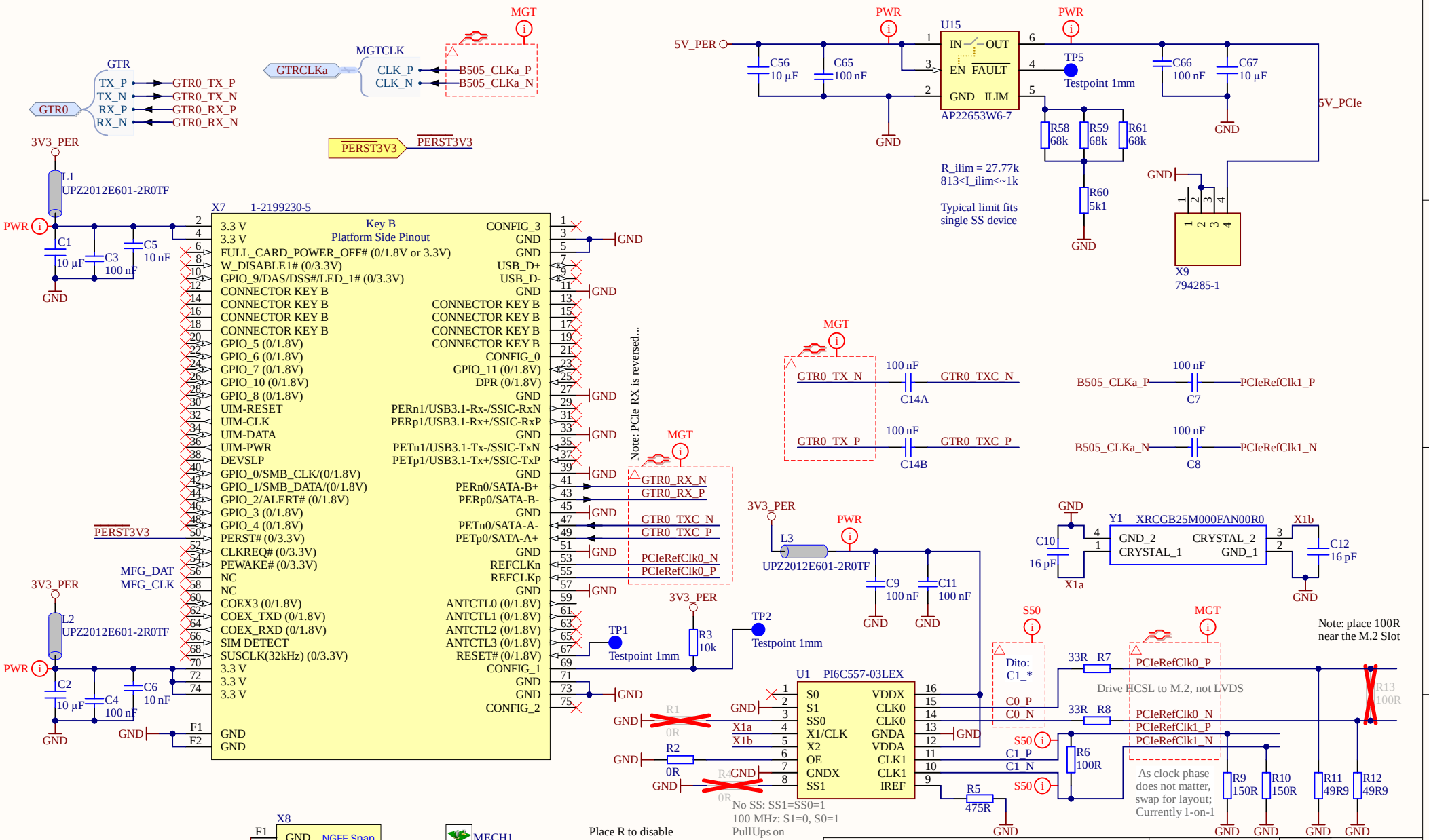




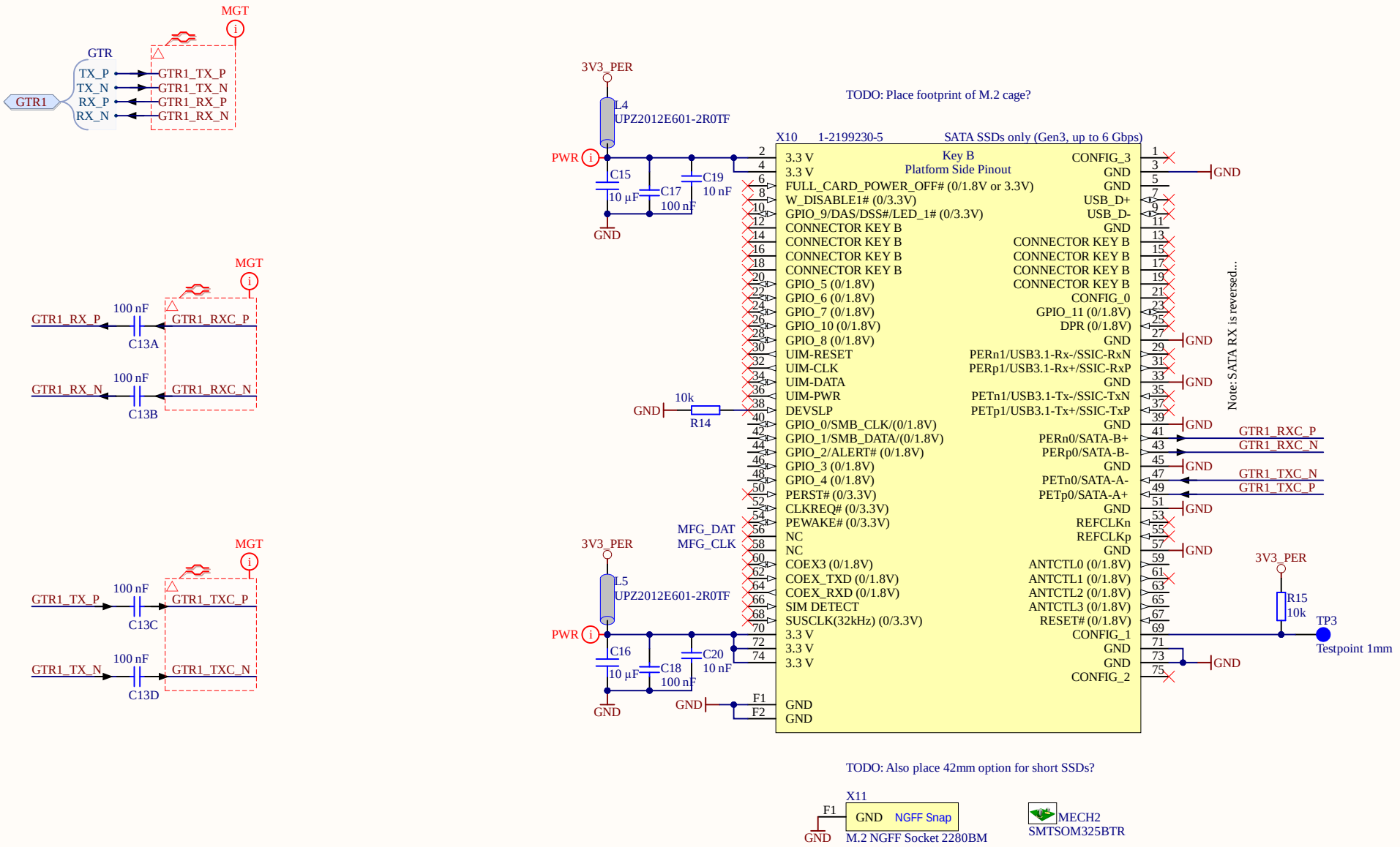




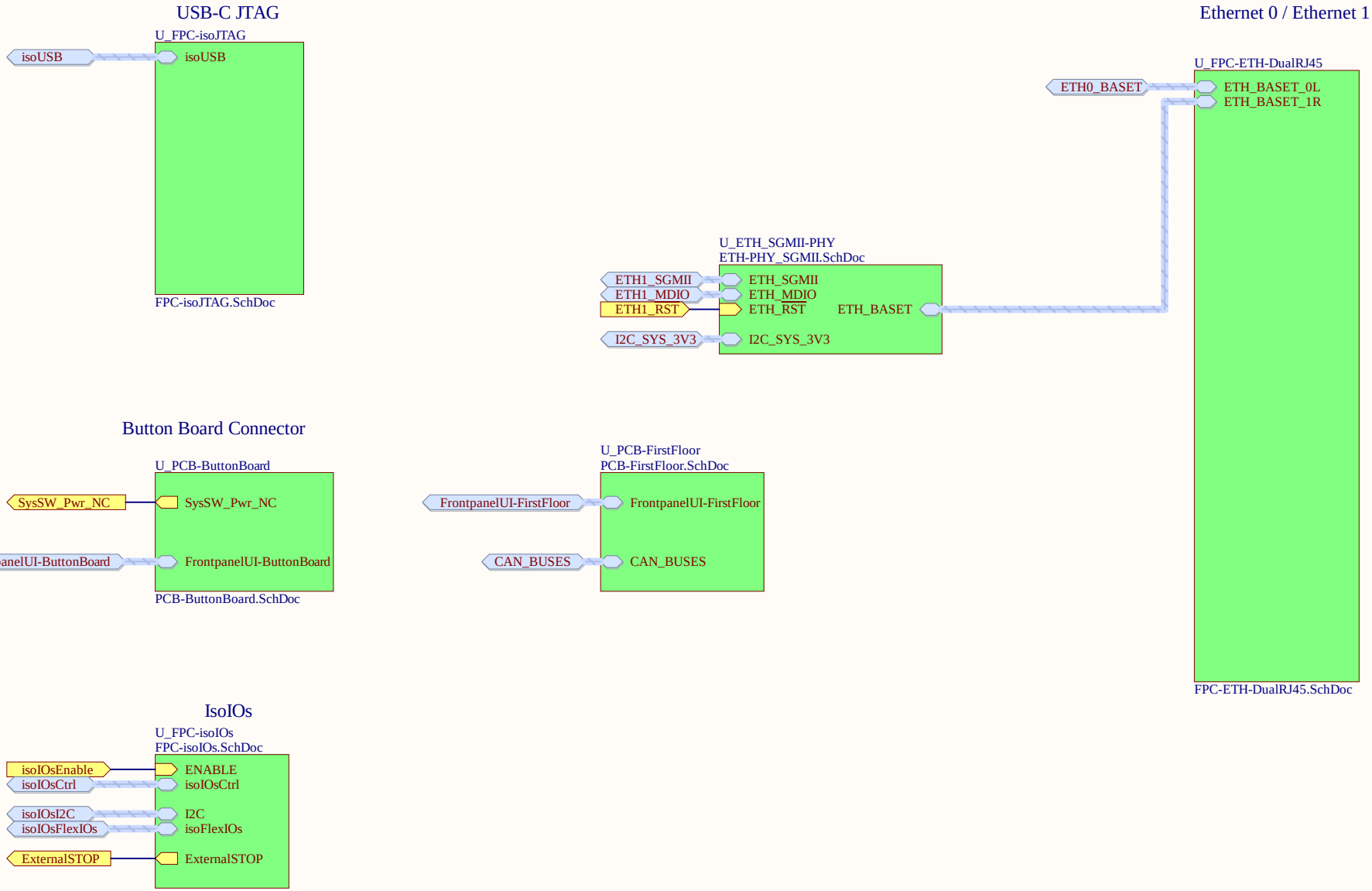
Title DigitalCarrierJack.SchDoc		UltraZohm www.ultrazohm.com
Revision: 02	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025 Sheet 2 of 34



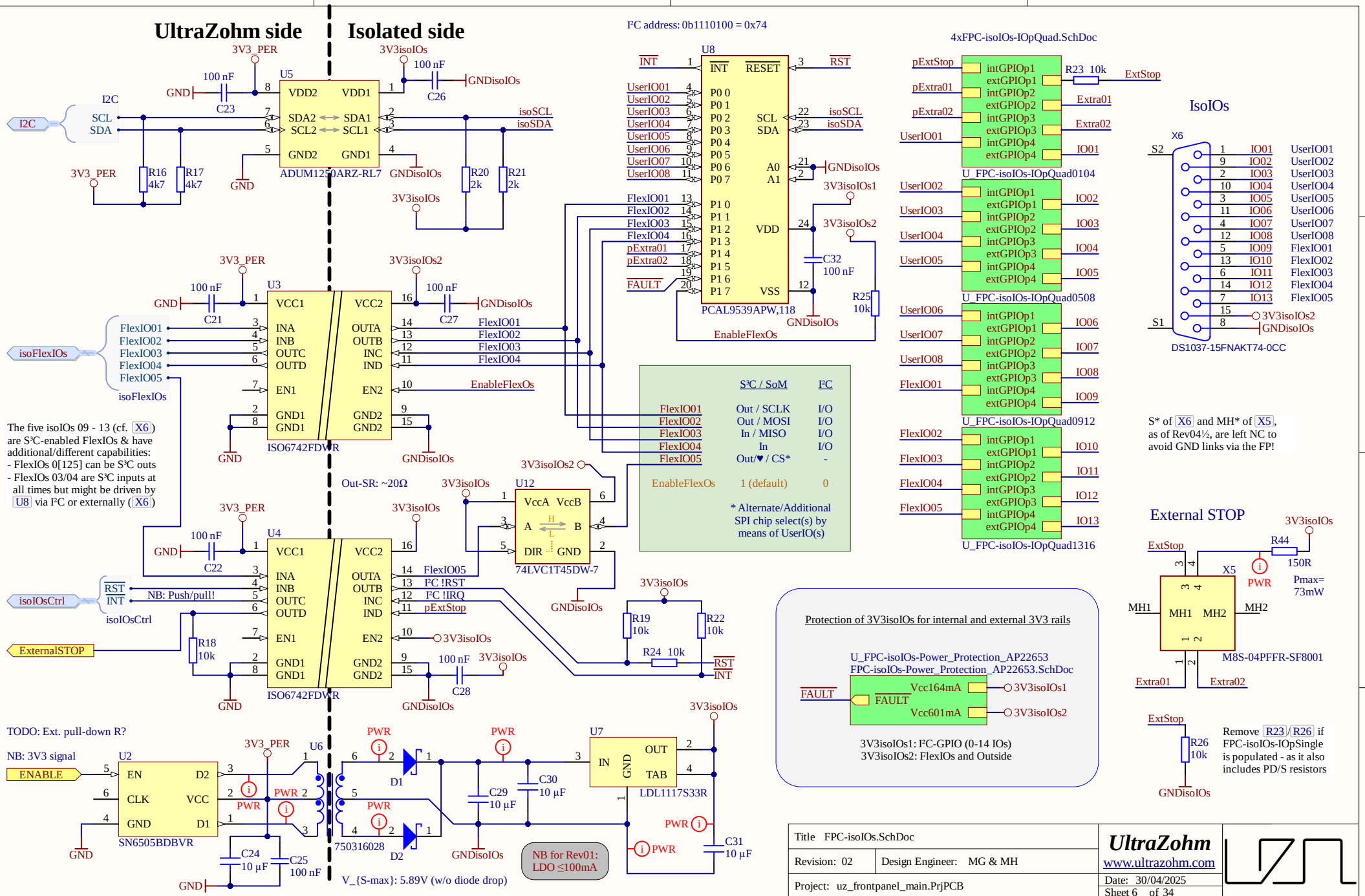
Title PCIe.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 3 of 34	

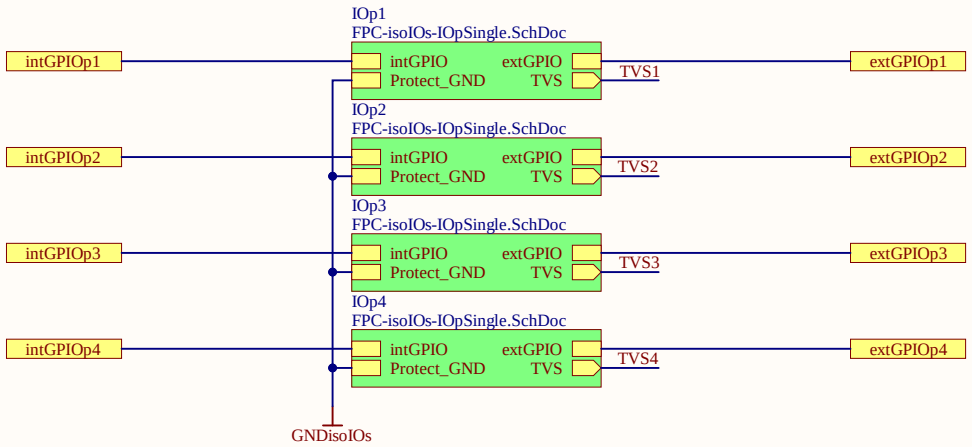


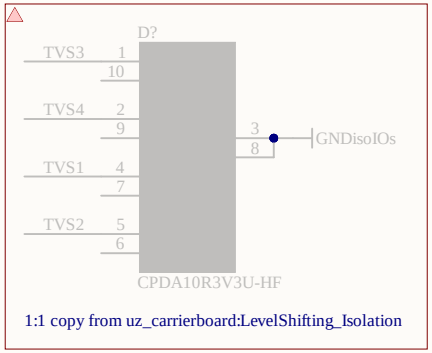
Title SSD.SchDoc		UltraZohm www.ultrazohm.com
Revision: 02	Design Engineer: MG & MH	Date: 30/04/2025
Project: uz_frontpanel_main.PrjPCB		Sheet 4 of 34



Title FrontPanelConnectors.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 5 of 34	

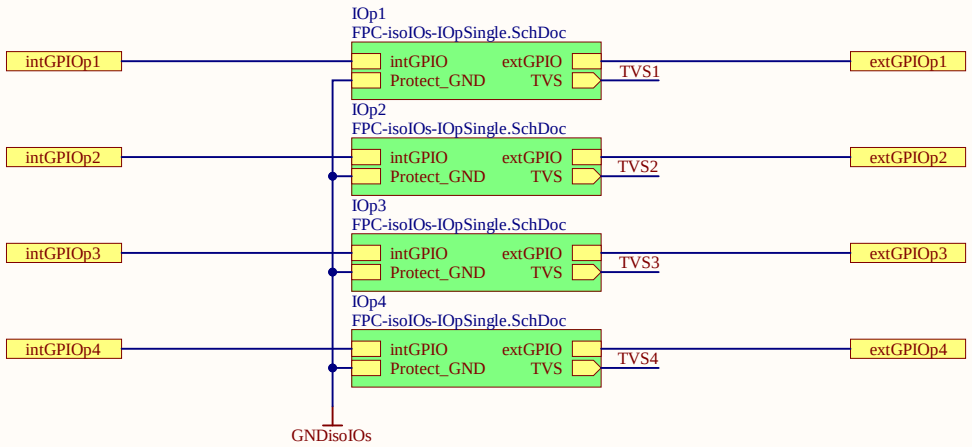

UltraZohm side
Isolated side
I²C address: 0b1110100 = 0x74
4xFPC-isoIOs-IOpQuad.SchDoc
IsoIOs
U5
ADUM1250ARZ-RL7
U8
PCAL9539APW,118
U3
ISO6742FDWR
U4
ISO6742FDWR
U12
74LVC1T45DW-7
U2
SN6505BDBVR
U6
750316028
U7
LDL1117S33R
U_FPC-isoIOs-IOpQuad0104
U_FPC-isoIOs-IOpQuad0508
U_FPC-isoIOs-IOpQuad0912
U_FPC-isoIOs-IOpQuad1316
X6
DS1037-15FNAKT74-0CC
X5
M8S-04PFFR-SF8001
S³C / SoM
I²C
* Alternate/Additional SPI chip select(s) by means of UserIO(s)
The five isoIOs 09 - 13 (cf. X6) are S³C-enabled FlexIOs & have additional/different capabilities:
- FlexIOs 0[125] can be S³C outs
- FlexIOs 03/04 are S³C inputs at all times but might be driven by U8 via I²C or externally (X6)
Out-SR: ~20Ω
NB: Push/pull!
TODO: Ext. pull-down R?
NB: 3V3 signal
V_{S-max}: 5.89V (w/o diode drop)
NB for Rev01: LDO ≤100mA
S* of X6 and MH* of X5, as of Rev04½, are left NC to avoid GND links via the FP!
External STOP
Protection of 3V3isoIOs for internal and external 3V3 rails
U_FPC-isoIOs-Power_Protection_AP22653
FPC-isoIOs-Power_Protection_AP22653.SchDoc
3V3isoIOs1: I²C-GPIO (0-14 IOs)
3V3isoIOs2: FlexIOs and Outside
Remove R23 / R26 if FPC-isoIOs-IOpSingle is populated - as it also includes PD/S resistors
Title FPC-isoIOs.SchDoc
Revision: 02
Design Engineer: MG & MH
Project: uz_frontpanel_main.PrjPCB
UltraZohm
www.ultrazohm.com
Date: 30/04/2025
Sheet 6 of 34

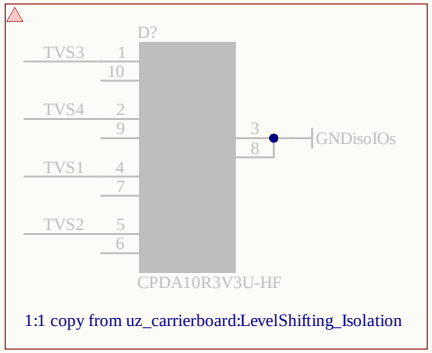




1:1 copy from uz_carrierboard:LevelShifting_Isolation

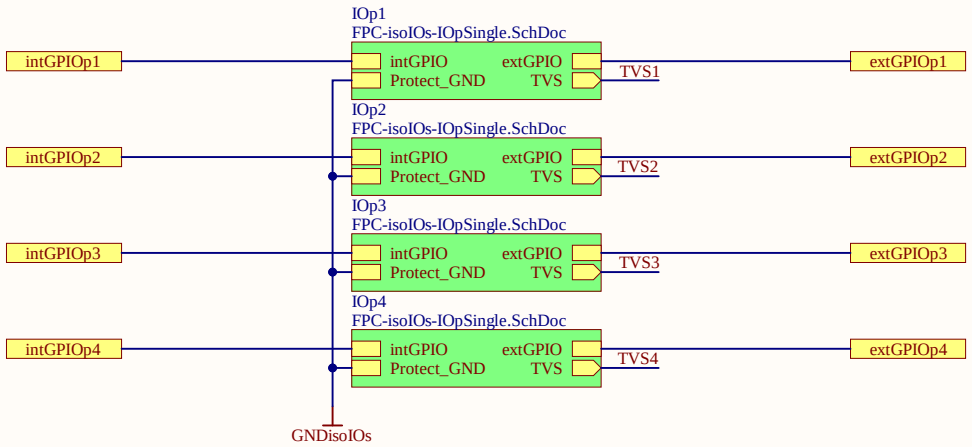
Title FPC-isoIOs-IOpQuad.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 7.1 of 34	

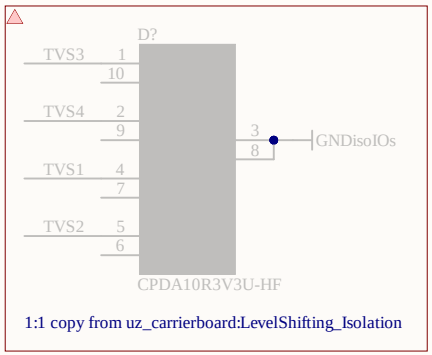




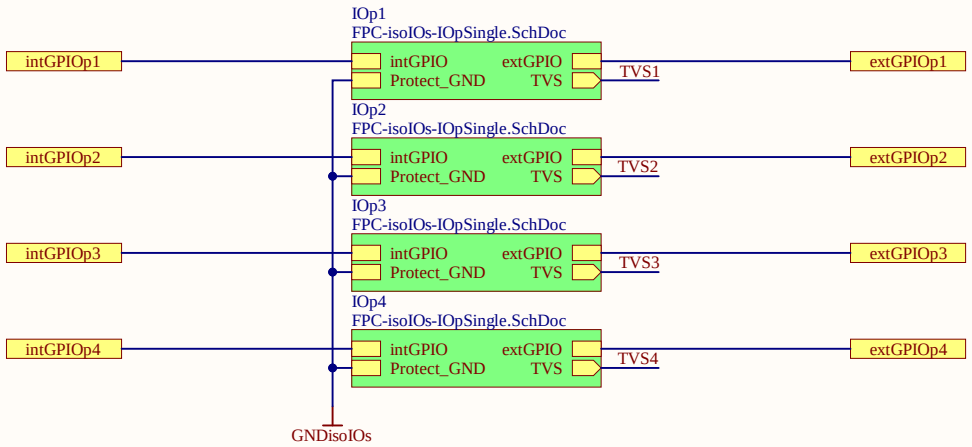
1:1 copy from uz_carrierboard:LevelShifting_Isolation

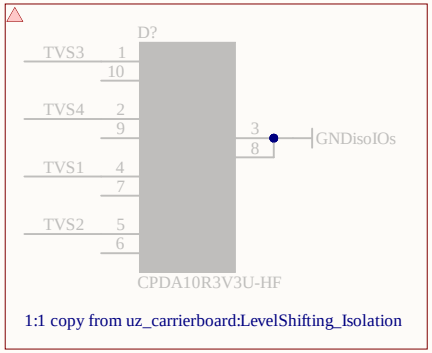
Title FPC-isoIOs-IOpQuad.SchDoc		**UltraZohm**	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 7.2 of 34	





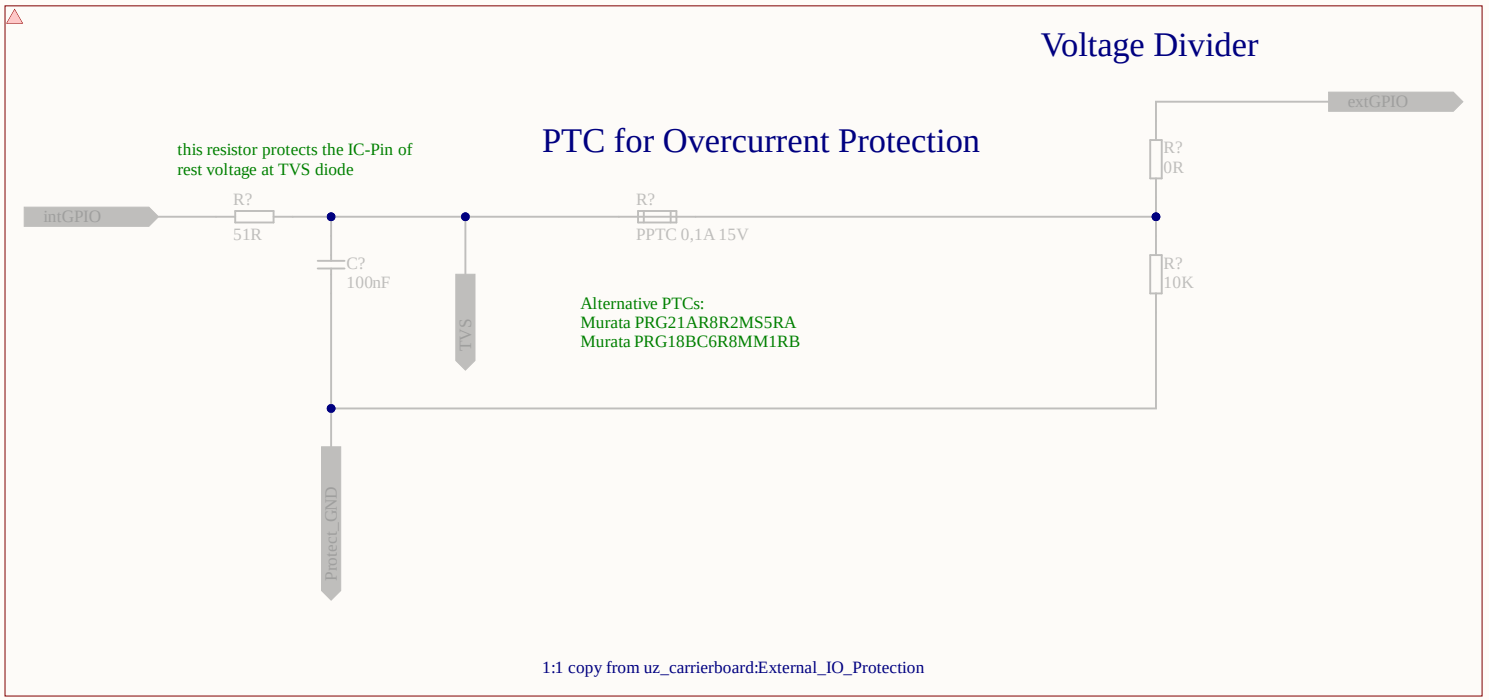
Title FPC-isoIOs-IOpQuad.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 7.3 of 34	

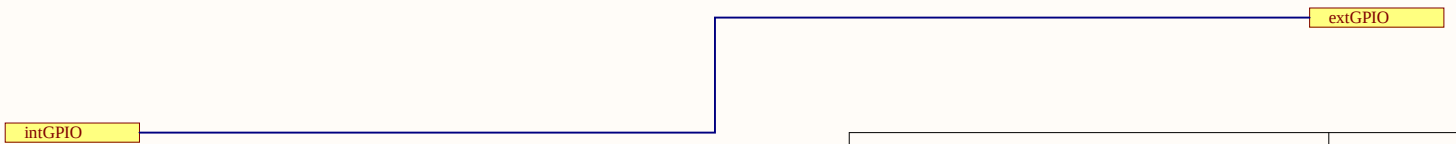




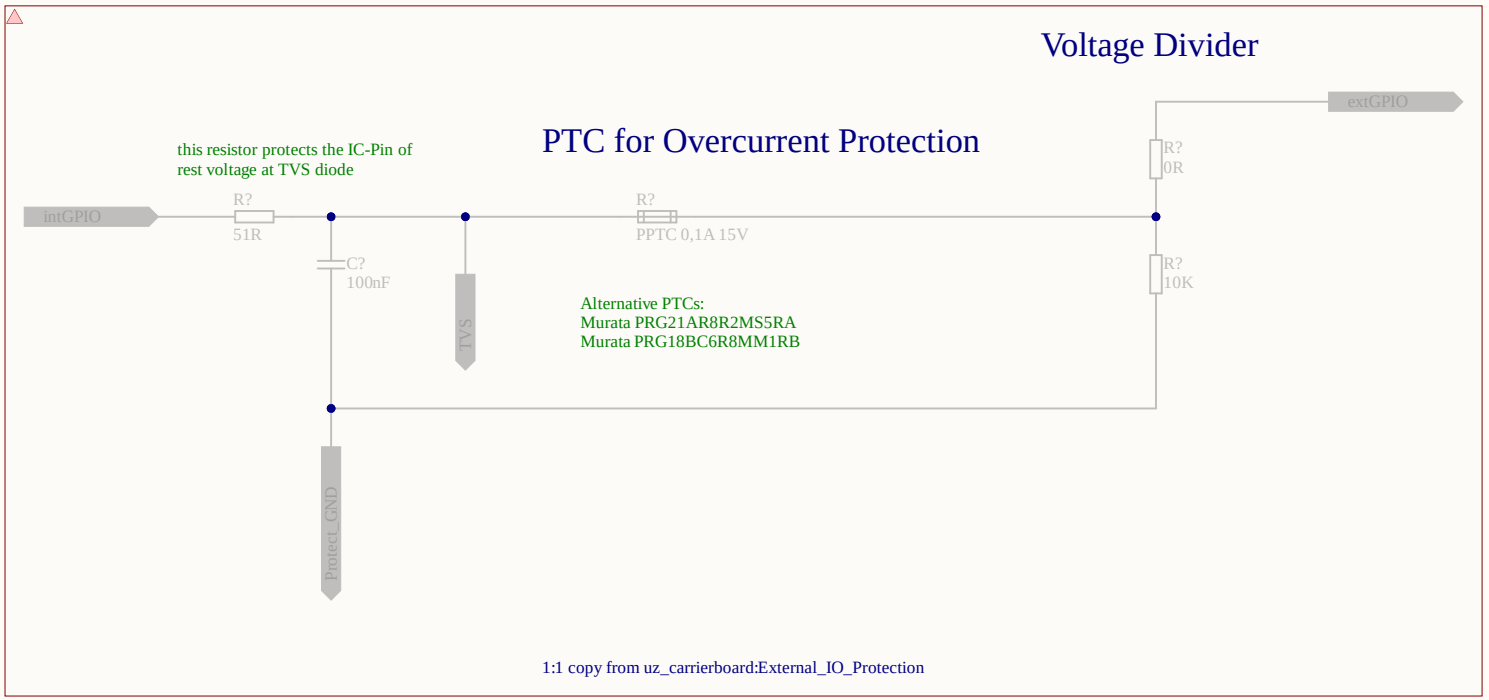
1:1 copy from uz_carrierboard:LevelShifting_Isolation

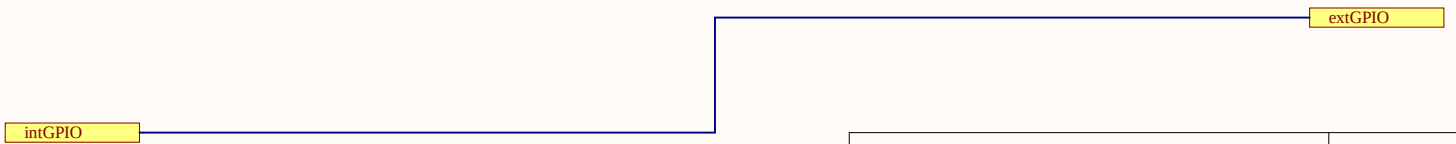
Title FPC-isoIOs-IOpQuad.SchDoc		**UltraZohm**	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 7.4 of 34	



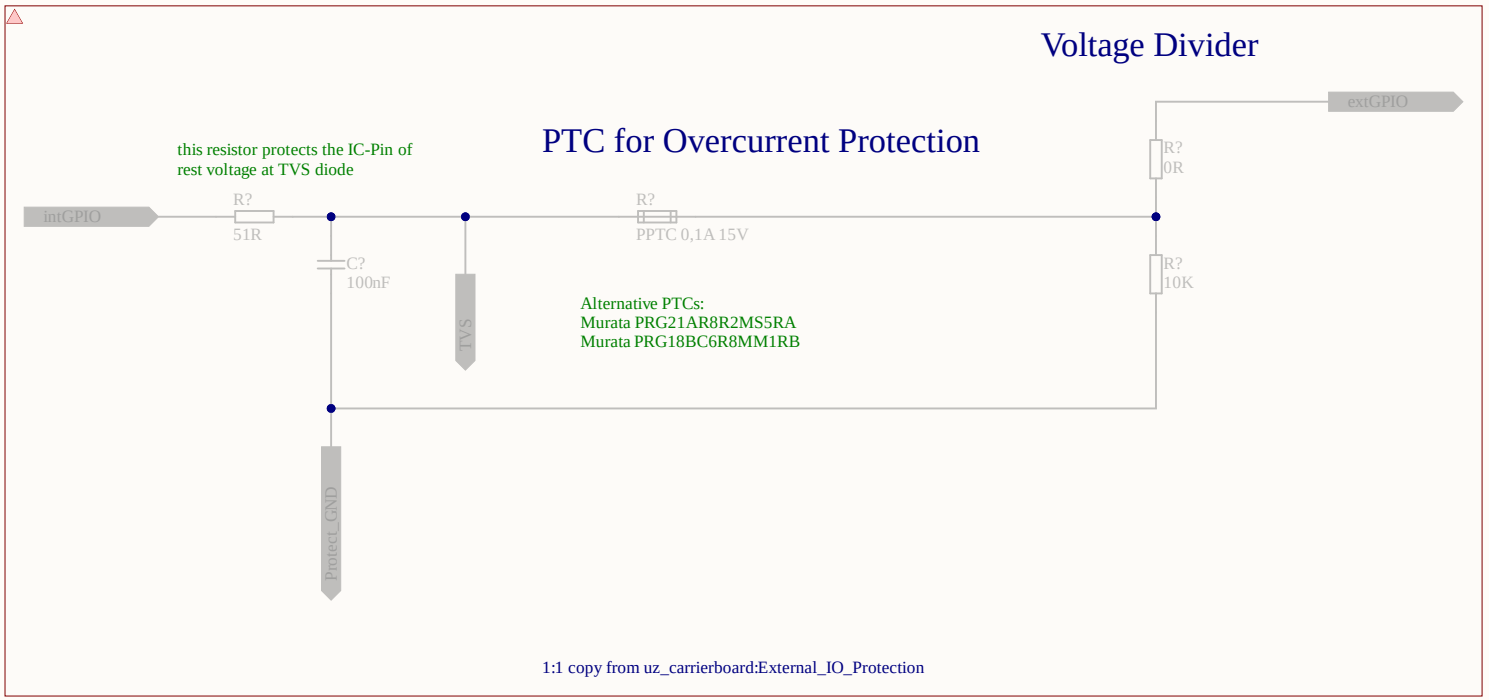


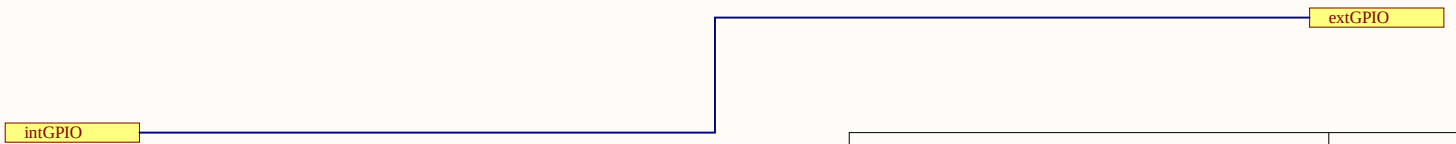
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm www.ultrazohm.com
Revision: 02	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025 Sheet 8.1.1 of 34



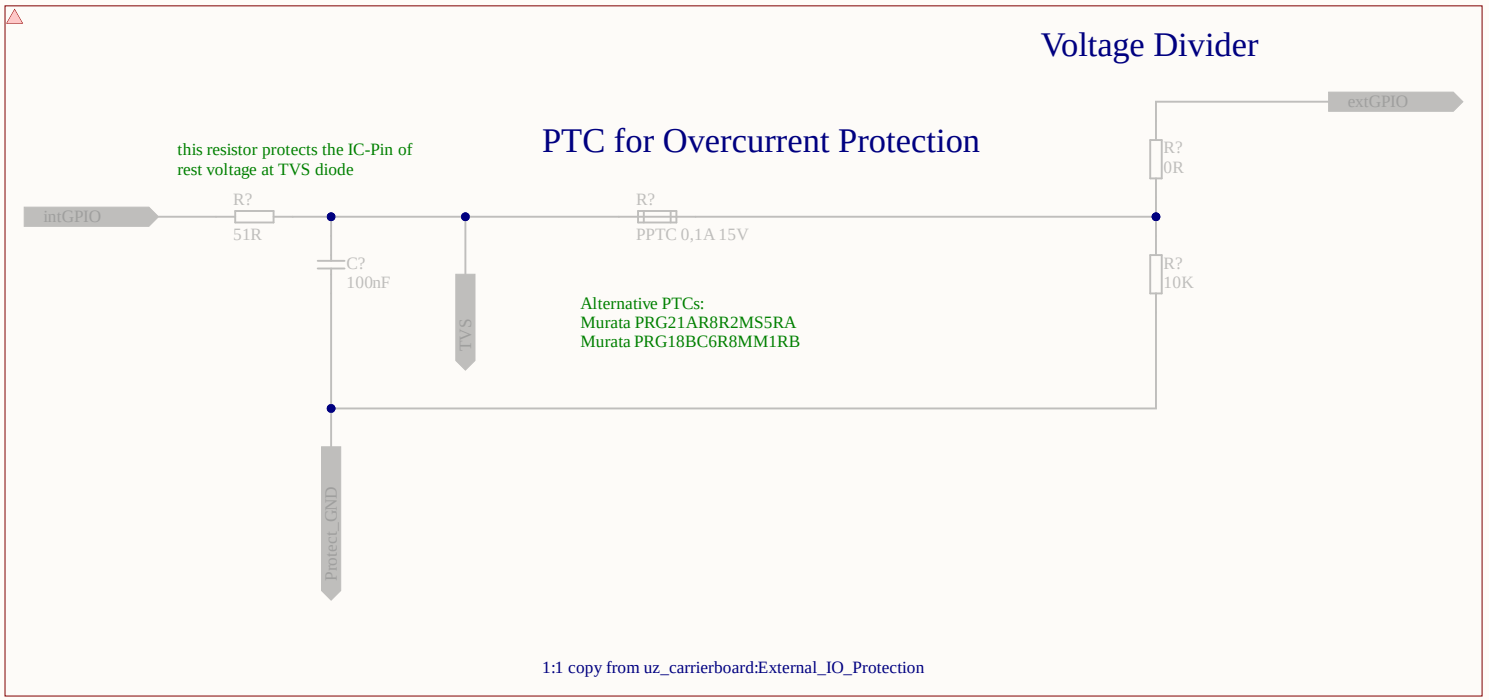


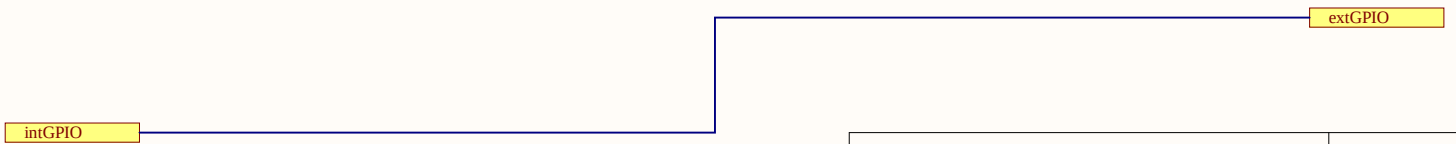
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.1.2 of 34	



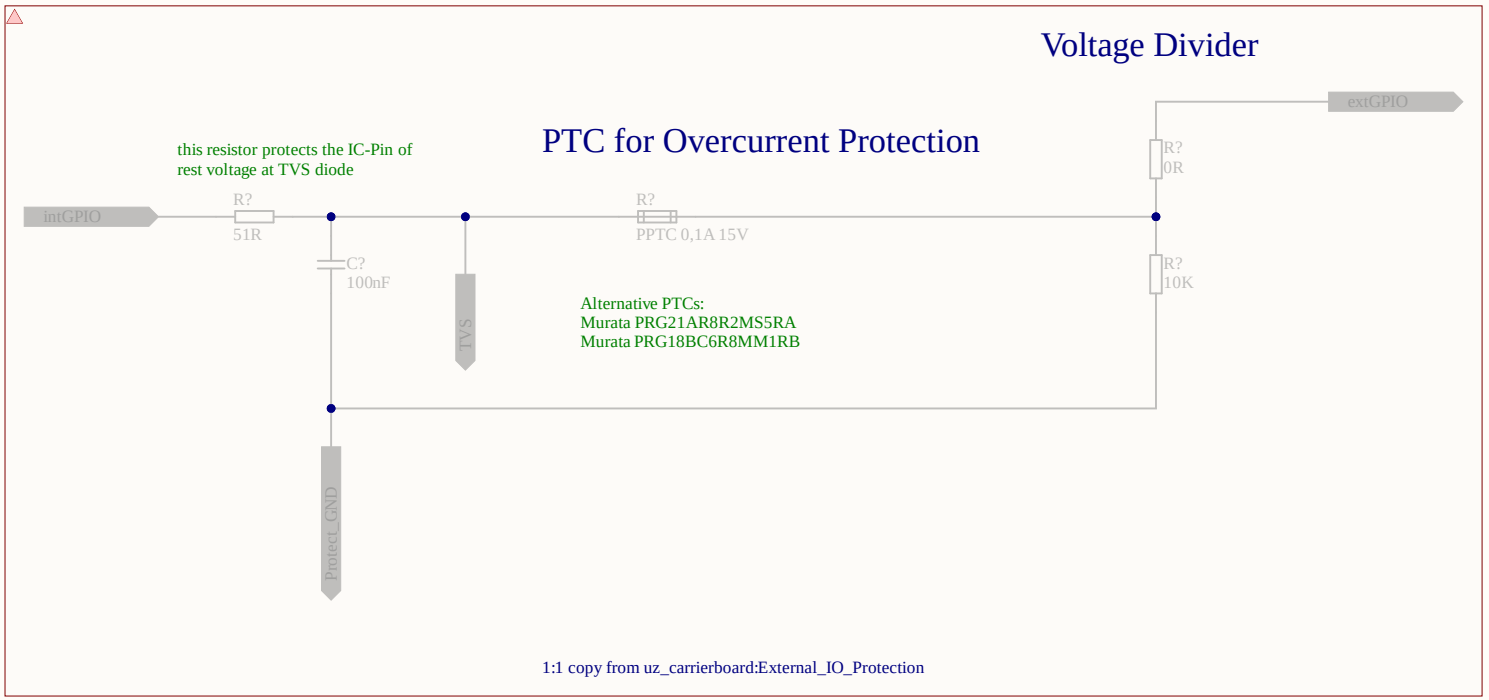


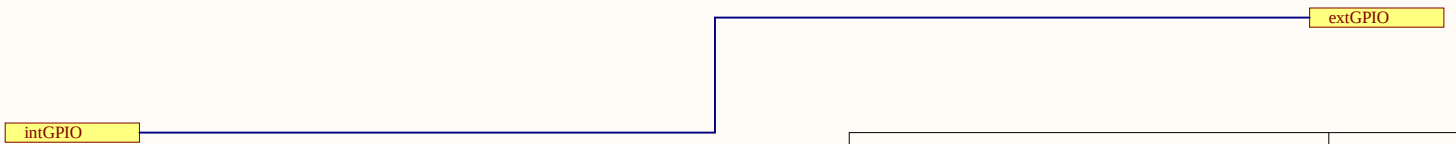
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.1.2 of 34	



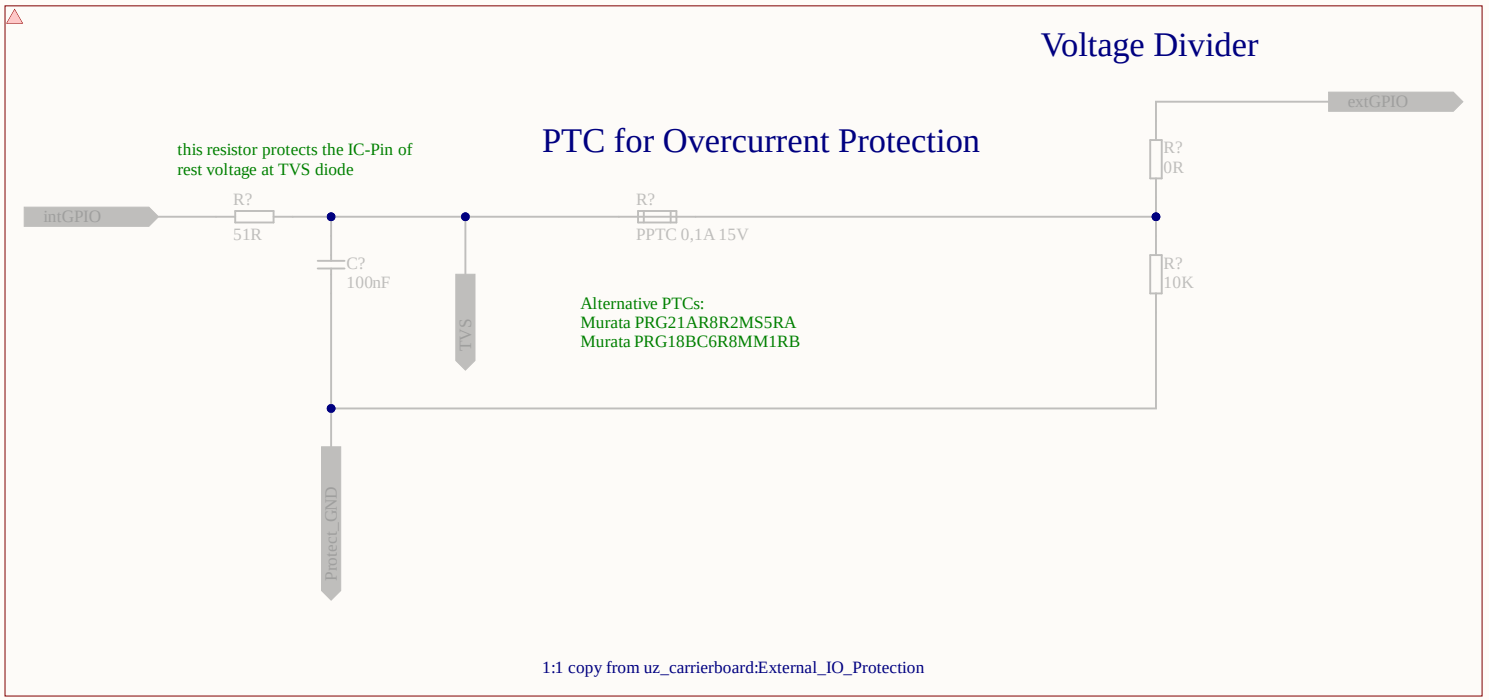


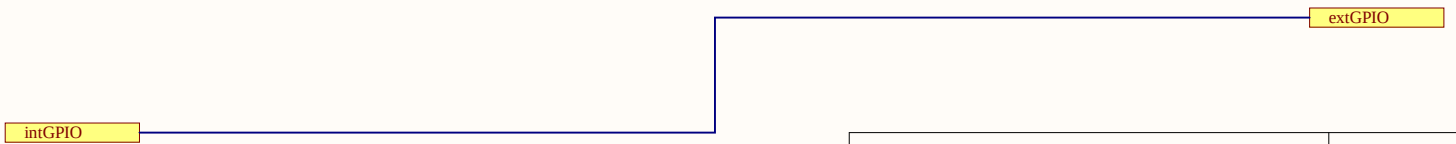
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.1.4 of 34	



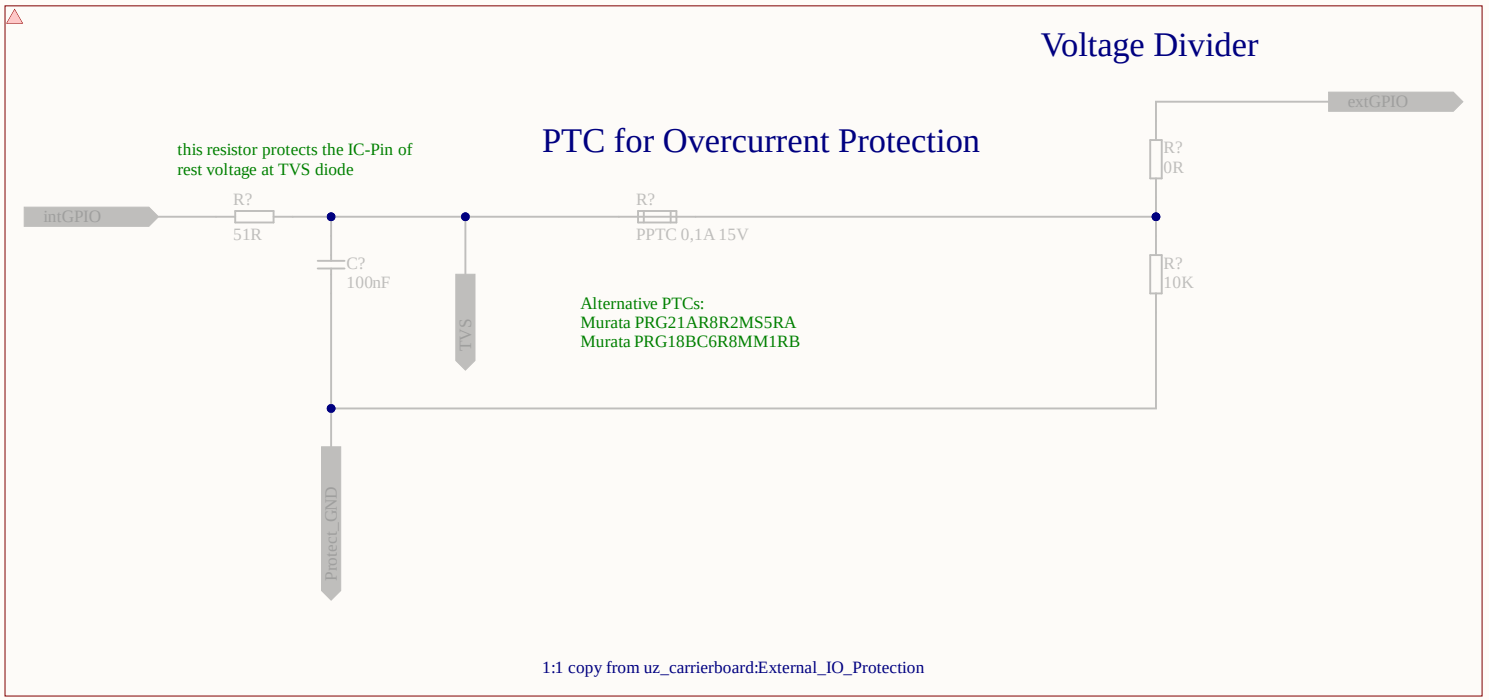


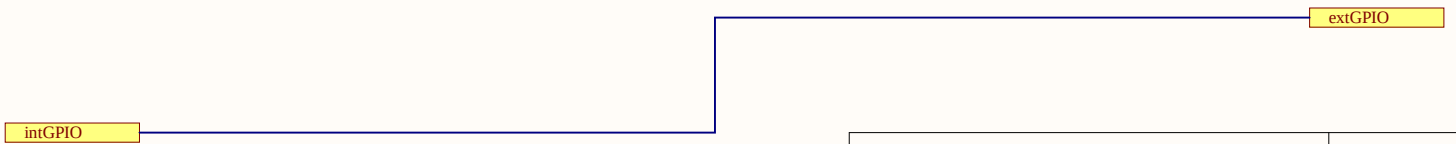
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.2.1 of 34	



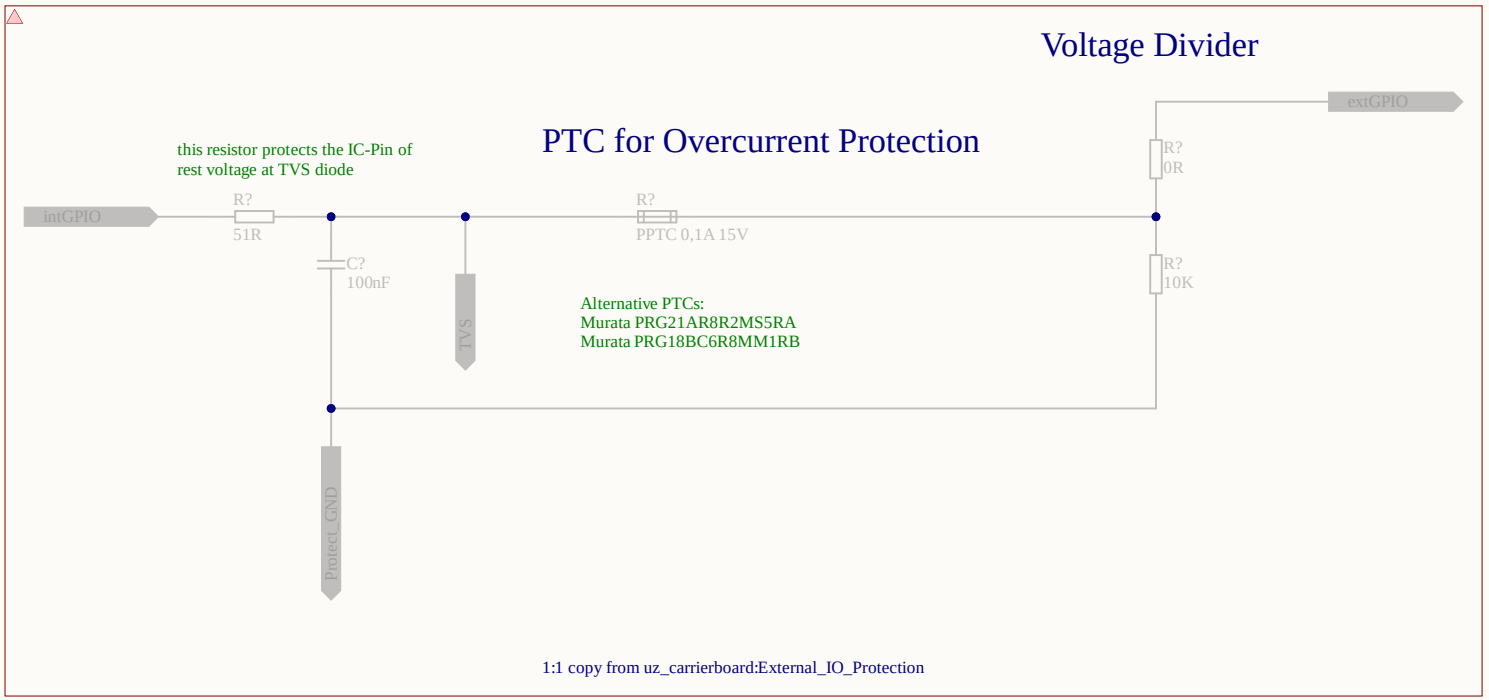


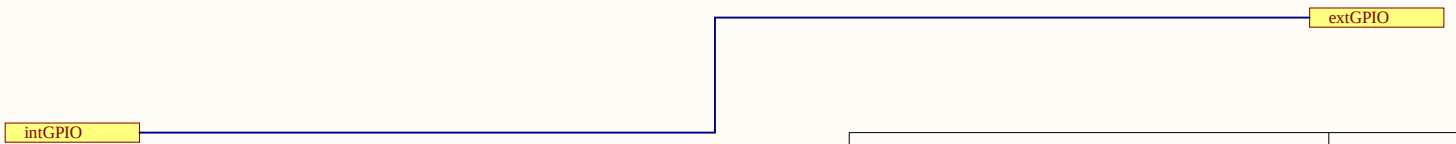
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm www.ultrazohm.com
Revision: 02	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025 Sheet 8.2.2 of 34



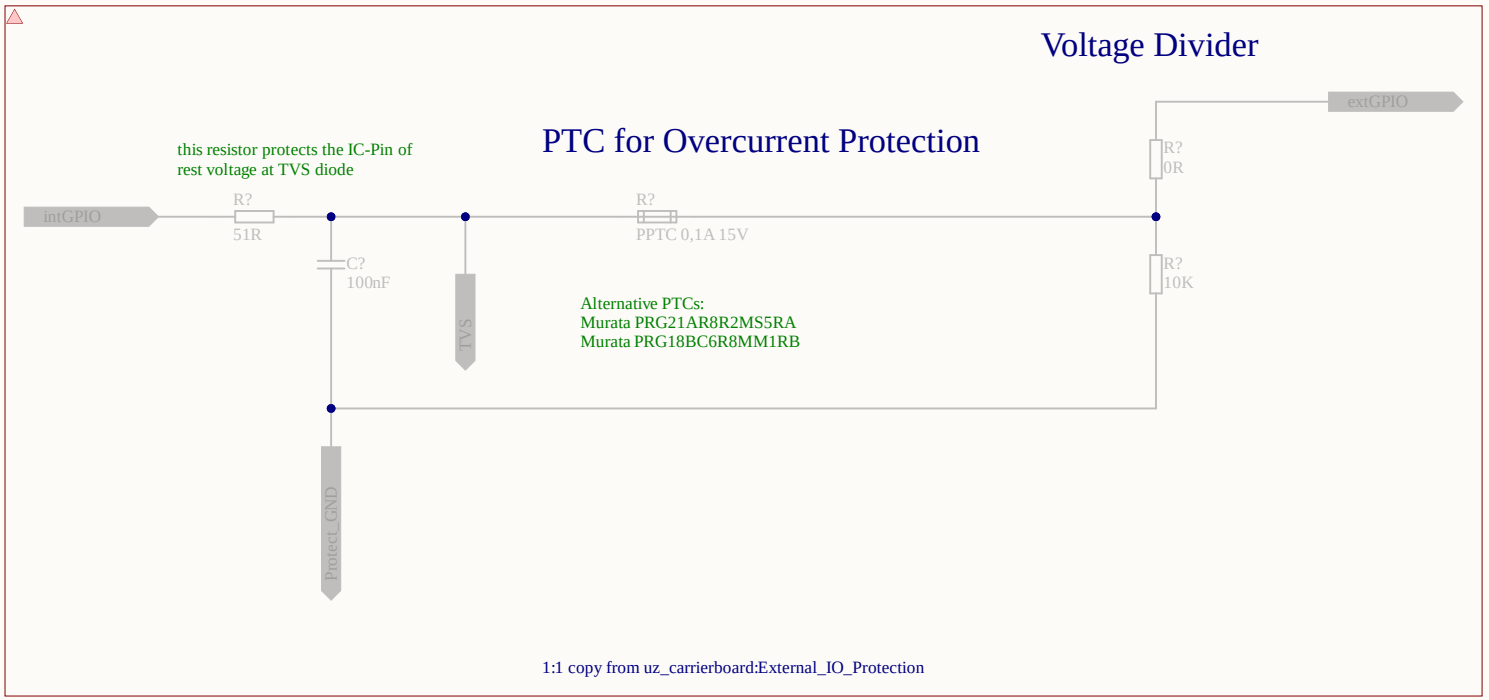


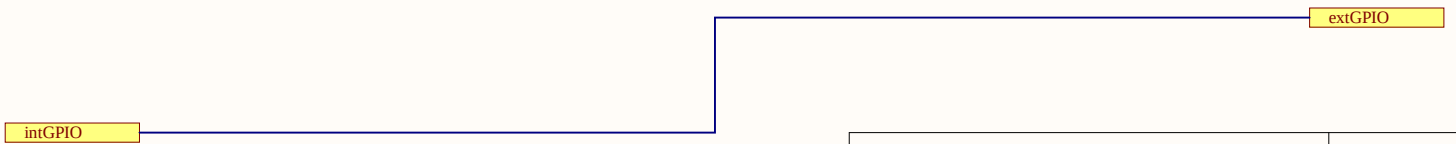
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm www.ultrazohm.com
Revision: 02	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025 Sheet 8.2.3 of 34



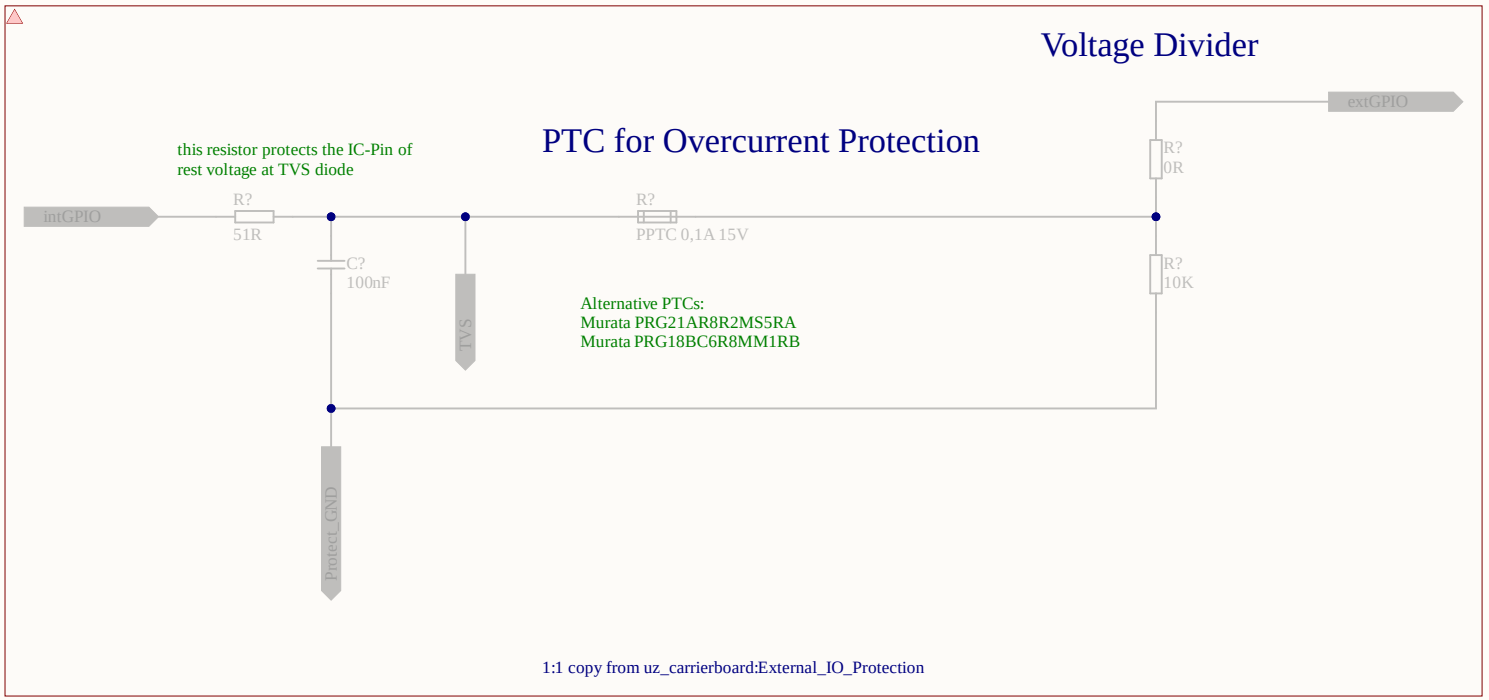


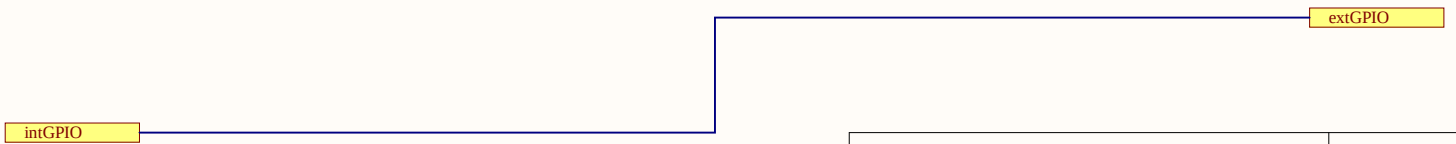
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm www.ultrazohm.com
Revision: 02	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025
		Sheet 8.2.4 of 34



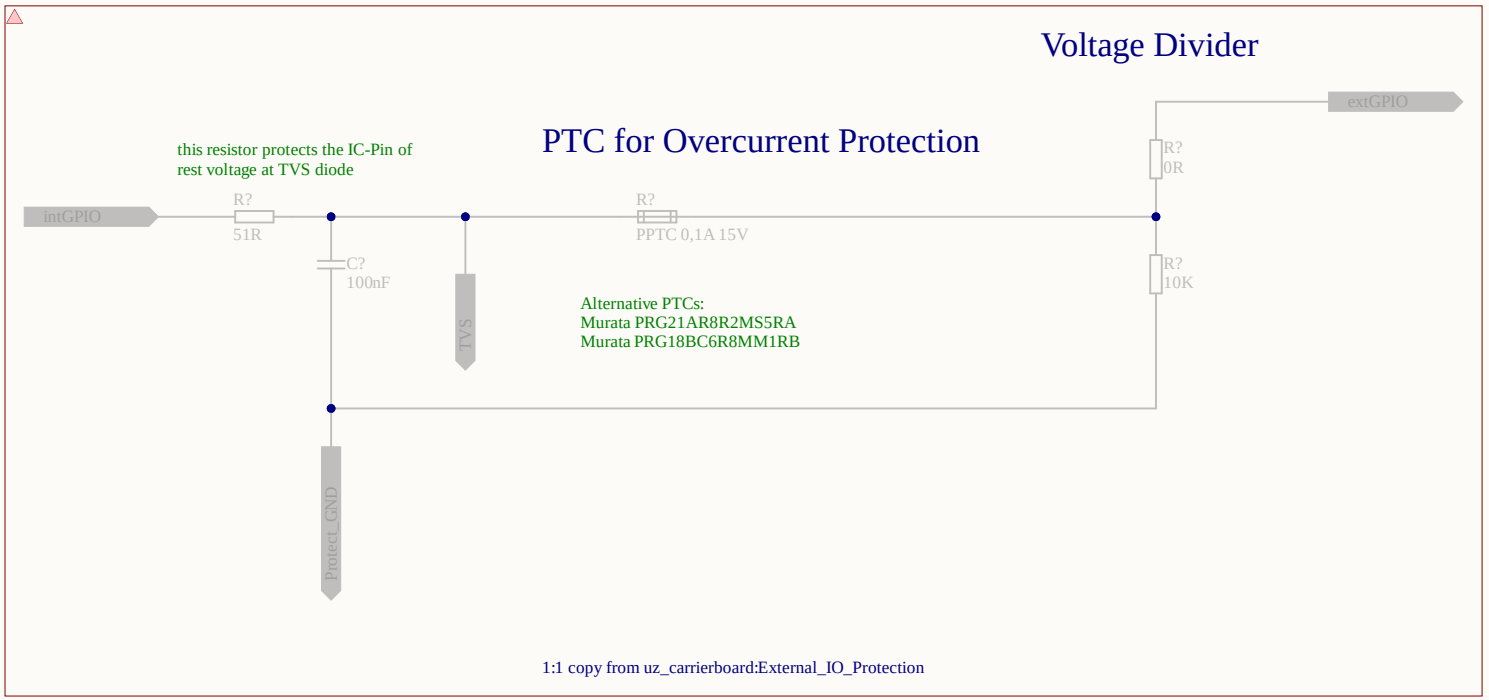


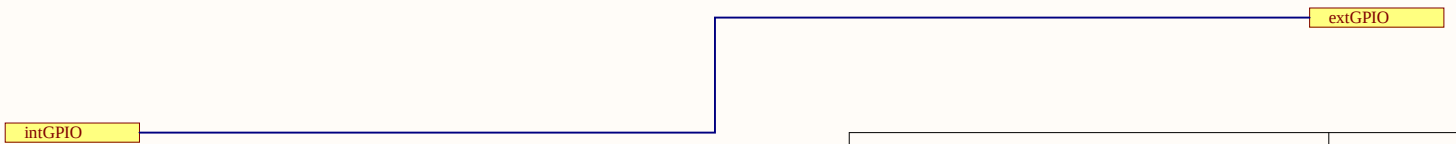
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.3.1 of 34	



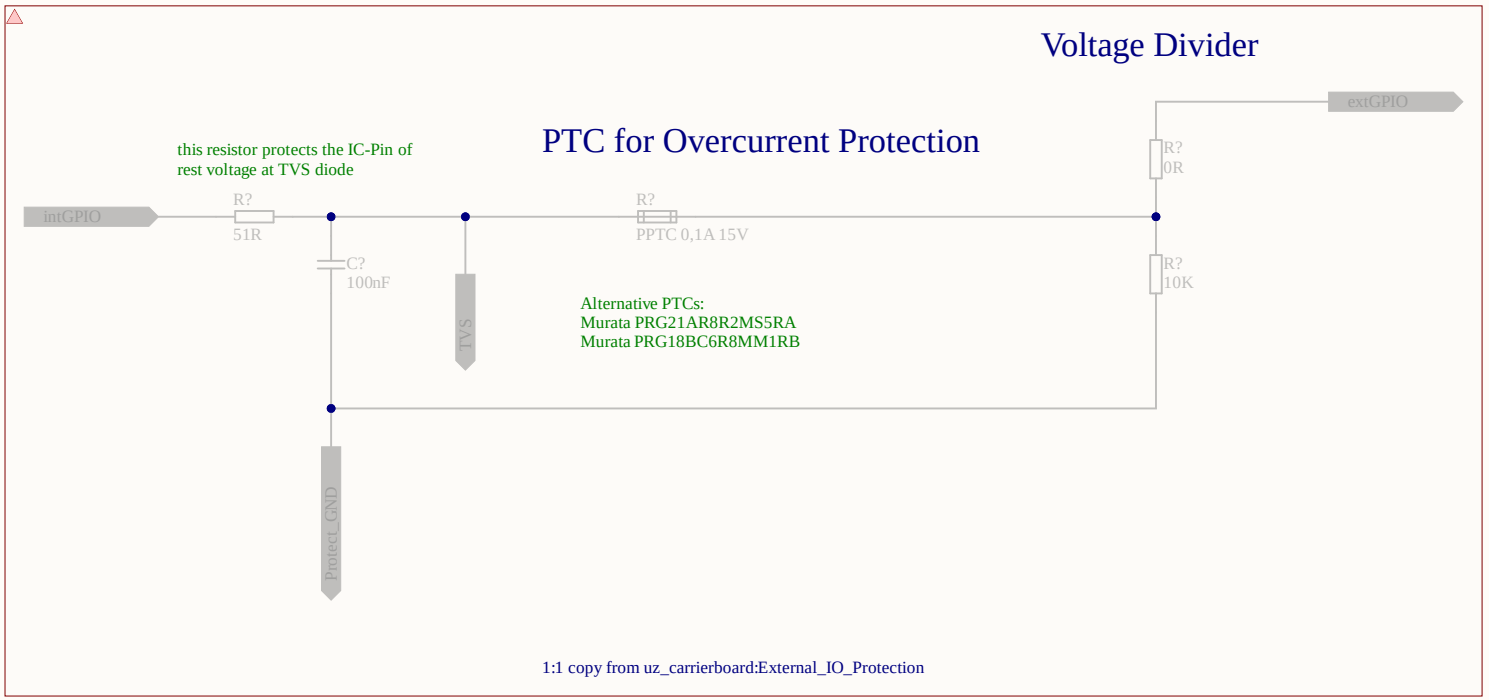


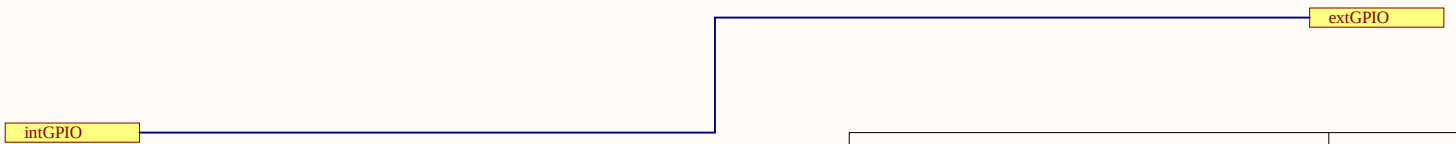
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.3.2 of 34	



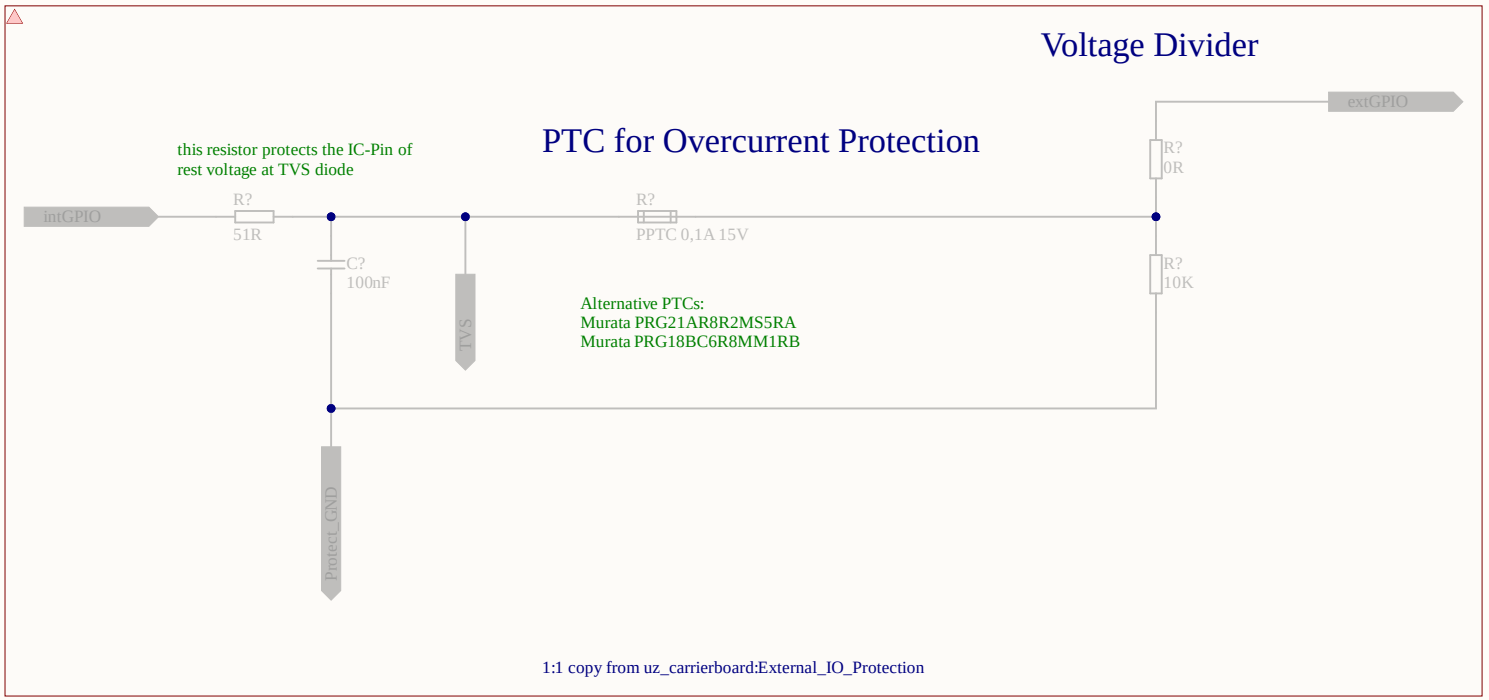


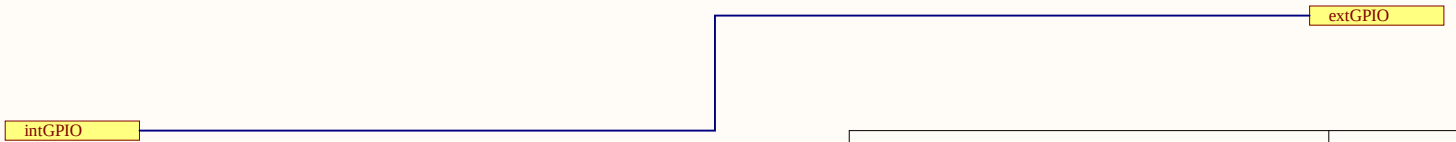
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.3.3 of 34	



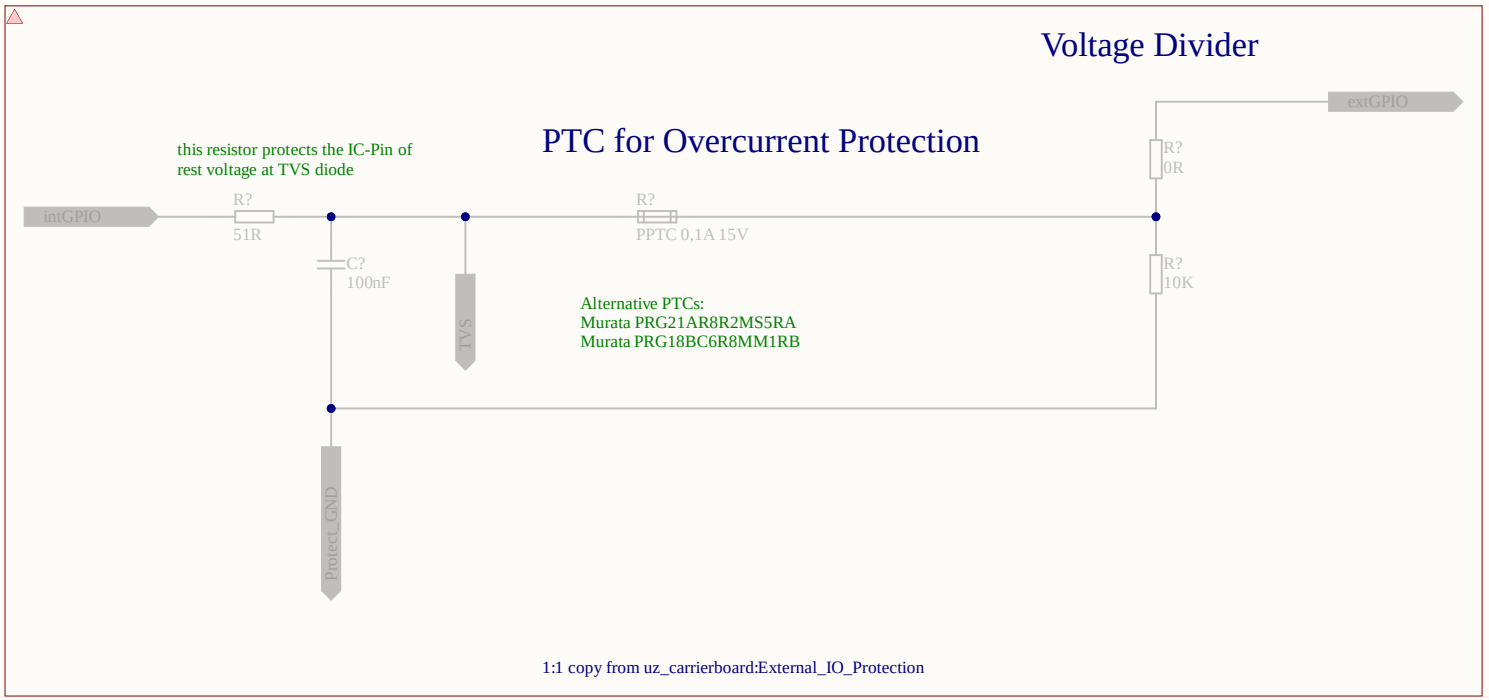


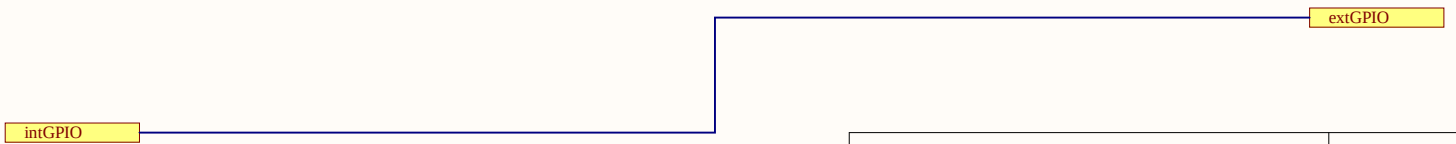
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.3.4 of 34	



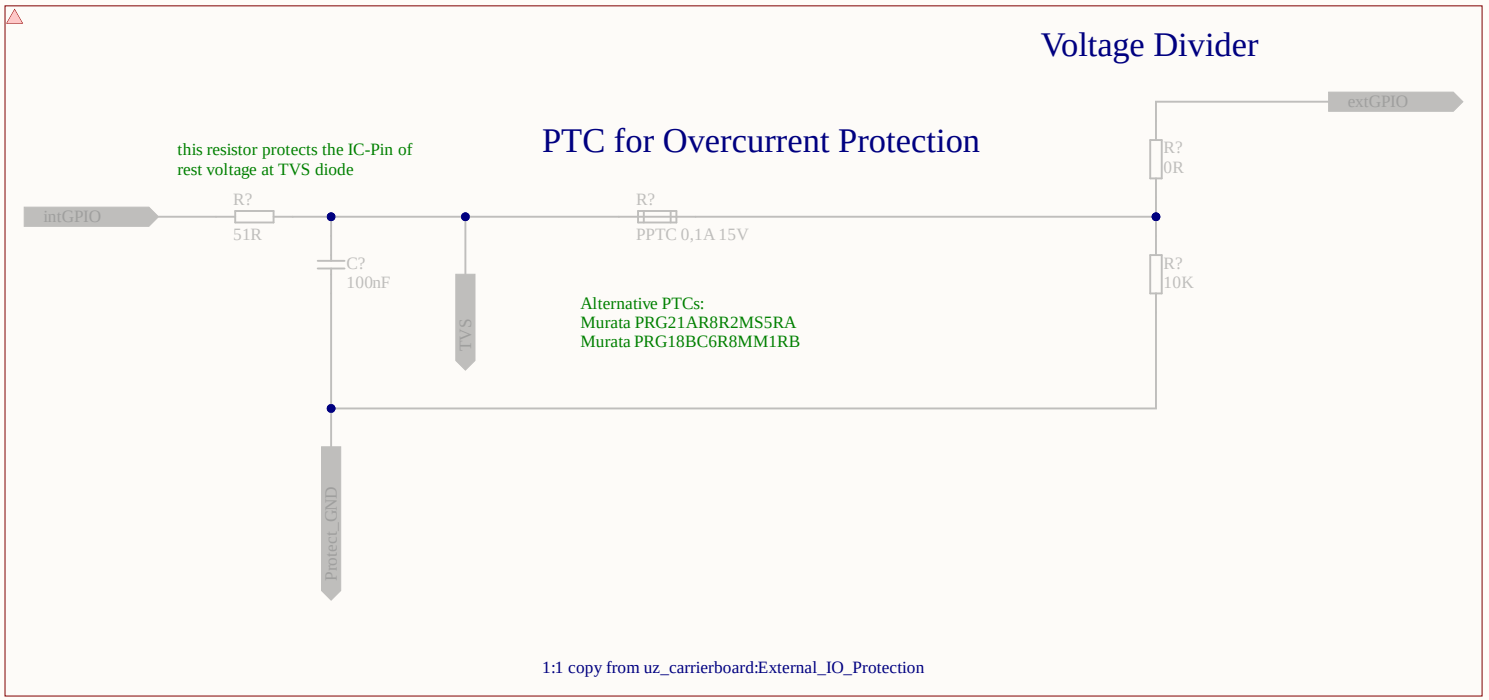


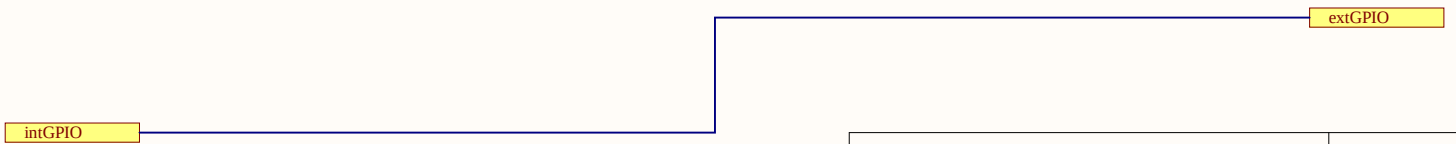
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.4.1 of 34	



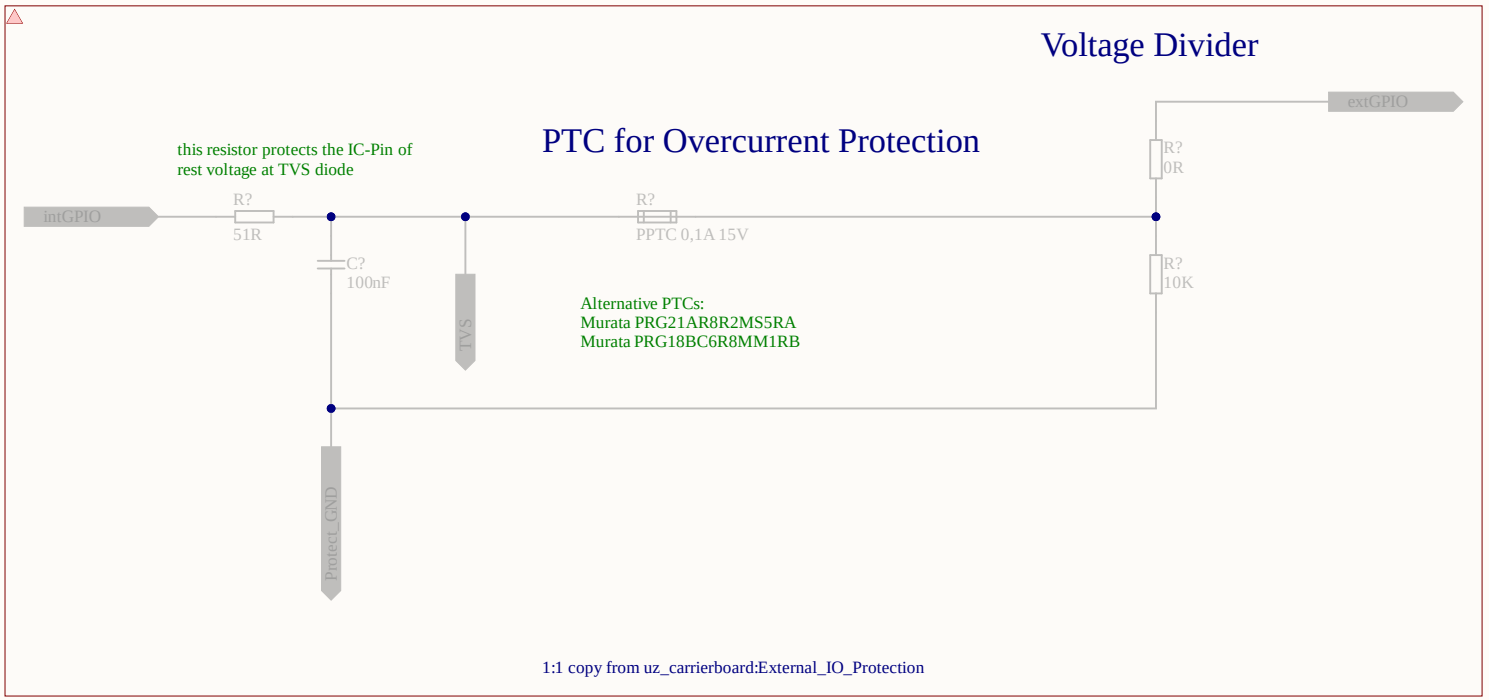


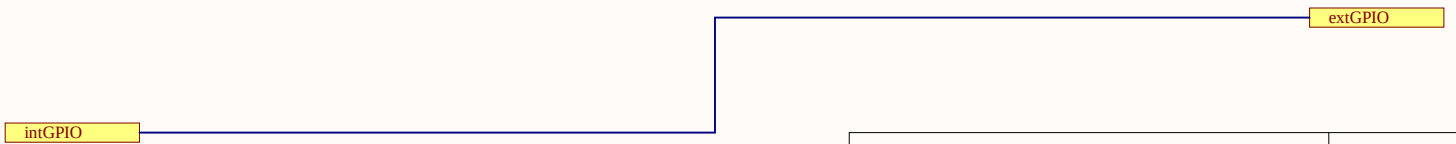
Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.4.2 of 34	



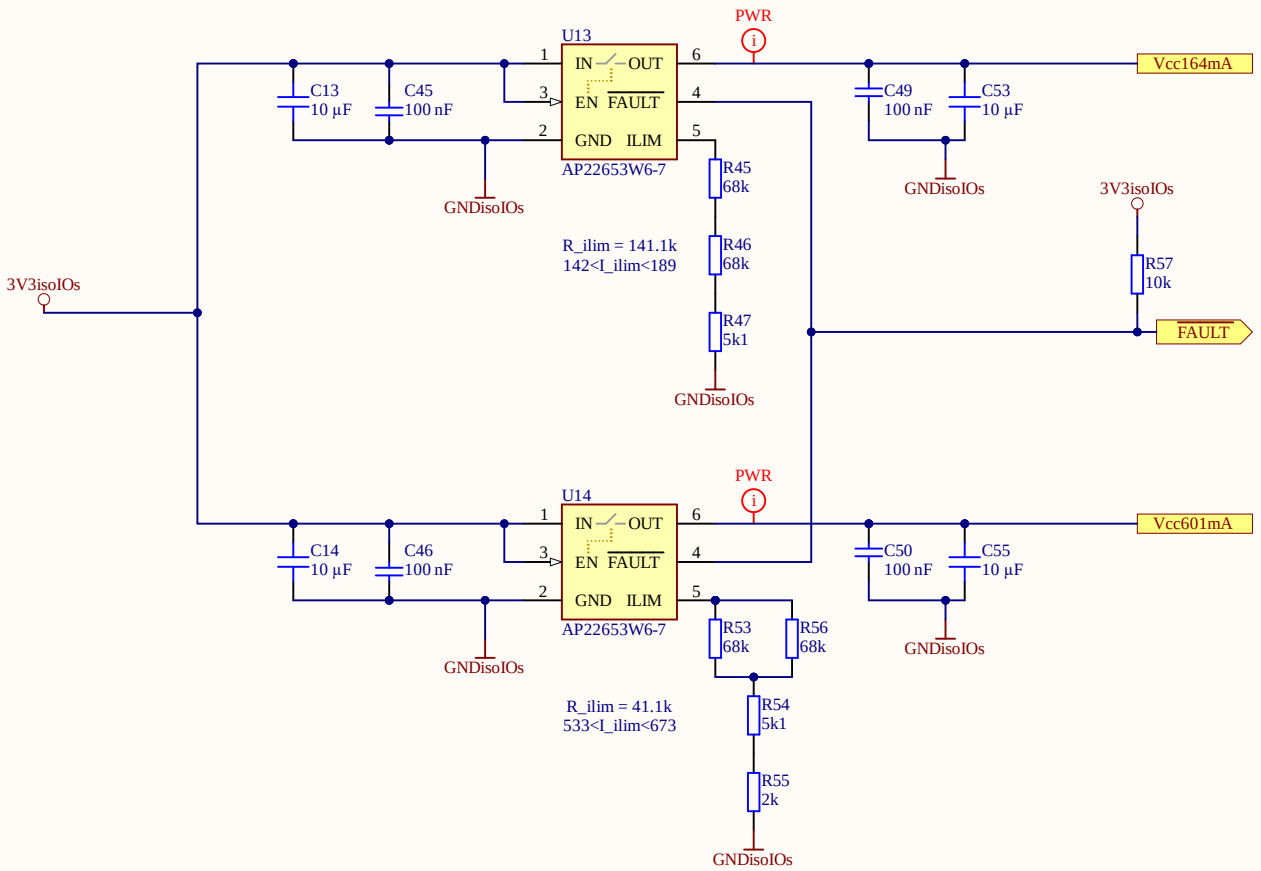


Title FPC-isoIOs-IOpSingle.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.4.3 of 34	

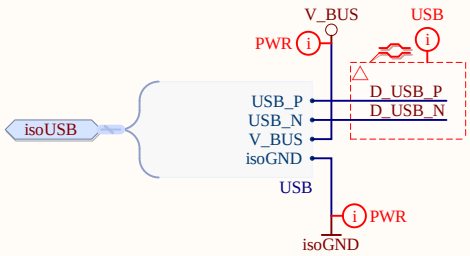




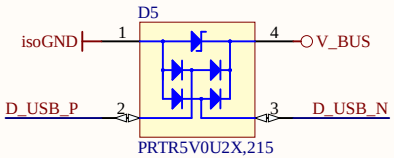
Title FPC-isoIOs-IOpSingle.SchDoc		***UltraZohm***	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 8.4.4f 34	

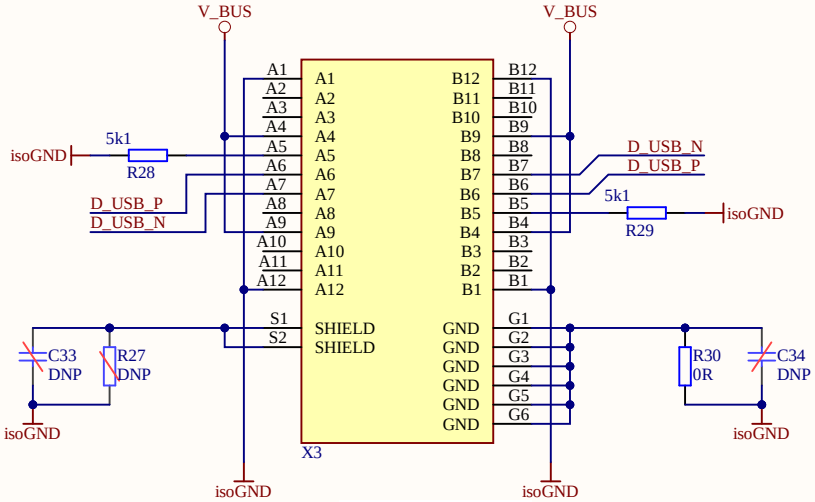


Title FPC-isoIOs-Power_Protection_AP22653.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 02	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 9 of 34	



Place GND poly on L2





Shell and mid-plate to GND as per spec.

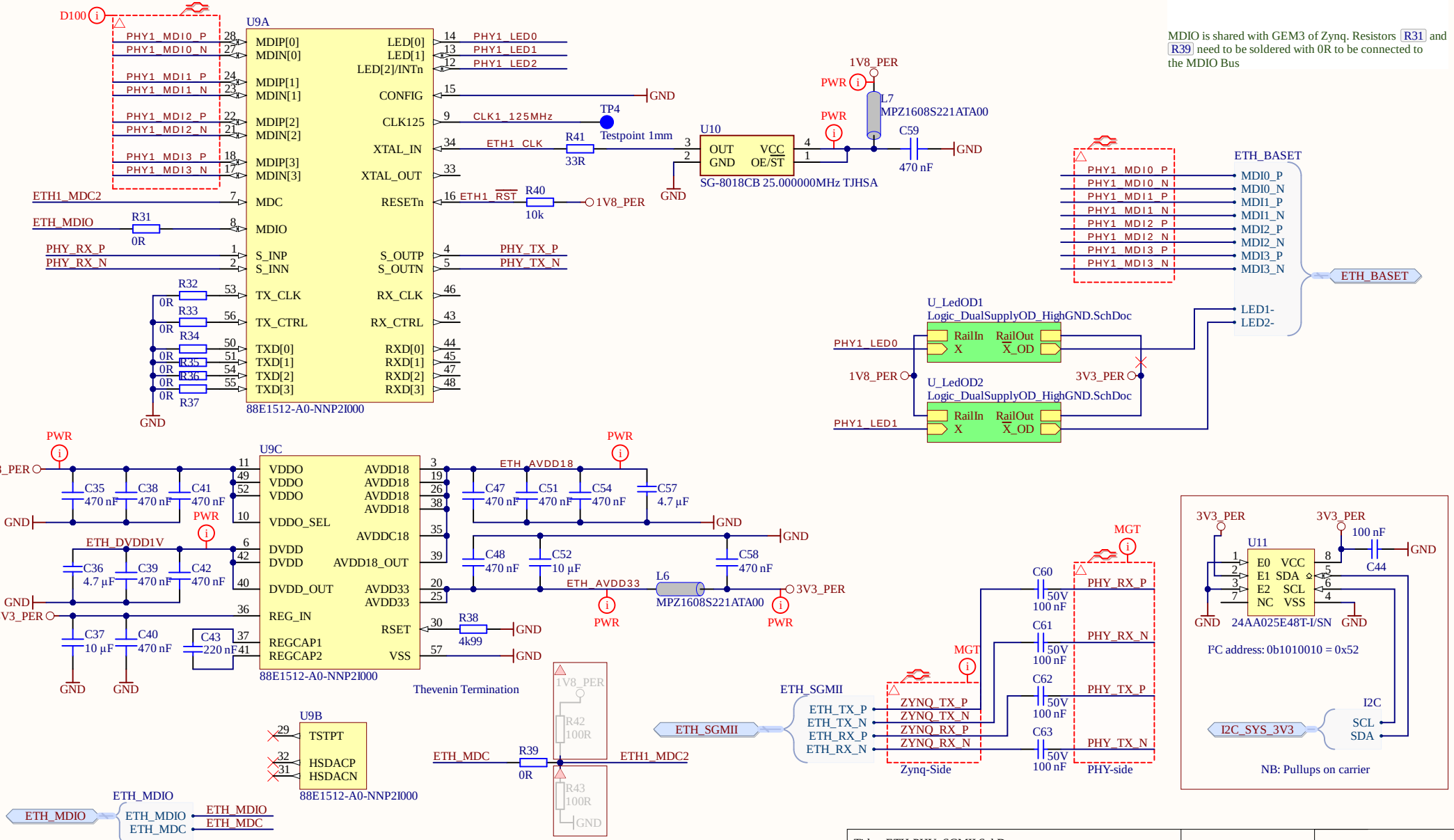
Place GND poly on 3/4 sides

HS USB-C pin assignment:
- A1/B12: GND
- A[23]/B1[10]: SS TX/RX
- A4/B9: VBus
- A5/B5: CC1/2; 5k1 GND
- A6/B6: D+
- A7/B7: D-
- A8/B8: SBU1/2; NC
- A9/B4: VBus
- A1[01]/B[32]: SS TX/RX
- A12/B1: GND

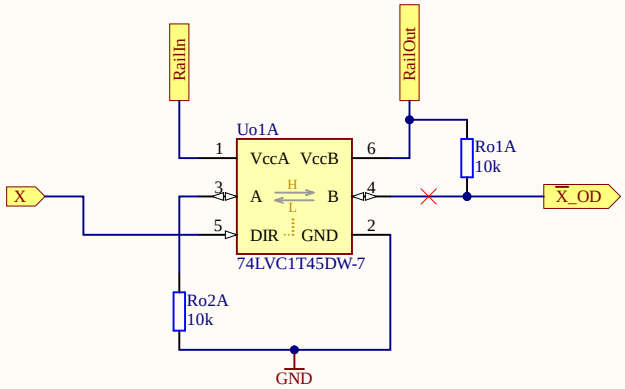
Title FPC-isoJTAG.SchDoc		UltraZohm www.ultrazohm.com
Revision: 02	Design Engineer: MG & MH	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025 Sheet 10 of 34

Config Pin 15 is low, so PHY address = 0
PHY is connected to GEM2 of Zynq via SGMII

MDIO is shared with GEM3 of Zynq. Resistors R31 and R39 need to be soldered with 0R to be connected to the MDIO Bus

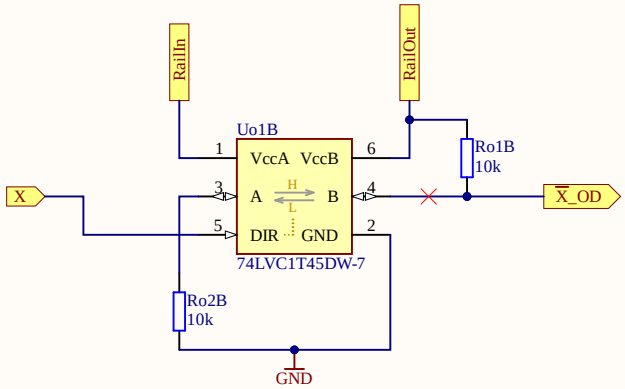


Title ETH-PHY_SGMII.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 11 of 34	



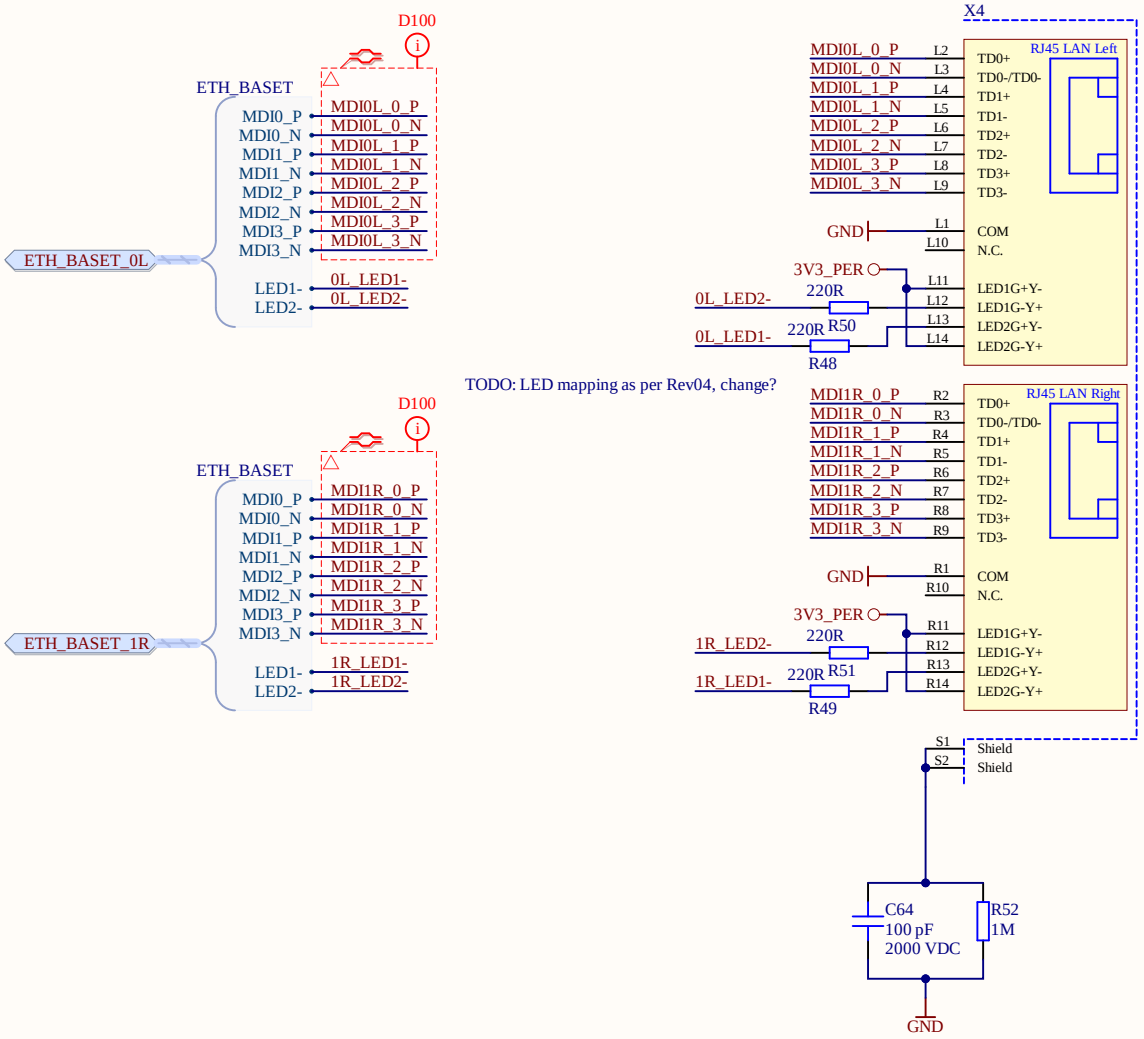
X:	nX_OD:
high	GND
low	Open

Title Logic_DualSupplyOD_HighGND.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 02	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 12.1of 34	

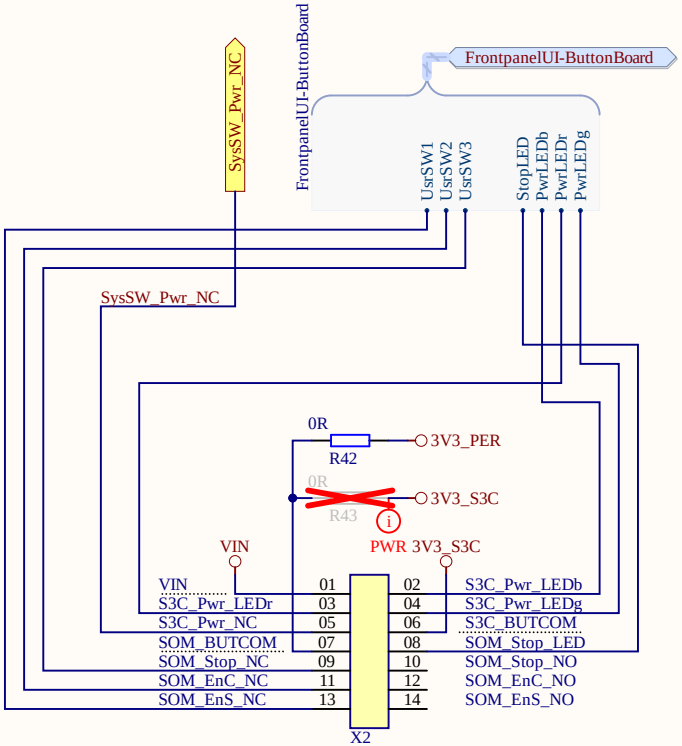


X:	nX_OD:
high	GND
low	Open

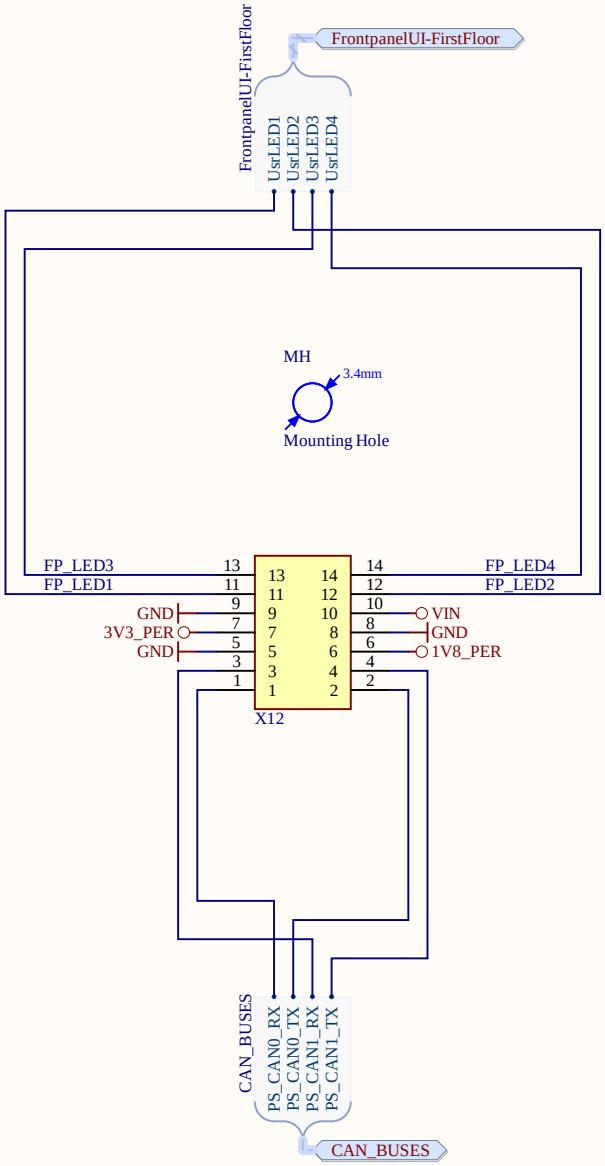
Title	Logic_DualSupplyOD_HighGND.SchDoc	UltraZohm www.ultrazohm.com	
Revision: 02	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 12.2 of 34	



Title FPC-ETH-DualRJ45.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 02	Design Engineer: MG & MH		
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 13 of 34	



Title PCB-ButtonBoard.SchDoc		***UltraZohm***	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 14 of 34	



Title PCB-FirstFloor.SchDoc		UltraZohm	
Revision: 02	Design Engineer: MG & MH	www.ultrazohm.com	
Project: uz_frontpanel_main.PrjPCB		Date: 30/04/2025	
		Sheet 15 of 34	