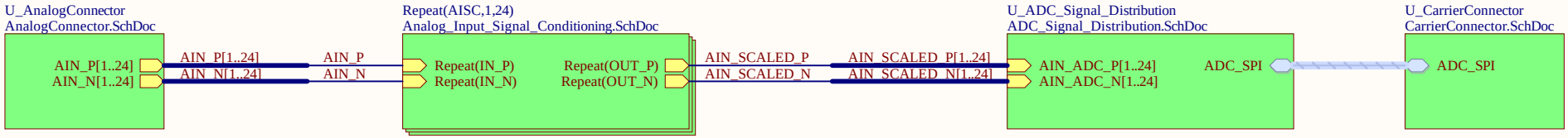
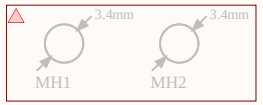
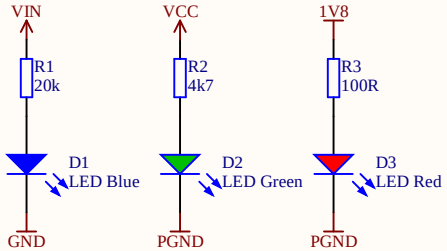


U_Power_Supply
Power_Supply.SchDoc

U_Block_Diagram
Block_Diagram.SchDoc





UZ_A_MAX11331
Project1

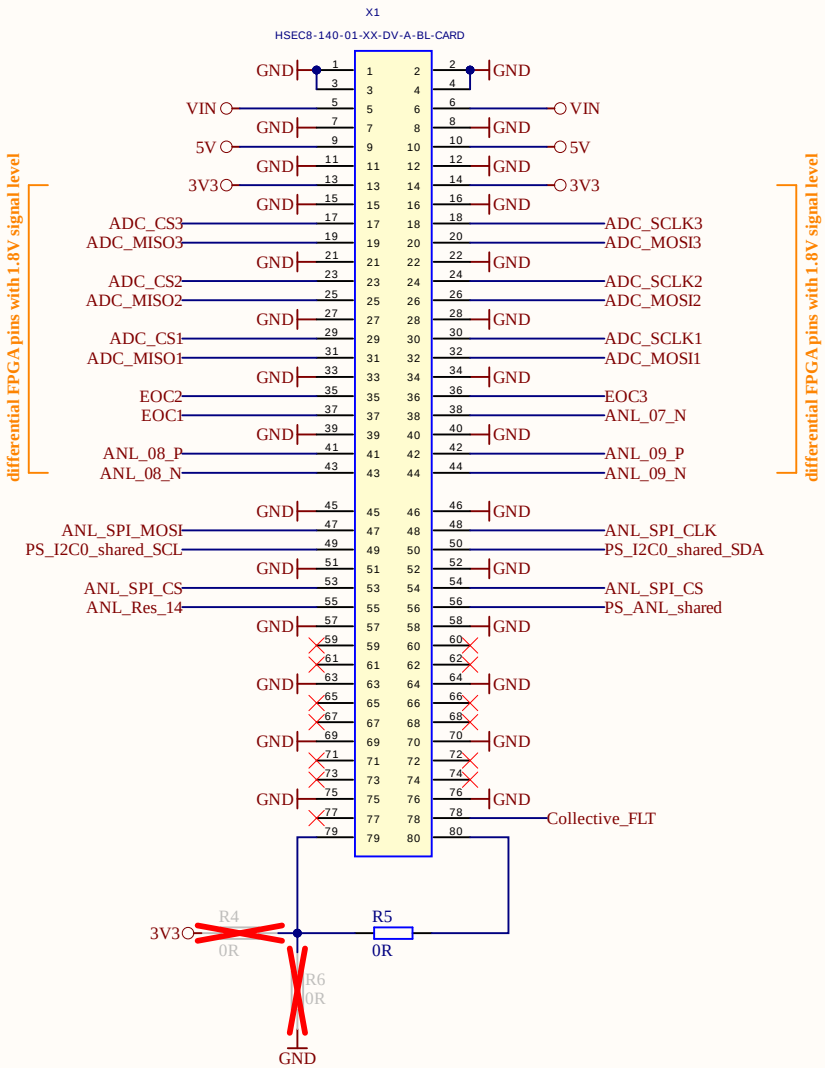
Revision1

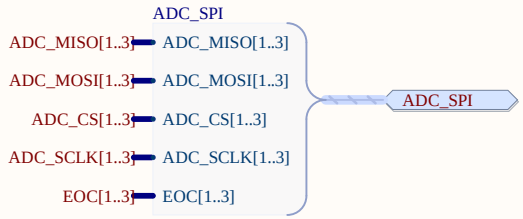
Designer1

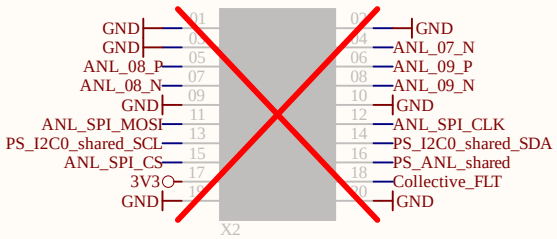
LOGO1

Serial
Serial1

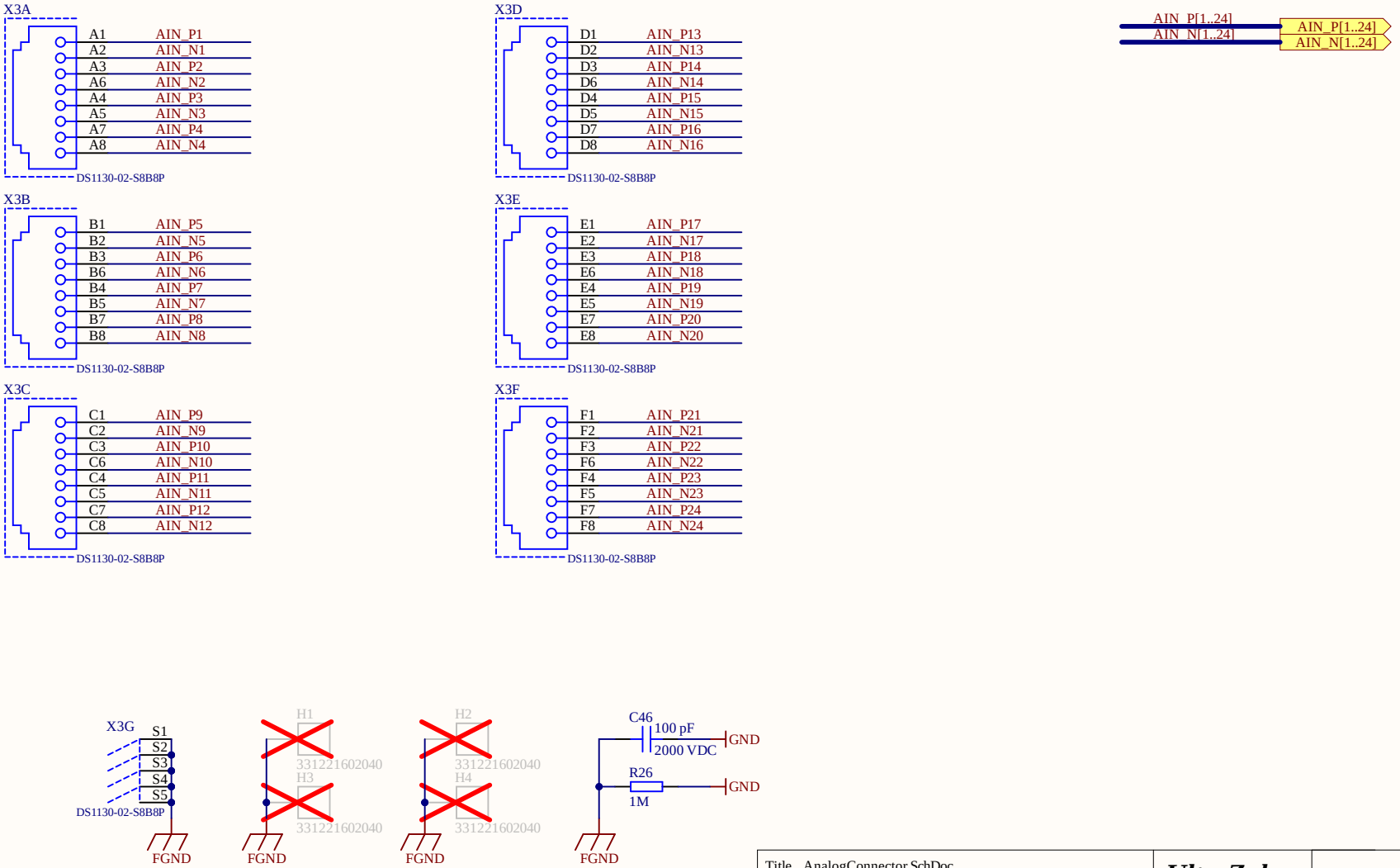
Title TopSheet.SchDoc		***UltraZohm***	
Revision: Rev01	Design Engineer: Andreas Geiger	www.ultrazohm.com	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	
		Sheet 1 of 36	



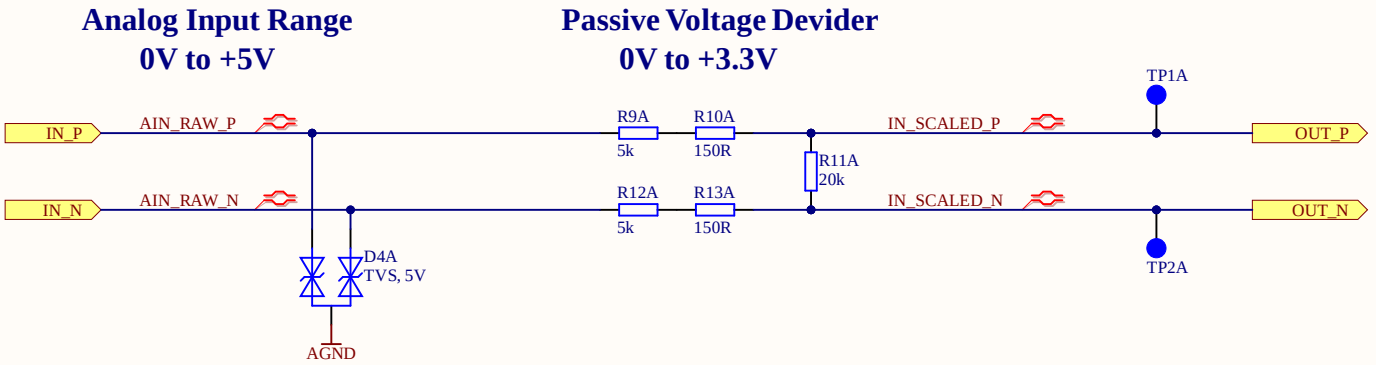




Title CarrierConnector.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 2 of 36



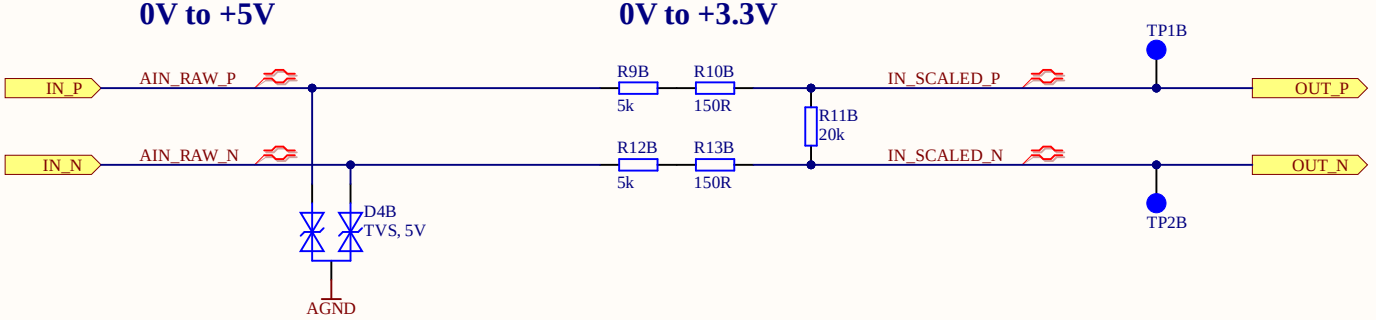
Title AnalogConnector.SchDoc		UltraZohm www.ultrazohm.com	
Revision: Rev01	Design Engineer: Andreas Geiger		
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	Sheet 3 of 36



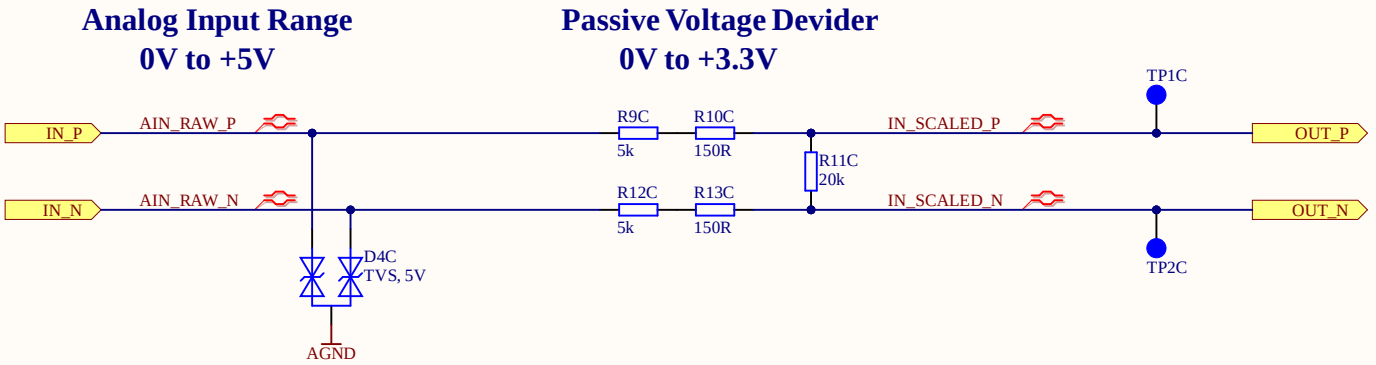
Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm	
Revision: Rev01	Design Engineer: Andreas Geiger	www.ultrazohm.com	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	
		Sheet 4.1 of 36	

Analog Input Range
0V to +5V

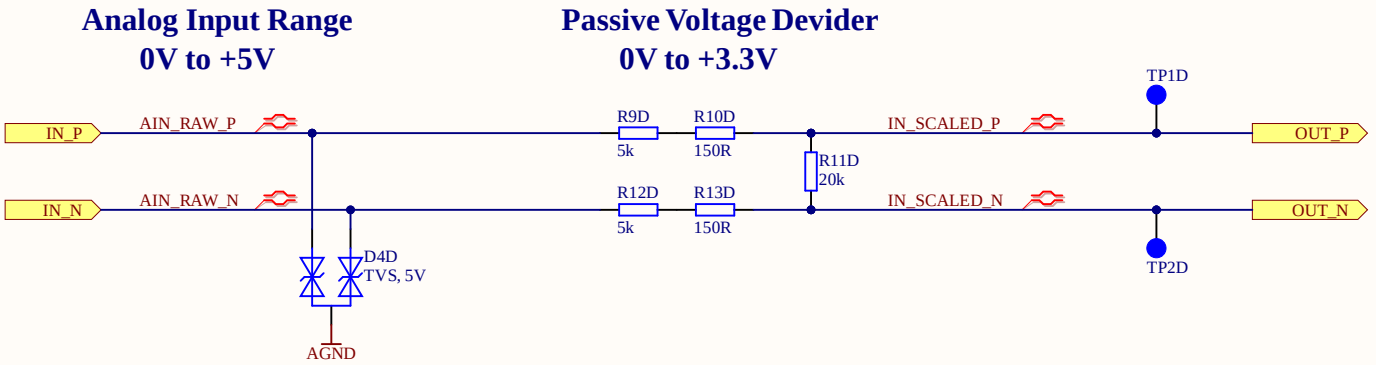
Passive Voltage Devider
0V to +3.3V



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 4.2 of 36



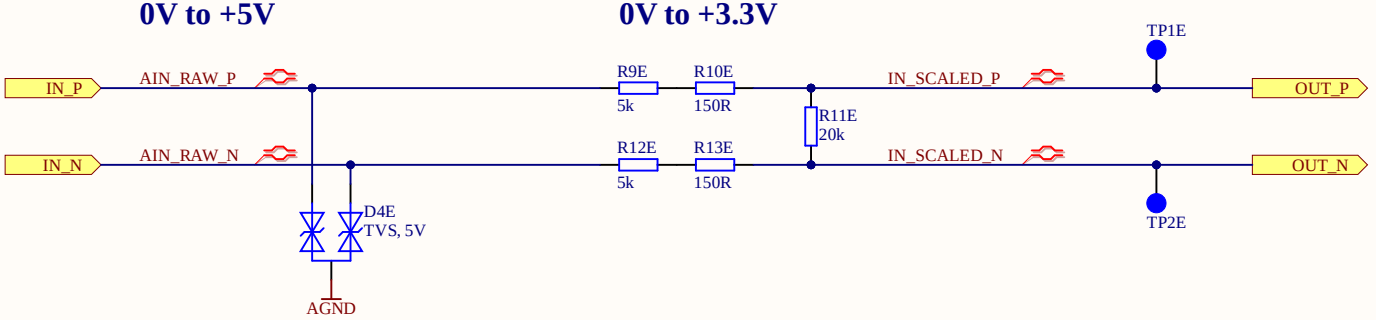
Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com	
Revision: Rev01	Design Engineer: Andreas Geiger		
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	Sheet 4.3 of 36



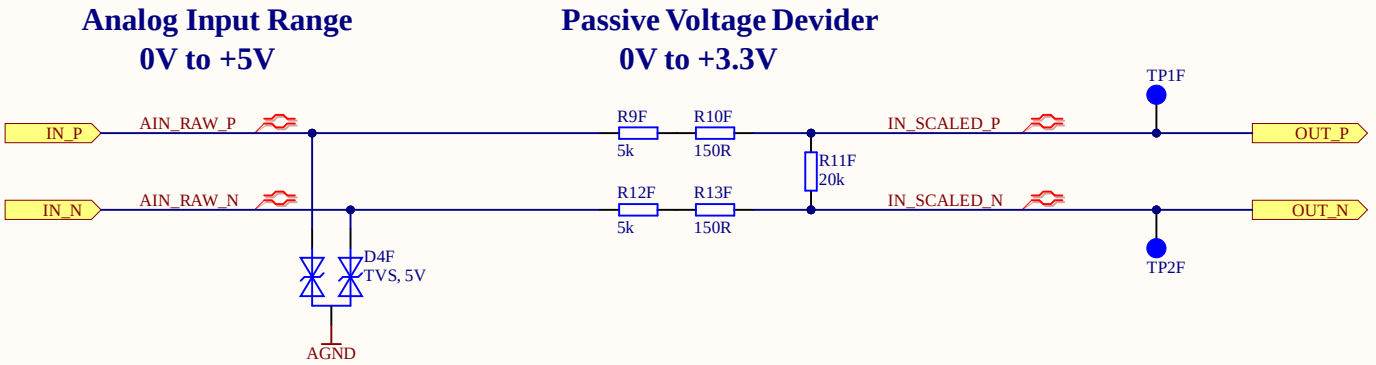
Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm	
Revision: Rev01	Design Engineer: Andreas Geiger	www.ultrazohm.com	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	
		Sheet 4.4 of 36	

Analog Input Range
0V to +5V

Passive Voltage Devider
0V to +3.3V



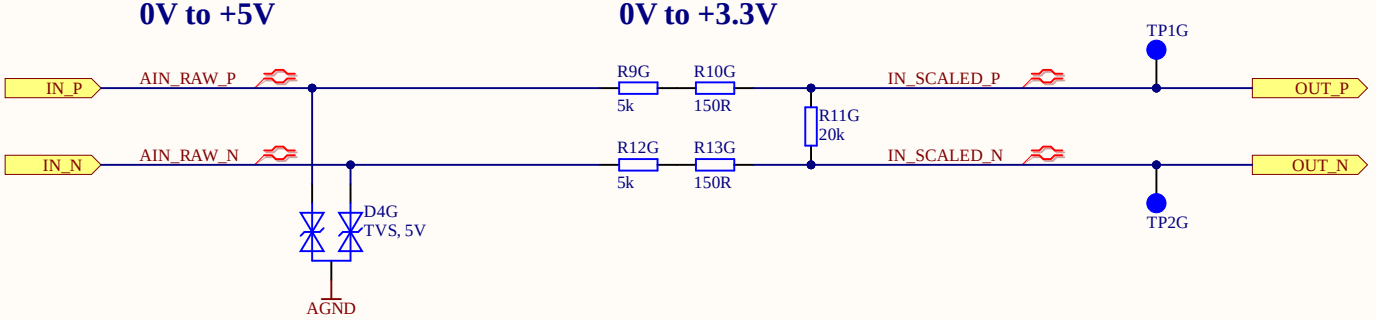
Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 4.5 of 36



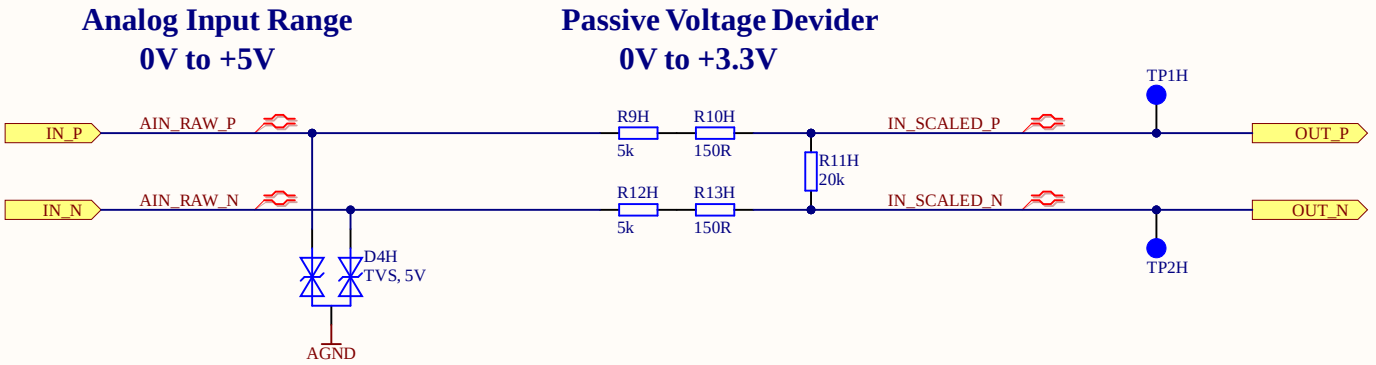
Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm	
Revision: Rev01	Design Engineer: Andreas Geiger	www.ultrazohm.com	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	
		Sheet 4.6 of 36	

Analog Input Range
0V to +5V

Passive Voltage Devider
0V to +3.3V



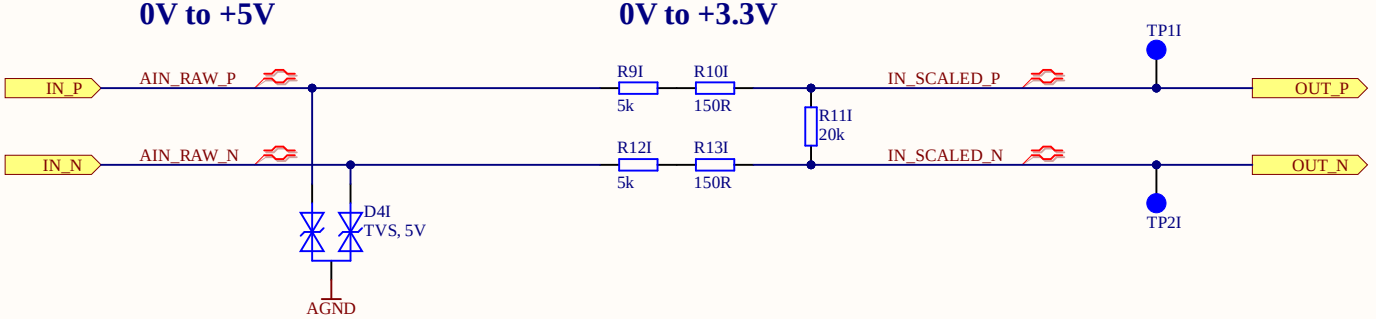
Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 4.7 of 36



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm	
Revision: Rev01	Design Engineer: Andreas Geiger	www.ultrazohm.com	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	
		Sheet 4.8 of 36	

Analog Input Range
0V to +5V

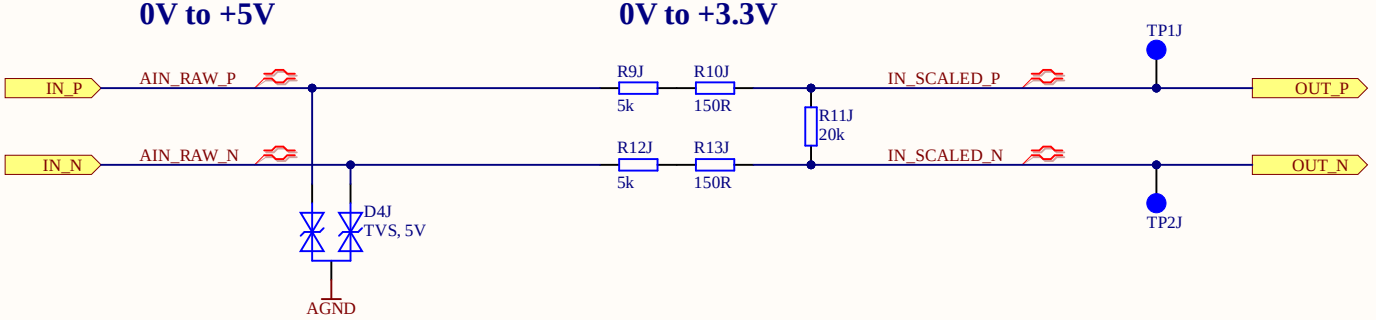
Passive Voltage Devider
0V to +3.3V



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	Date: 02.12.2022
Project: UZ_A_MAX11331.PrjPCB		Sheet 4.9 of 36

Analog Input Range
0V to +5V

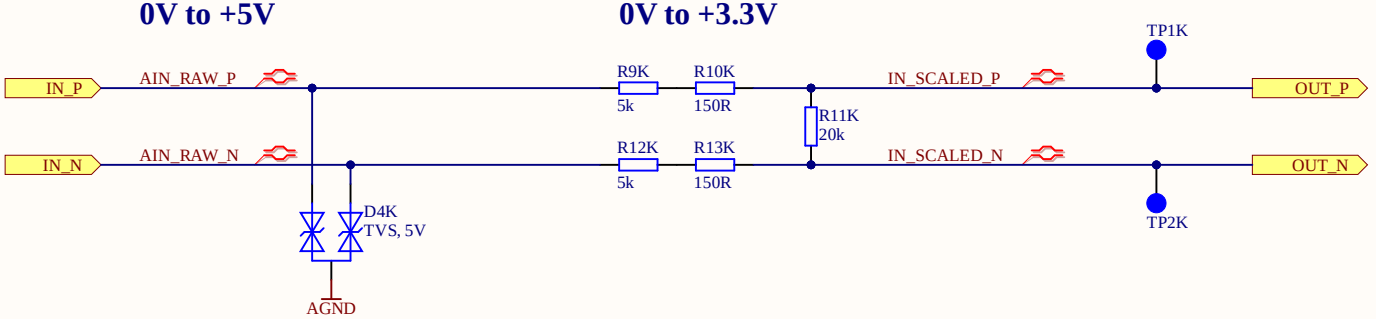
Passive Voltage Devider
0V to +3.3V



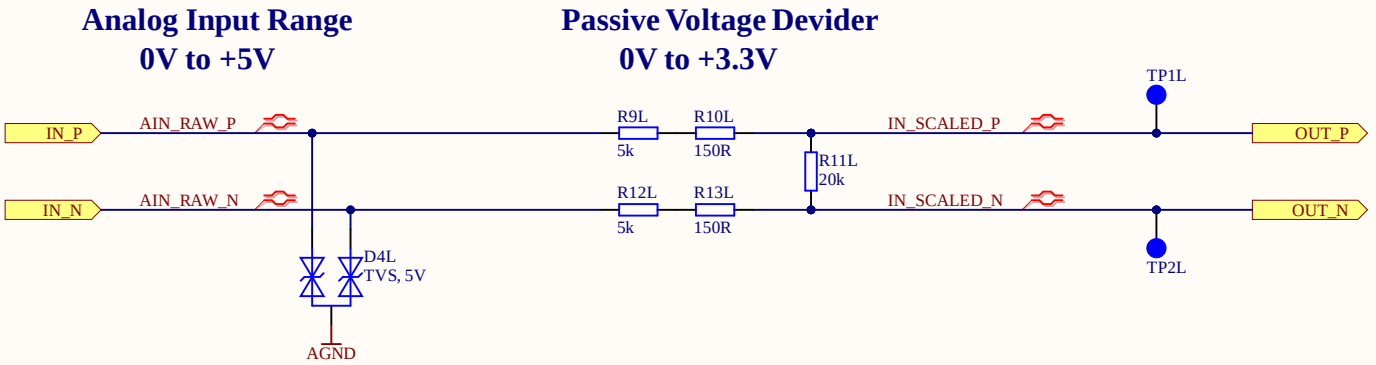
Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm	
Revision: Rev01	Design Engineer: Andreas Geiger	www.ultrazohm.com	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	
		Sheet 4.10of 36	

Analog Input Range
0V to +5V

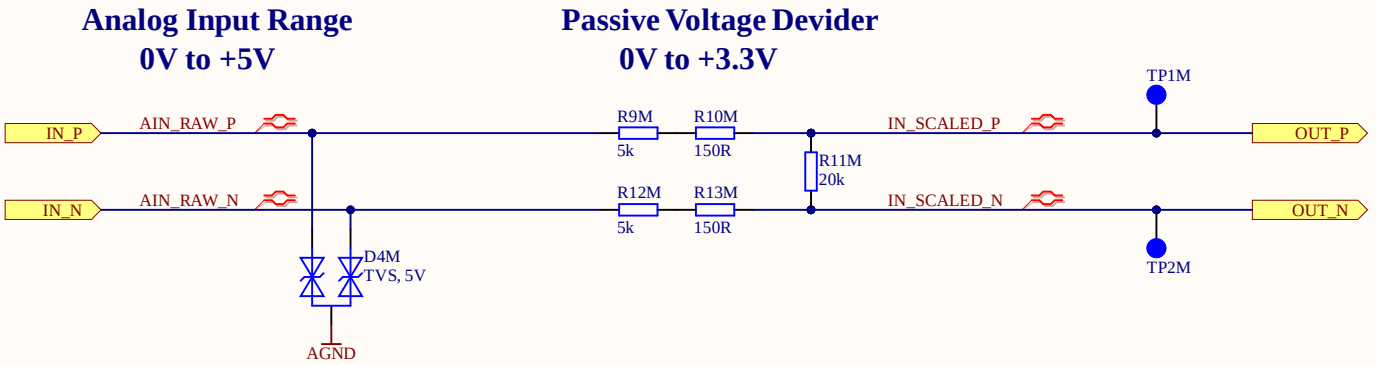
Passive Voltage Devider
0V to +3.3V



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 4.11of 36



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com	
Revision: Rev01	Design Engineer: Andreas Geiger		
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	
		Sheet 4.12 of 36	



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm	
Revision: Rev01	Design Engineer: Andreas Geiger	www.ultrazohm.com	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	
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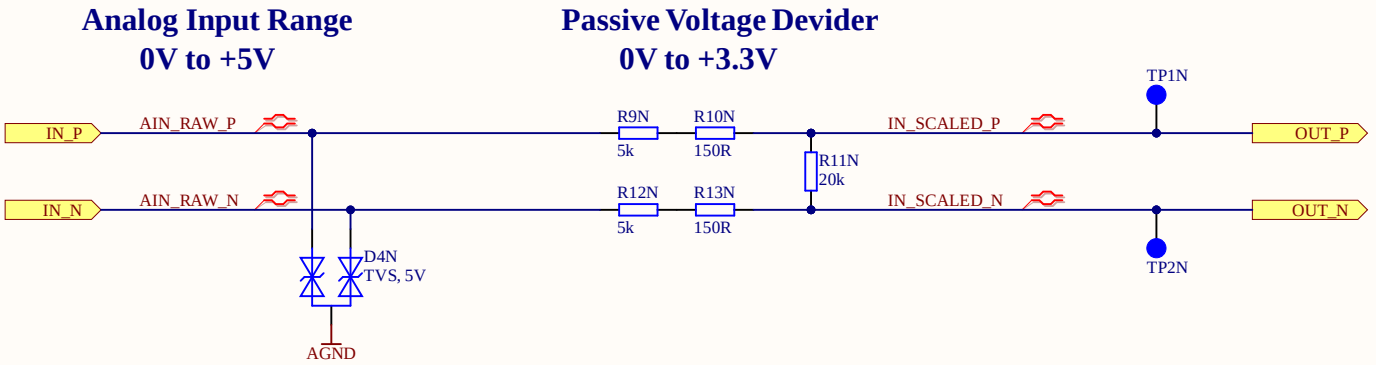
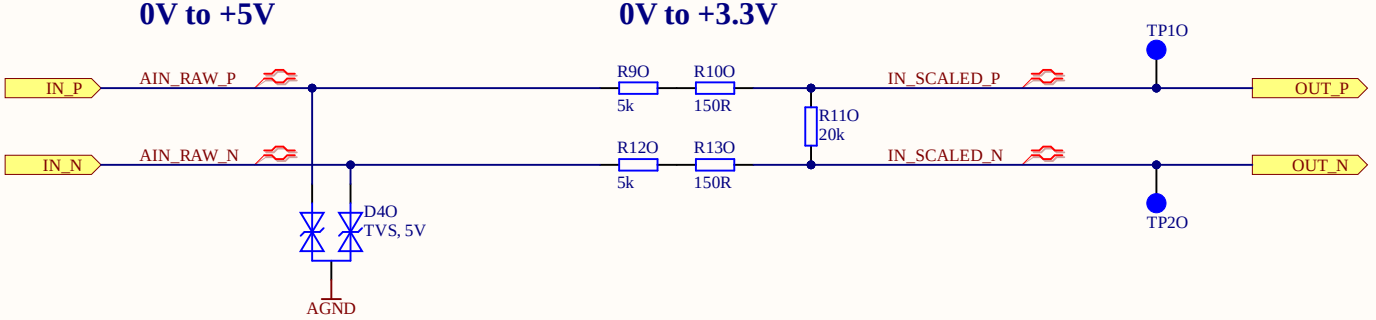


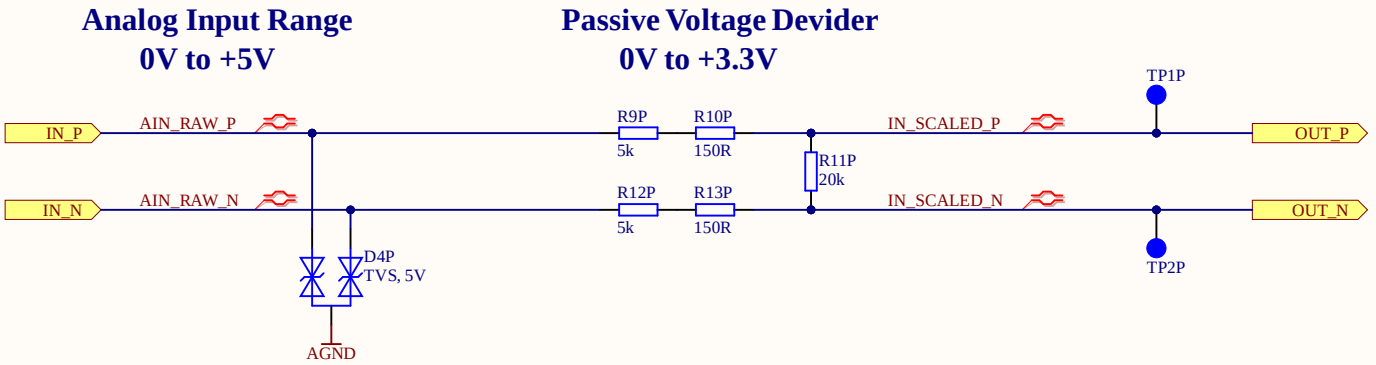
Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com	
Revision: Rev01	Design Engineer: Andreas Geiger		
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	Sheet 4.14of 36

Analog Input Range
0V to +5V

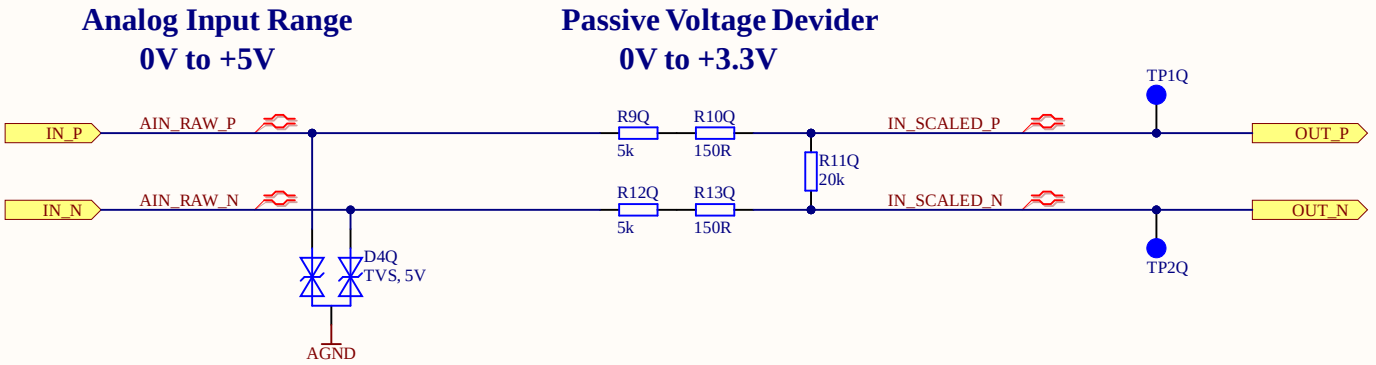
Passive Voltage Devider
0V to +3.3V



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 4.15of 36



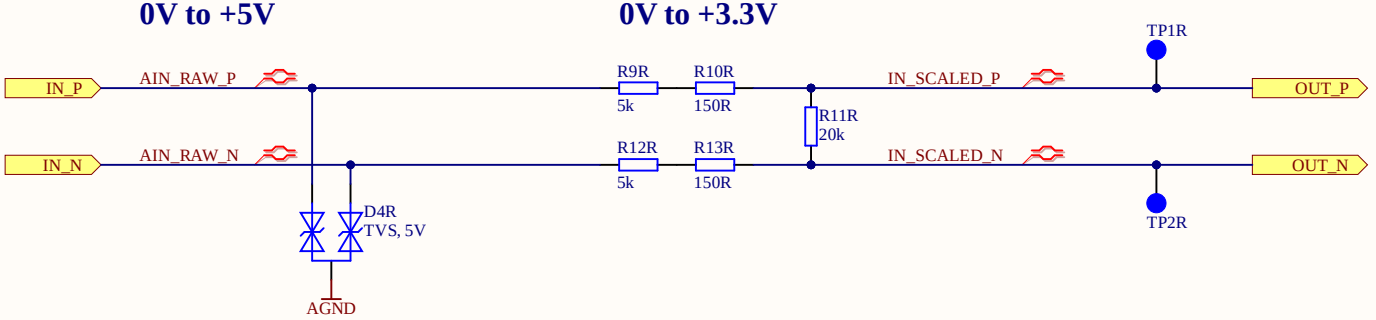
Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com	
Revision: Rev01	Design Engineer: Andreas Geiger		
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	
		Sheet 4.16 of 36	



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com	
Revision: Rev01	Design Engineer: Andreas Geiger		
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 4.17of 36	

Analog Input Range
0V to +5V

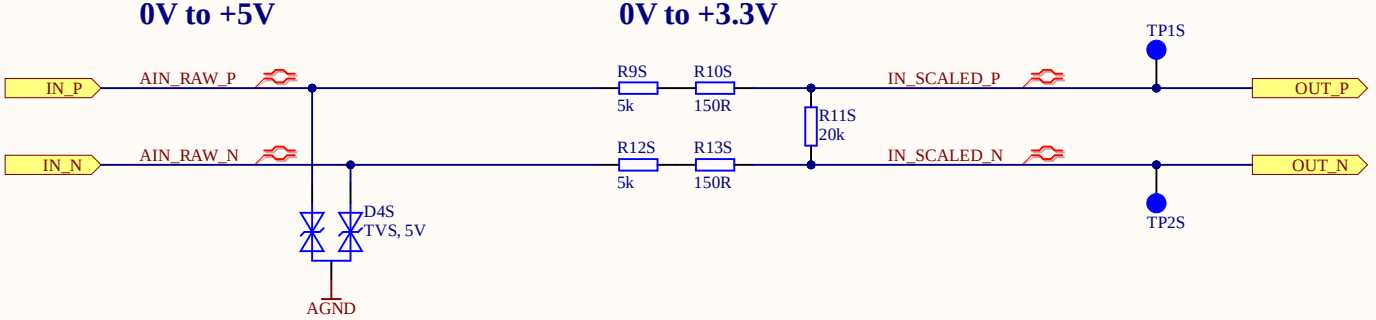
Passive Voltage Devider
0V to +3.3V



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 4.18of 36

Analog Input Range
0V to +5V

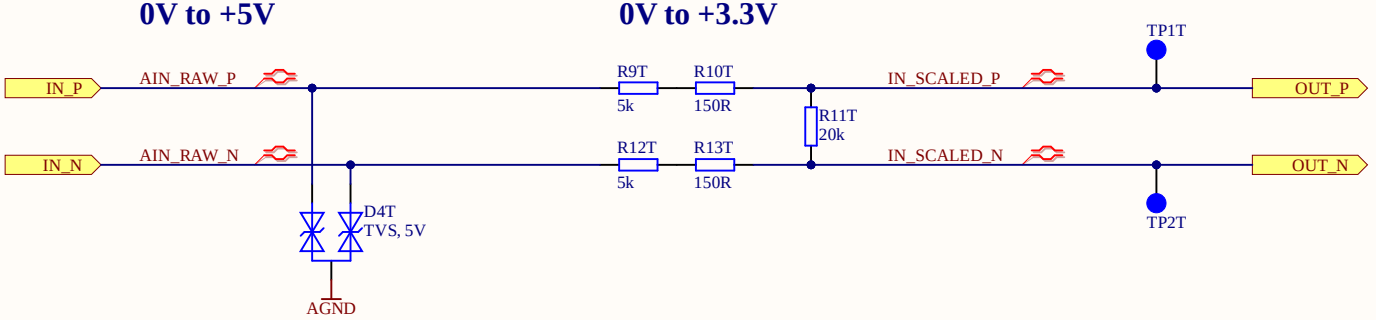
Passive Voltage Devider
0V to +3.3V



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022
		Sheet 4.19of 36

Analog Input Range
0V to +5V

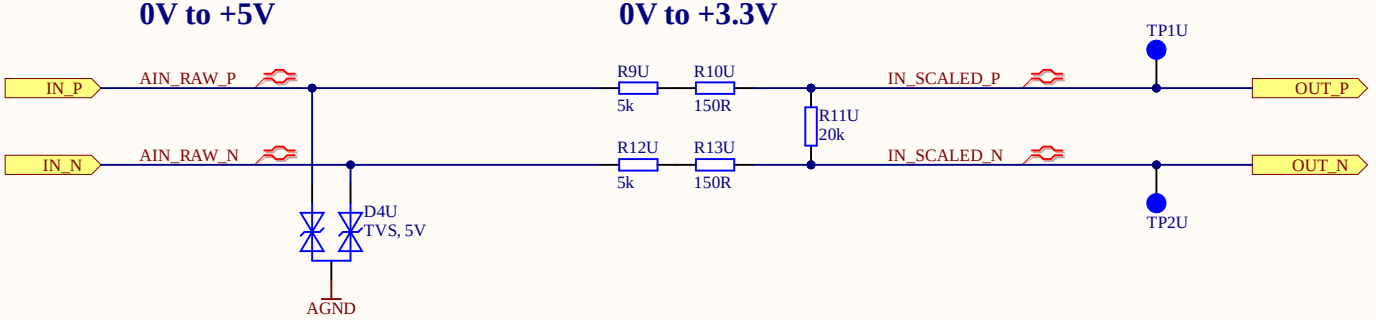
Passive Voltage Devider
0V to +3.3V



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com	
Revision: Rev01	Design Engineer: Andreas Geiger		
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 4.20of 36	

Analog Input Range
0V to +5V

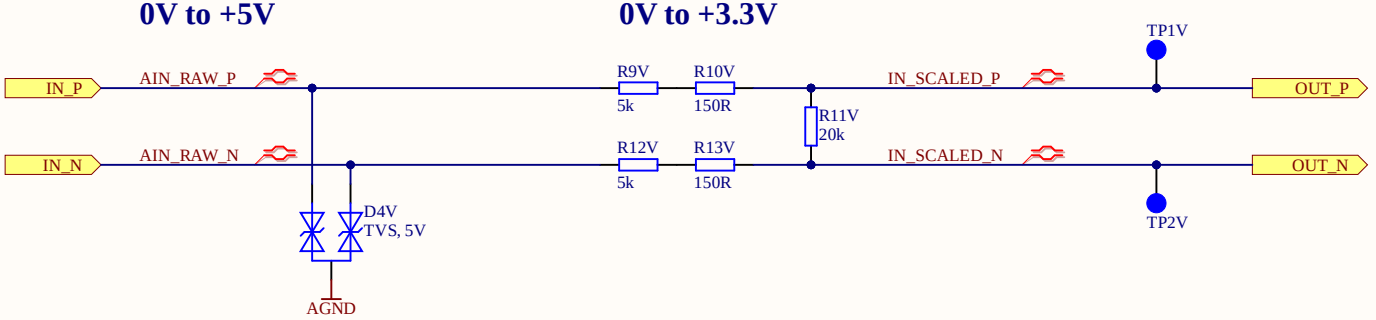
Passive Voltage Devider
0V to +3.3V



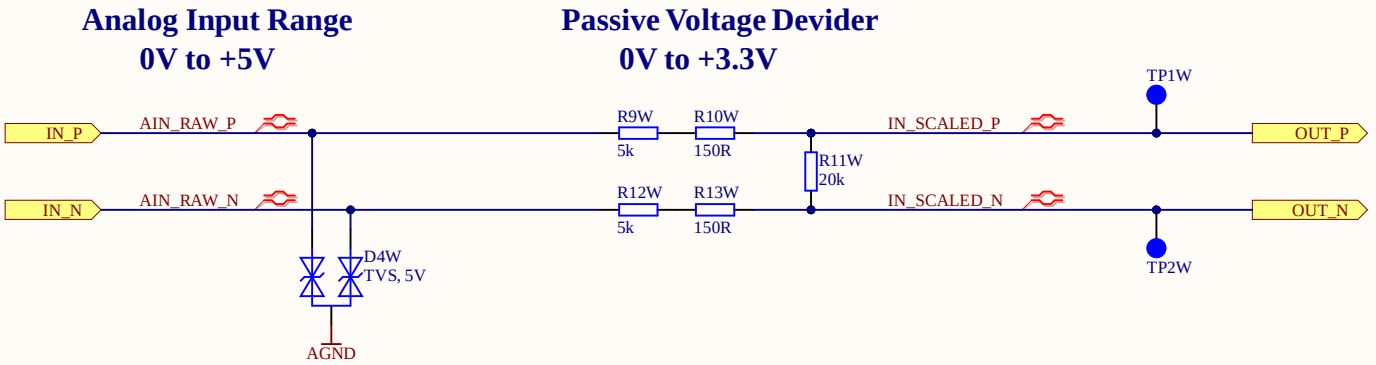
Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 4.21of 36

Analog Input Range
0V to +5V

Passive Voltage Devider
0V to +3.3V



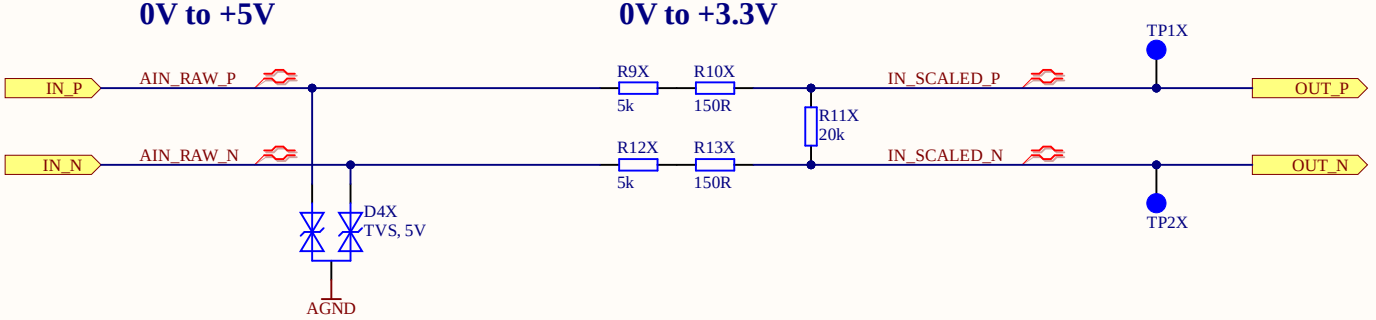
Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022
		Sheet 4.22 of 36



Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm	
Revision: Rev01	Design Engineer: Andreas Geiger	www.ultrazohm.com	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	
		Sheet 4.23 of 36	

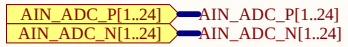
Analog Input Range
0V to +5V

Passive Voltage Devider
0V to +3.3V

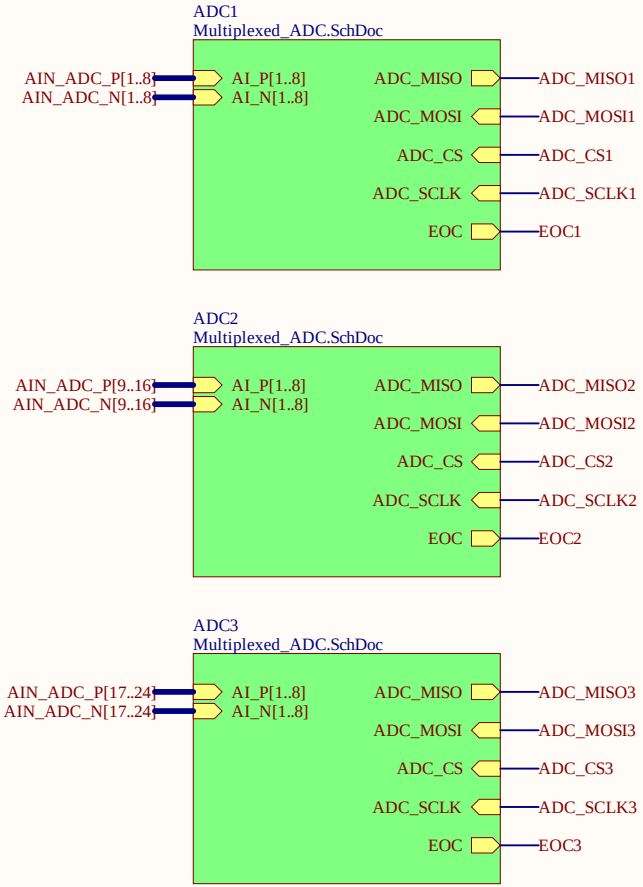


Title Analog_Input_Signal_Conditioning.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 4.24of 36

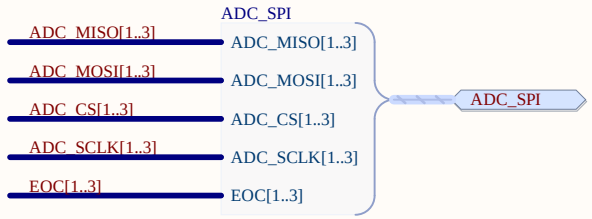
Analog Inputs



Multiplexed ADCs

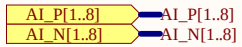


Interface to FPGA

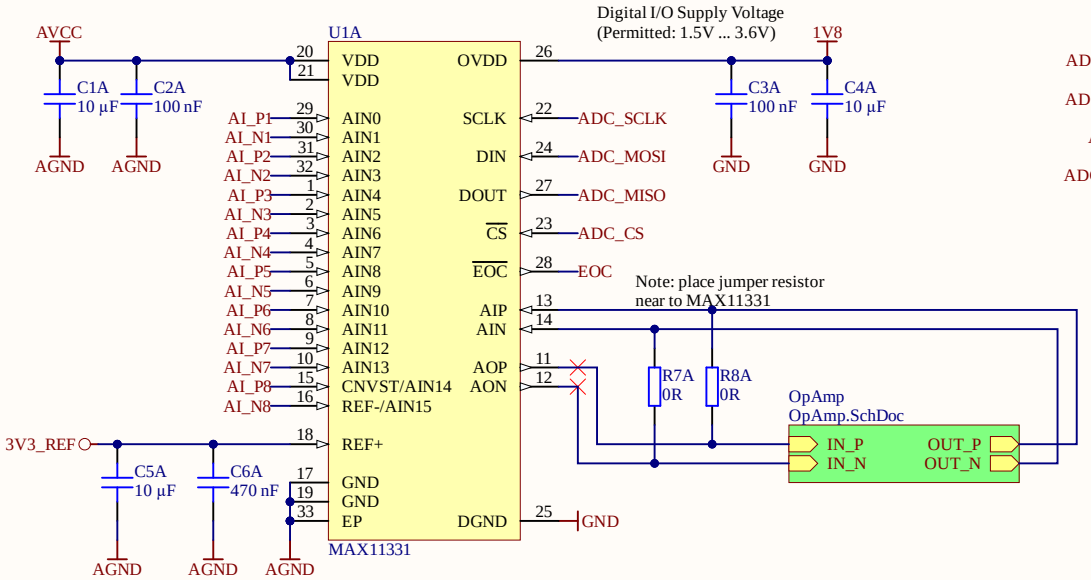


Title ADC_Signal_Distribution.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	Date: 02.12.2022
Project: UZ_A_MAX11331.PrjPCB		Sheet 5 of 36

Analog Inputs

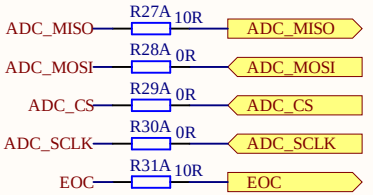


Multiplexed 16-Channel ADC



Note: Maximum sampling rate: with 16 channel: 187.5 kSps per channel
- 8 channel, Differential: 375 kSps per channel
- 16 channel, Single-Ended: 187.5 kSps per channel

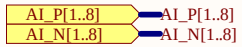
Interface to FPGA



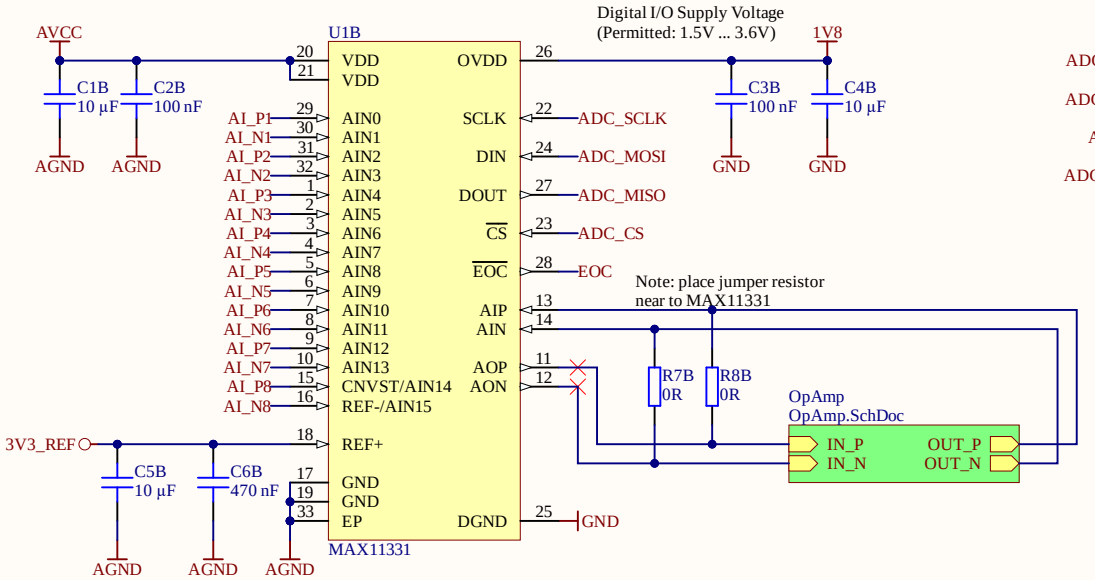
Single-Ended line termination:
MISO resistor near MAX11331
MOSI/SCLK/CS/EOC resistor near FPGA

Title Multiplexed_ADC.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 6.1 of 36

Analog Inputs

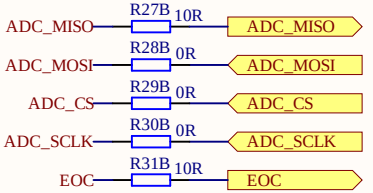


Multiplexed 16-Channel ADC



Note: Maximum sampling rate: with 16 channel: 187.5 kSps per channel
- 8 channel, Differential: 375 kSps per channel
- 16 channel, Single-Ended: 187.5 kSps per channel

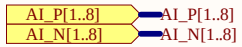
Interface to FPGA



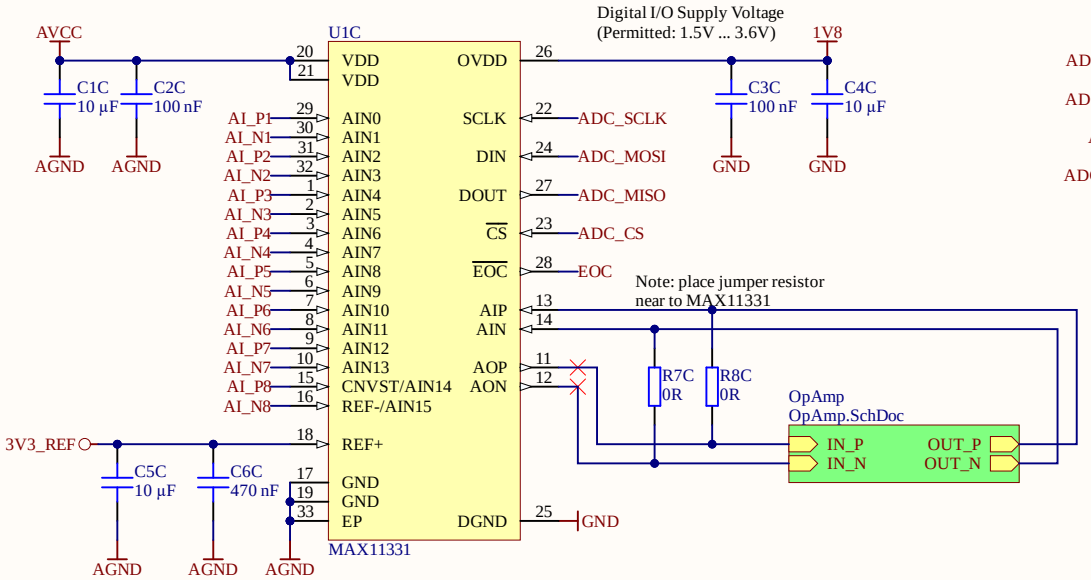
Single-Ended line termination:
MISO resistor near MAX11331
MOSI/SCLK/CS/EOC resistor near FPGA

Title Multiplexed_ADC.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022 Sheet 6.2 of 36

Analog Inputs

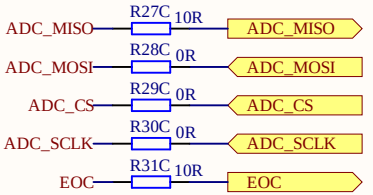


Multiplexed 16-Channel ADC



Note: Maximum sampling rate: with 16 channel: 187.5 kSps per channel
- 8 channel, Differential: 375 kSps per channel
- 16 channel, Single-Ended: 187.5 kSps per channel

Interface to FPGA



Single-Ended line termination:
MISO resistor near MAX11331
MOSI/SCLK/CS/EOC resistor near FPGA

Title Multiplexed_ADC.SchDoc		UltraZohm www.ultrazohm.com
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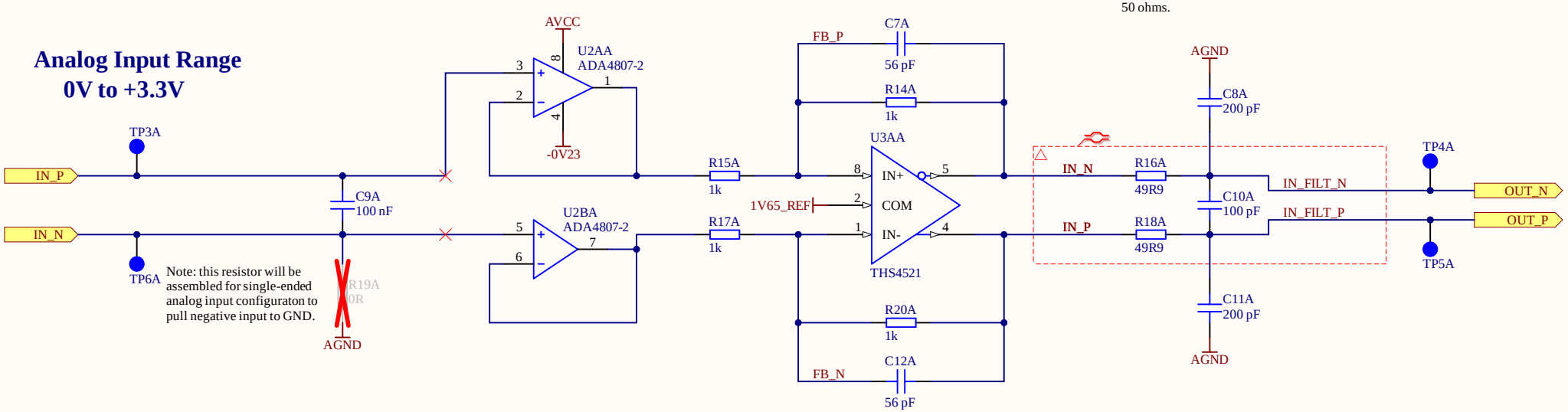
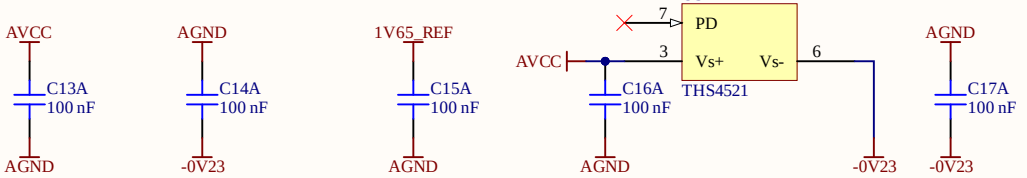
Analog Input Range
0V to +3.3V



Filter design:
At a cutoff frequency of 16.25MHz (1/4 of 65MSample/sec), an R of 98 ohms and a C of 100 pF should be used. Since this is a differential filter, the resistance is calculated as half, i.e. 50 ohms.



Note: place buffer Cap near Pin 8 of Opamp

Note: place buffer Cap near Pin 4 of Opamp

Note: place buffer Cap near Pin 2 of Diff-Opamp

Note: place buffer Cap near Pin 3 of Diff-Opamp

Note: place buffer Cap near Pin 6 of Diff-Opamp

Title OpAmp.SchDoc		UltraZohm www.ultrazohm.com
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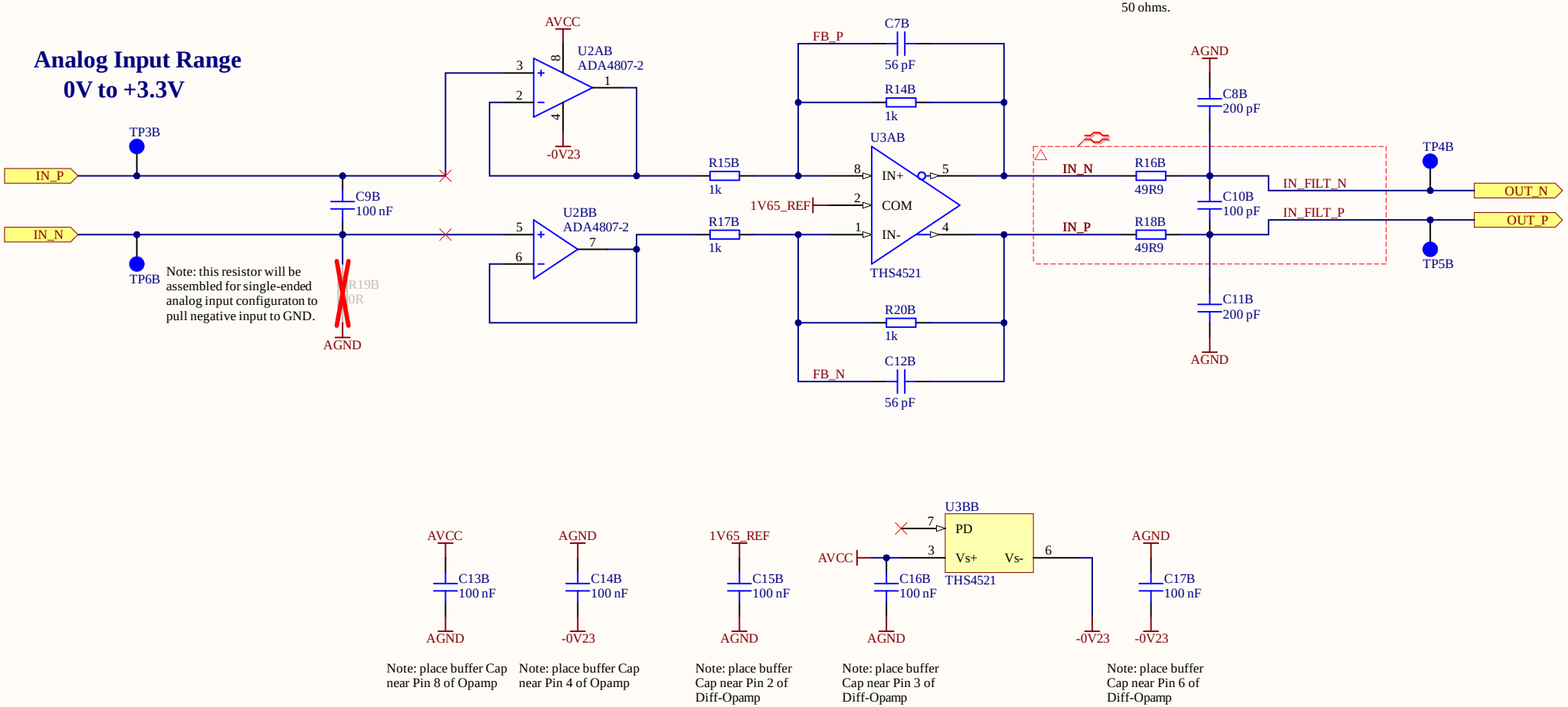
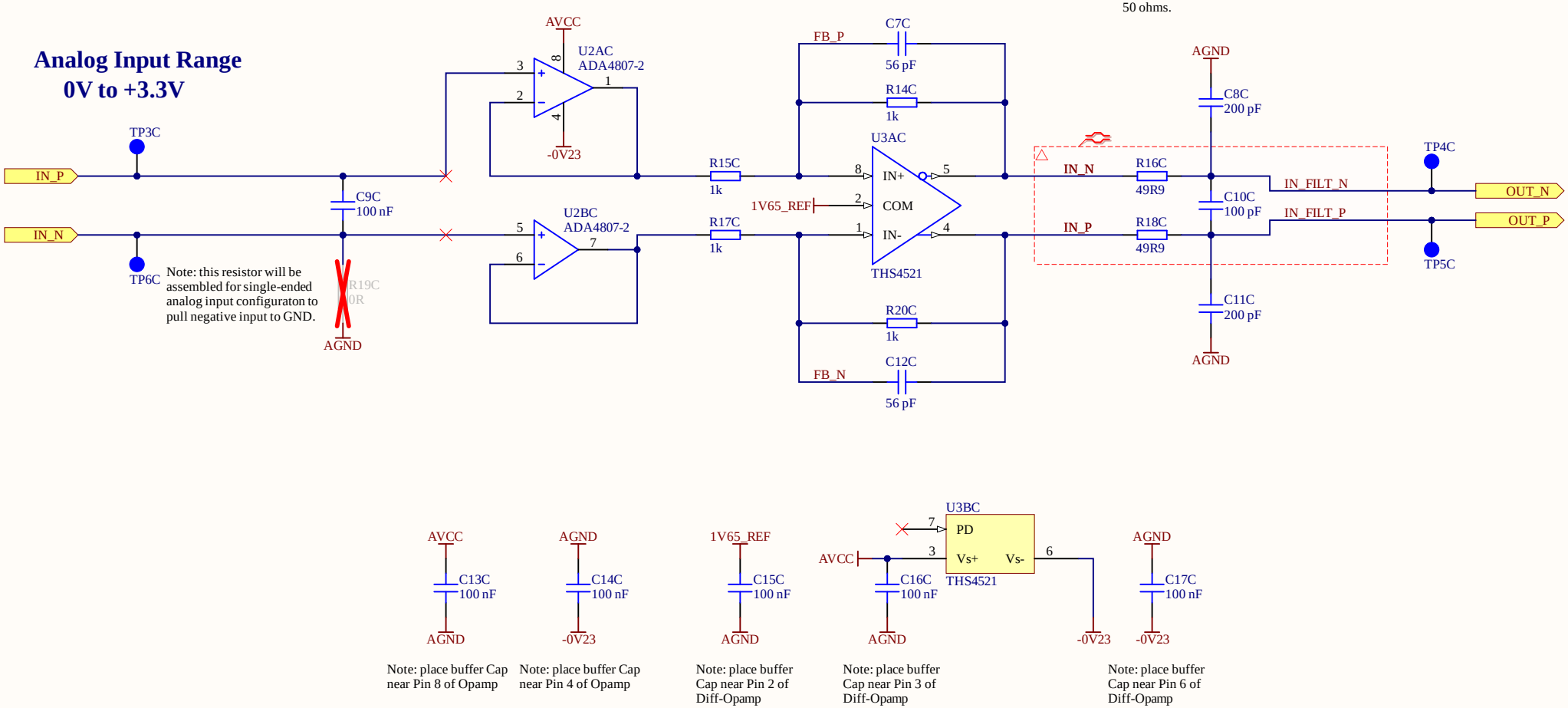
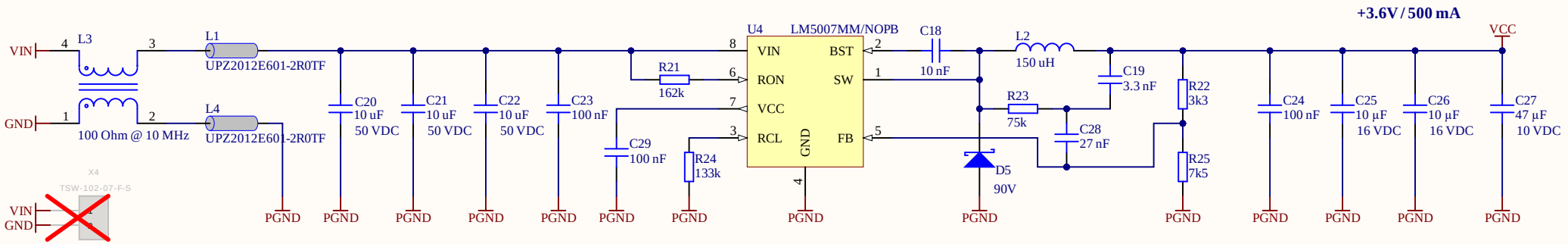


Title OpAmp.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	Date: 02.12.2022
Project: UZ_A_MAX11331.PrjPCB		Sheet 7.2.1 of 36

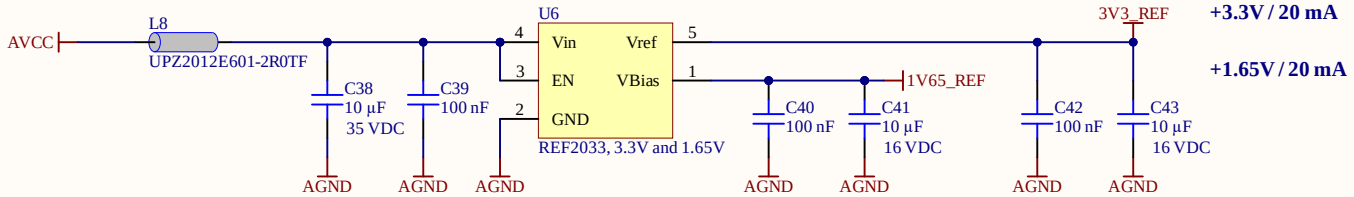


Title OpAmp.SchDoc		UltraZohm www.ultrazohm.com
Revision: Rev01	Design Engineer: Andreas Geiger	Date: 02.12.2022
Project: UZ_A_MAX11331.PrjPCB		Sheet 7.3.1 of 36

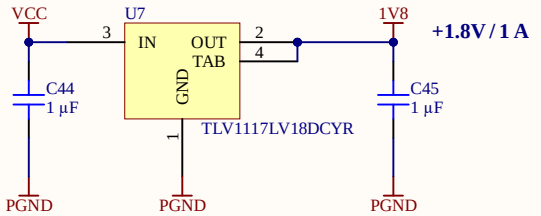
3.6 V Power Supply



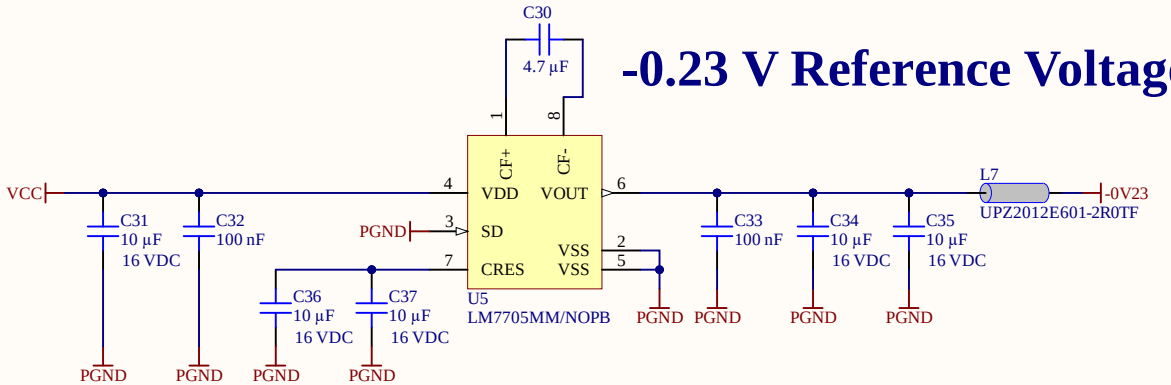
3.3 V and 1.65 V Reference Voltage

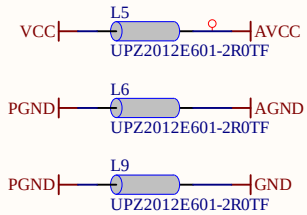


1.8 V Power Supply



-0.23 V Reference Voltage





Title Power_Supply.SchDoc		UltraZohm	
Revision: Rev01	Design Engineer: Andreas Geiger	www.ultrazohm.com	
Project: UZ_A_MAX11331.PrjPCB		Date: 02.12.2022	
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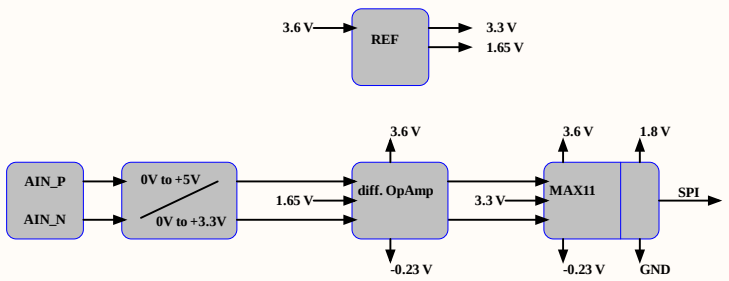
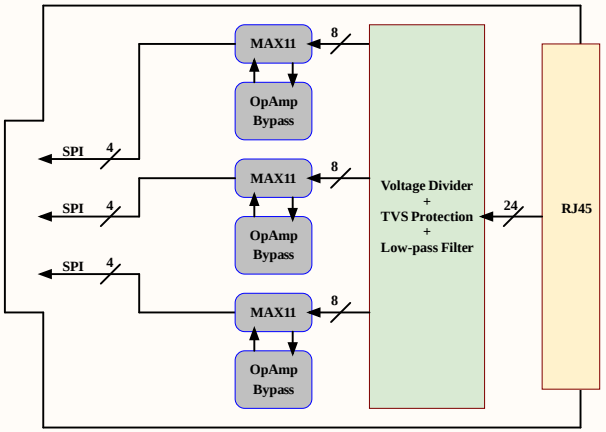
Functional Block Diagram

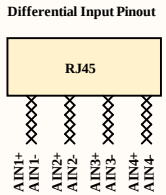


Manufacturing Dokumentation

- JLC PCB Layer Stackup: JLC7628 for 1.6mm
- Assembly only on TOP side



Analog Input Interface via RJ45 Connector



Title Block_Diagram.SchDoc		UltraZohm www.ultrazohm.com
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