

A

A

B

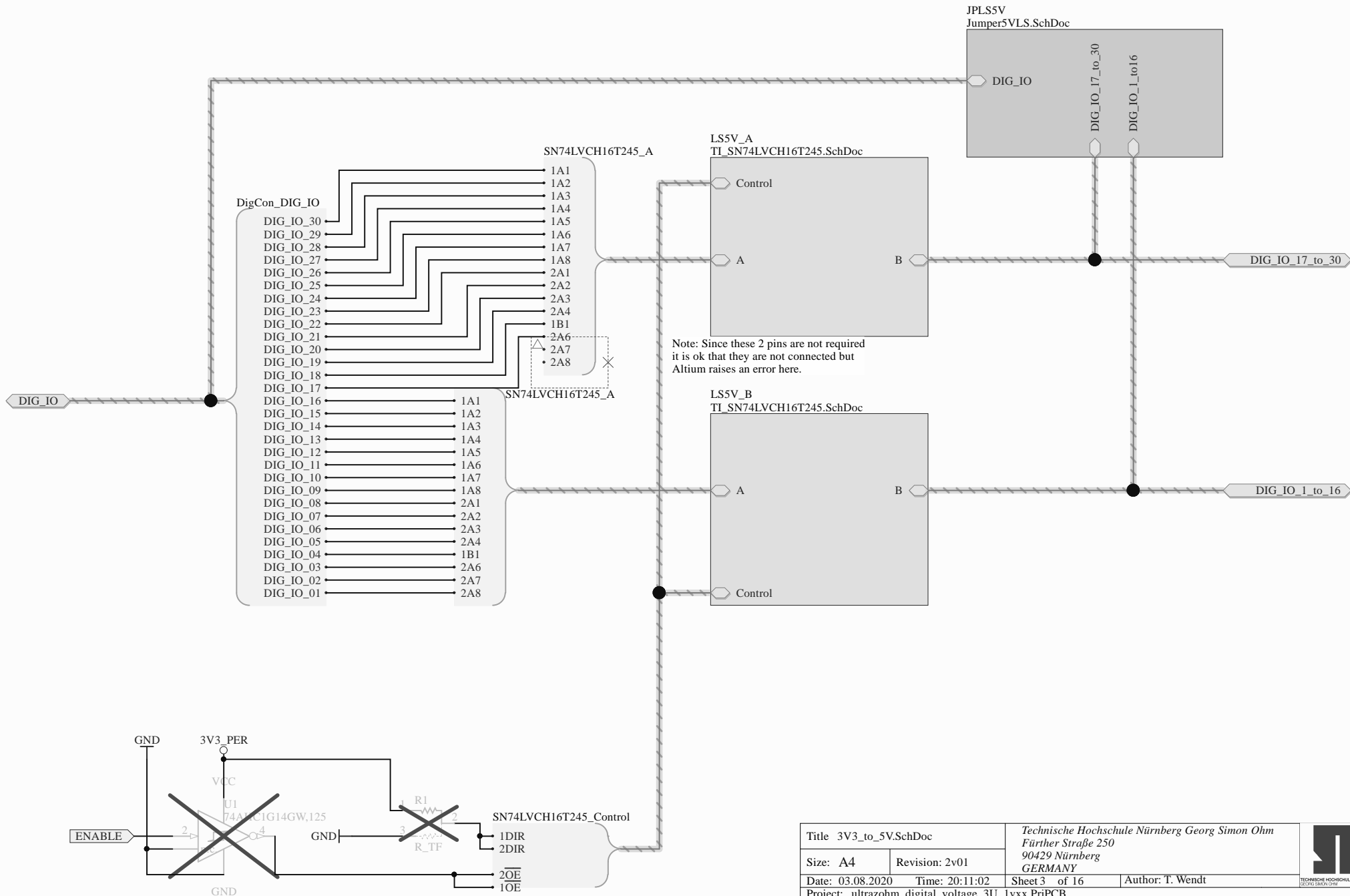
B

C

C

D

D



SN74LVCH16T245_B

2B8 DIG_IO_5V_A1
2B7 DIG_IO_5V_B1
2B6 DIG_IO_5V_C1
2B5 DIG_IO_5V_D1
2B4 DIG_IO_5V_E1
2B3 DIG_IO_5V_F1
2B2 DIG_IO_5V_A2
2B1 DIG_IO_5V_B2
1B8 DIG_IO_5V_C2
1B7 DIG_IO_5V_D2
1B6 DIG_IO_5V_E2
1B5 DIG_IO_5V_F2
1B4 DIG_IO_5V_A3
1B3 DIG_IO_5V_B3
1B2 DIG_IO_5V_C3
1B1 DIG_IO_5V_D3

DIG_IO_1_to_16

~~DIG_IO_5V_A[1..5]~~
~~DIG_IO_5V_B[1..5]~~
~~DIG_IO_5V_C[1..5]~~
~~DIG_IO_5V_D[1..5]~~
~~DIG_IO_5V_E[1..5]~~
~~DIG_IO_5V_F[1..5]~~

DIG_IO_SINGLE

~~DIG_IO_SINGLE_A[1..5]~~
~~DIG_IO_SINGLE_B[1..5]~~
~~DIG_IO_SINGLE_C[1..5]~~
~~DIG_IO_SINGLE_D[1..5]~~
~~DIG_IO_SINGLE_E[1..5]~~
~~DIG_IO_SINGLE_F[1..5]~~

DIG_O_15V_A[1..5]
DIG_O_15V_B[1..5]
DIG_O_15V_C[1..5]
DIG_O_15V_D[1..5]
DIG_O_15V_E[1..5]
DIG_O_15V_F[1..5]

DIG_IO_SINGLE

Note: Since these 2 pins are not required
it is ok that they are not connected but
Altium raises an error here.

SN74LVCH16T245_B

2B8
2B7 DIG_IO_5V_E3
2B6 DIG_IO_5V_F3
2B5 DIG_IO_5V_A4
2B4 DIG_IO_5V_B4
2B3 DIG_IO_5V_C4
2B2 DIG_IO_5V_D4
2B1 DIG_IO_5V_E4
1B8 DIG_IO_5V_F4
1B7 DIG_IO_5V_A5
1B6 DIG_IO_5V_B5
1B5 DIG_IO_5V_C5
1B4 DIG_IO_5V_D5
1B3 DIG_IO_5V_E5
1B2 DIG_IO_5V_F5
1B1

DIG_IO_17_to_30

REPEAT(LS15V,1,5)
ONSEMI_MC14504BDR2G

DIG_IO_5V_A
DIG_IO_5V_B
DIG_IO_5V_C
DIG_IO_5V_E
DIG_IO_5V_F
DIG_IO_5V_D

REPEAT(AIN)
REPEAT(BIN)
REPEAT(CIN)
REPEAT(DIN)
REPEAT(EIN)
REPEAT(FIN)
REPEAT(AOUT)
REPEAT(BOUT)
REPEAT(COUT)
REPEAT(DOUT)
REPEAT(EOUT)
REPEAT(FOUT)

DIG_IO_SINGLE A
DIG_IO_SINGLE B
DIG_IO_SINGLE C
DIG_IO_SINGLE E
DIG_IO_SINGLE F
DIG_IO_SINGLE D

S50
S50
S50
S50
S50
S50

5V_PERO
GND
R2
R_TF

MODE

A

B

C

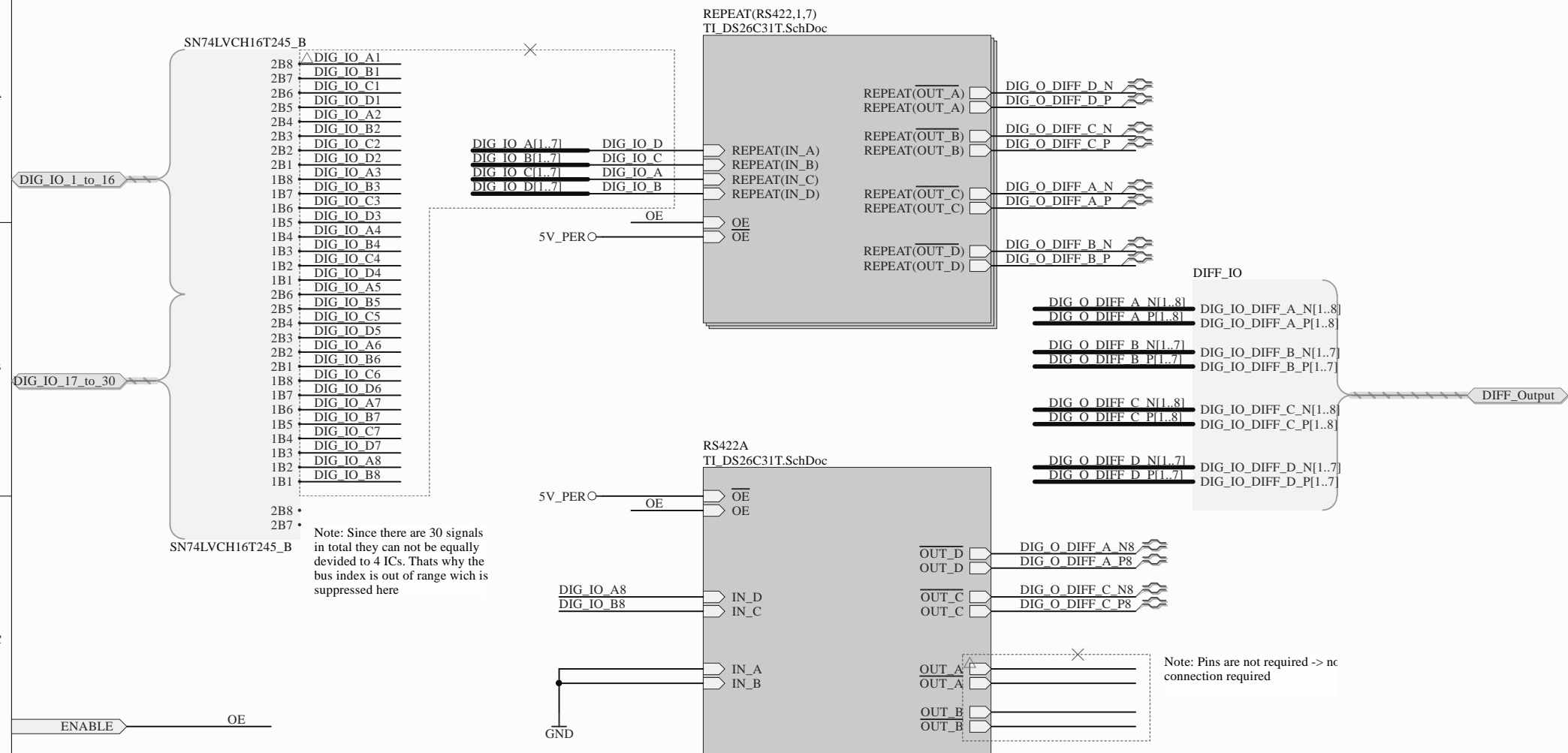
D

A

B

C

D



A

A

B

B

C

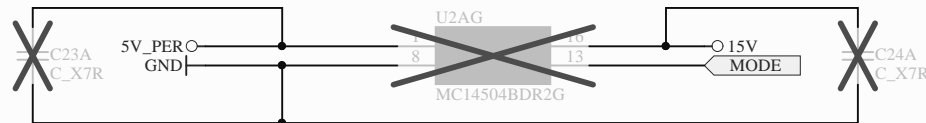
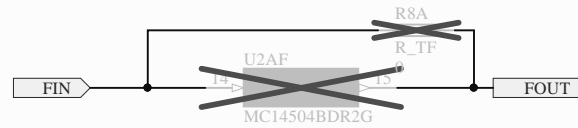
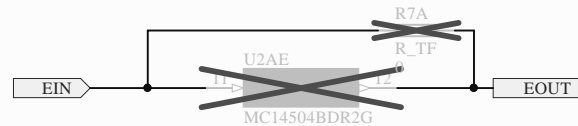
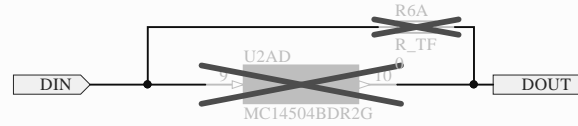
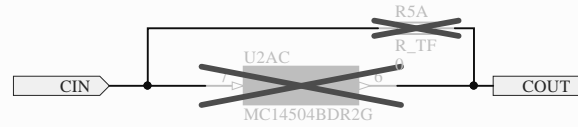
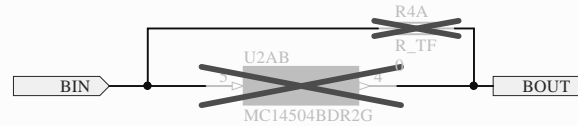
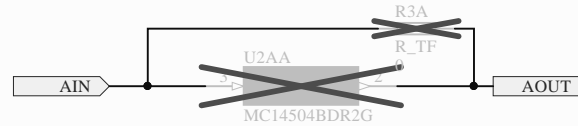
C

D

D

Voltages:
VCC = voltage level of the input signal
VDD = output voltage level

Application:
MODE = VCC -> TTL logic level input
MODE = VSS -> CMOS logic level input



A

A

B

B

C

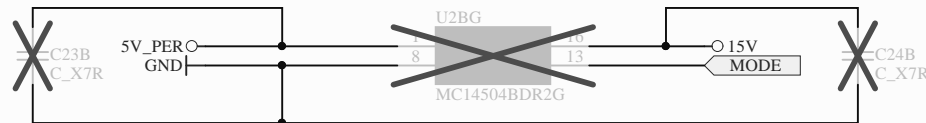
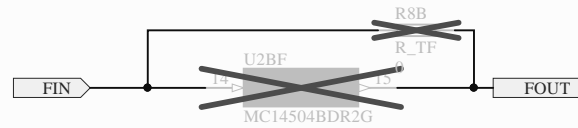
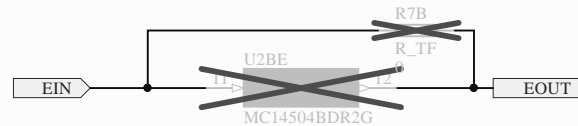
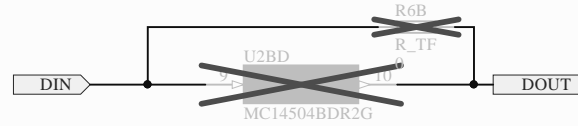
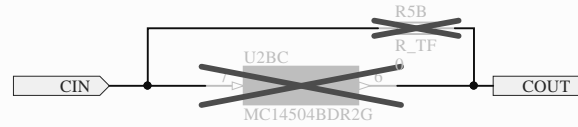
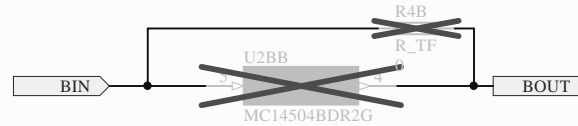
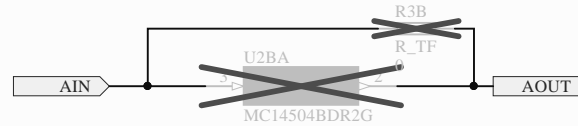
C

D

D

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Application:
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MODE = VSS -> CMOS logic level input



A

A

B

B

C

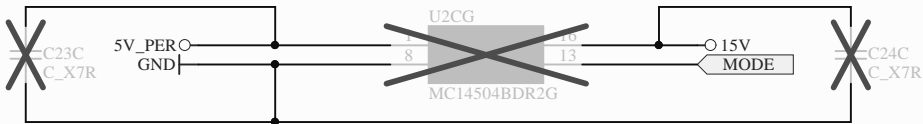
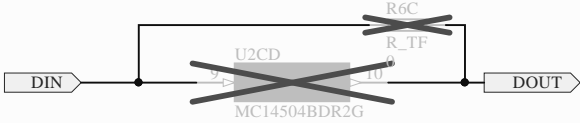
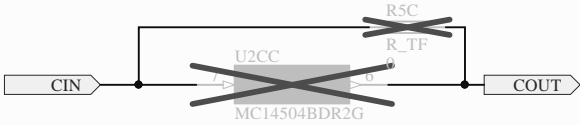
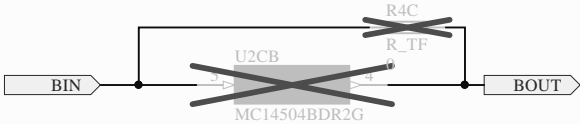
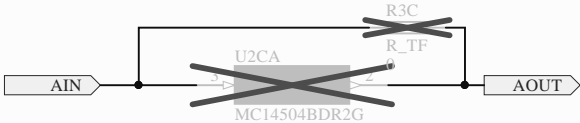
C

D

D

Voltages:
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VDD = output voltage level

Application:
MODE = VCC -> TTL logic level input
MODE = VSS -> CMOS logic level input



A

A

B

B

C

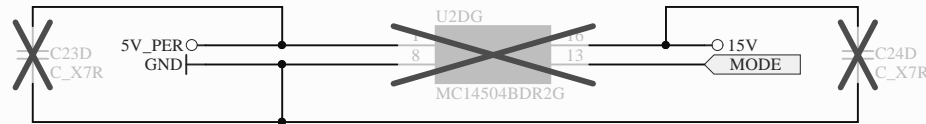
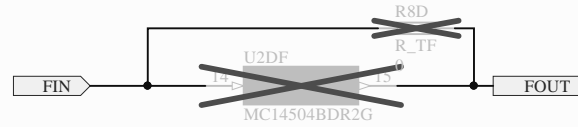
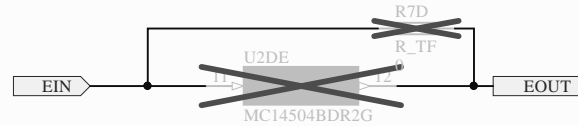
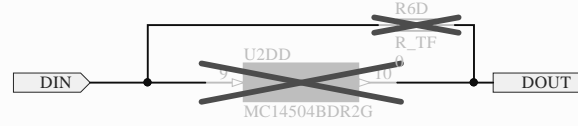
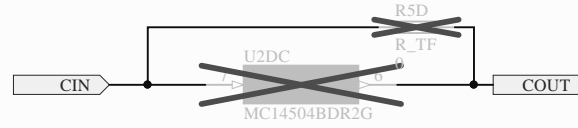
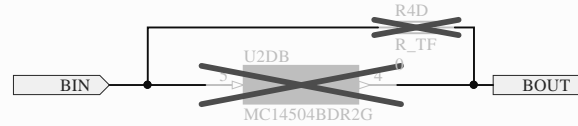
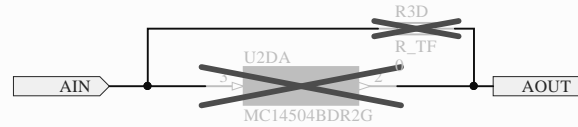
C

D

D

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VDD = output voltage level

Application:
MODE = VCC -> TTL logic level input
MODE = VSS -> CMOS logic level input



A

A

B

B

C

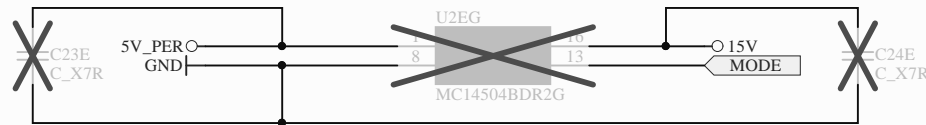
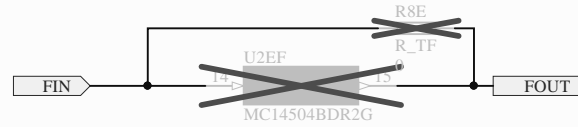
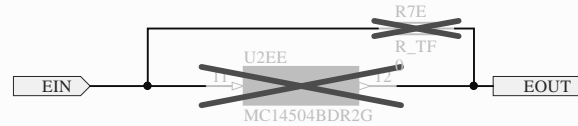
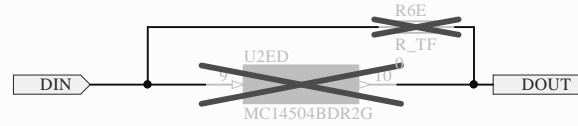
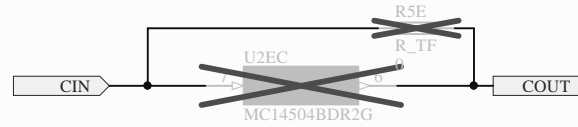
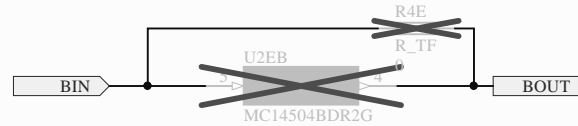
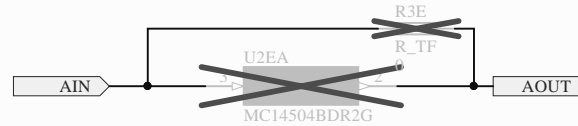
C

D

D

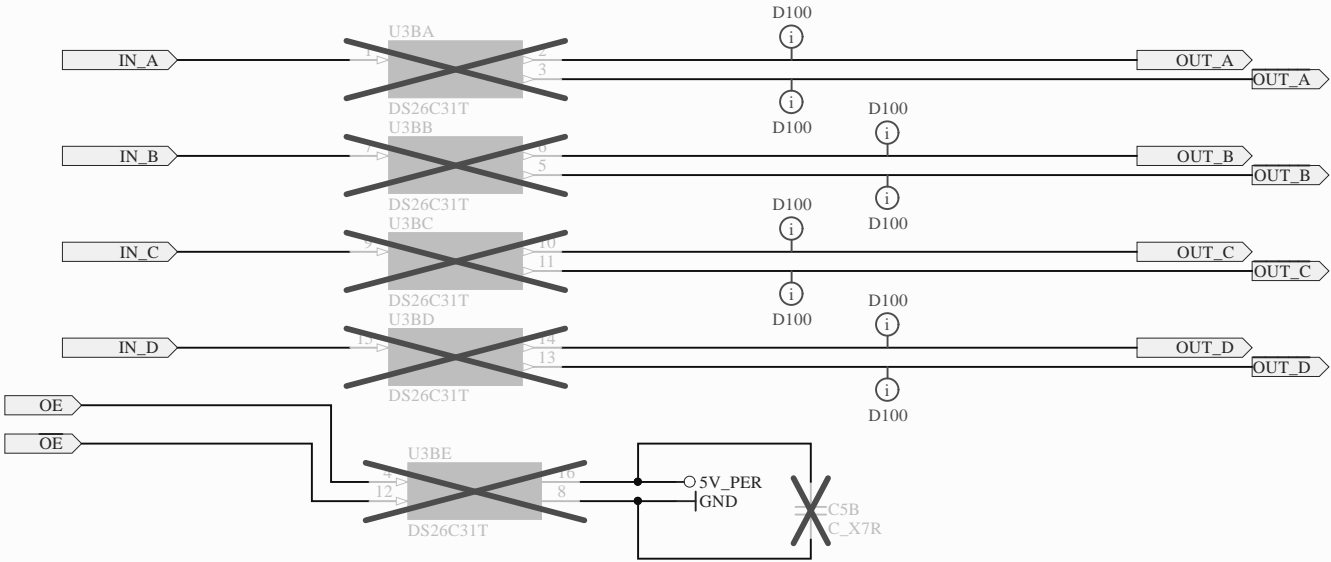
Voltages:
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VDD = output voltage level

Application:
MODE = VCC -> TTL logic level input
MODE = VSS -> CMOS logic level input



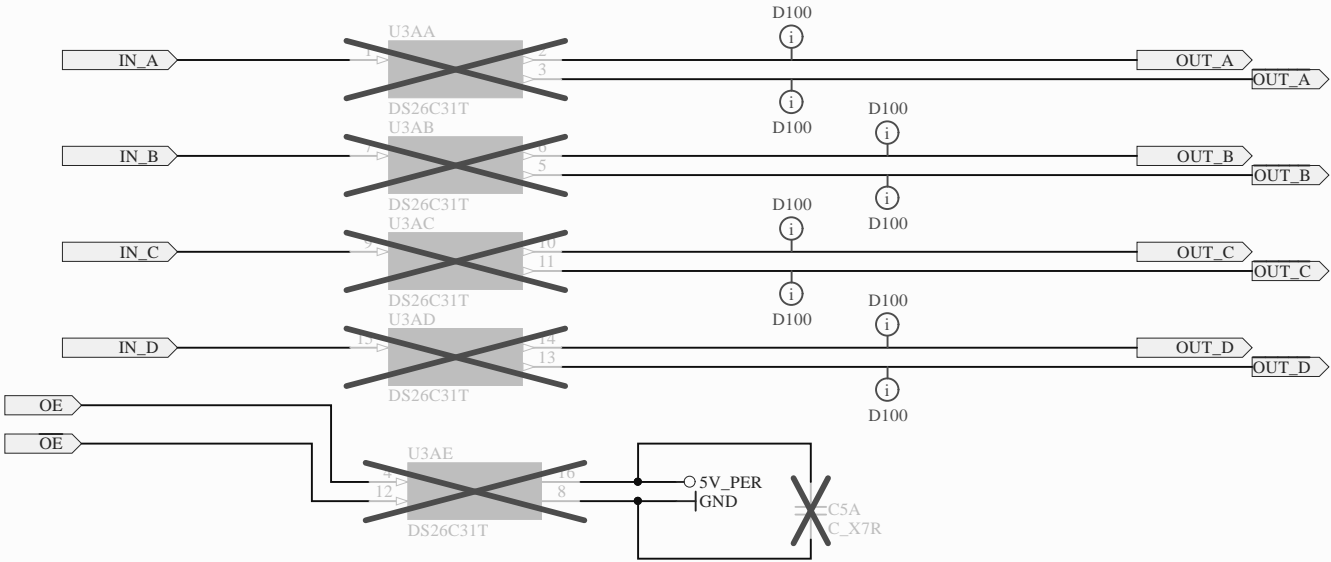
Application:
VDD_min = 4.5V
VDD_max 5.5V

VIN_high_min = 2.0V
VIN_low_max = 0.8V



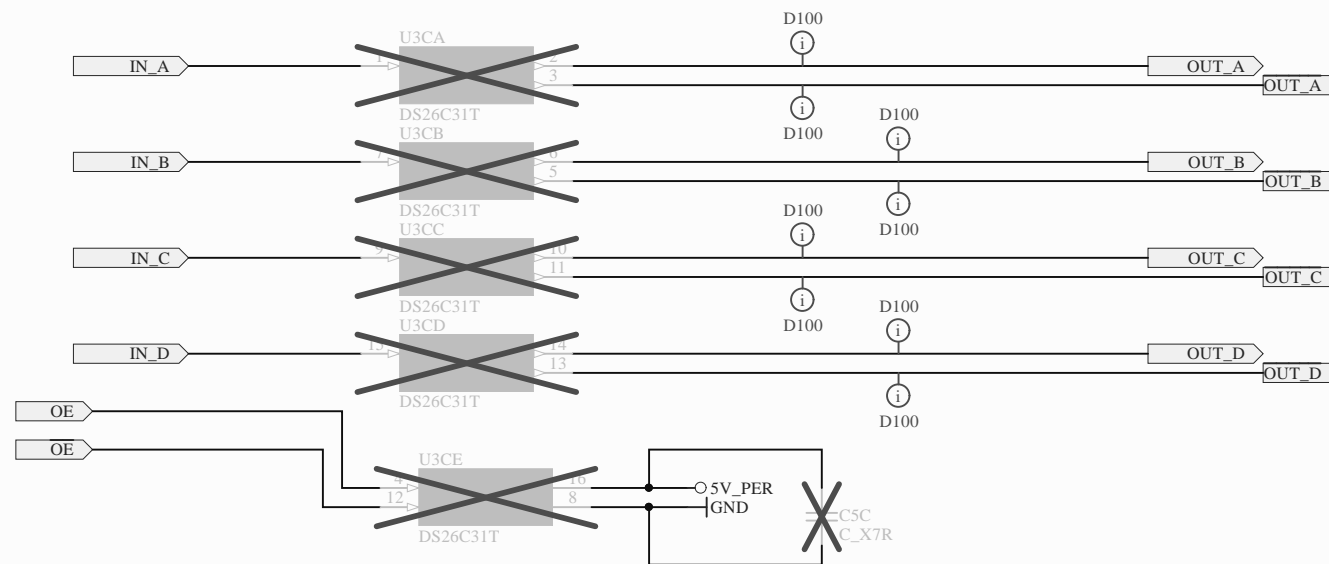
Application:
VDD_min = 4.5V
VDD_max 5.5V

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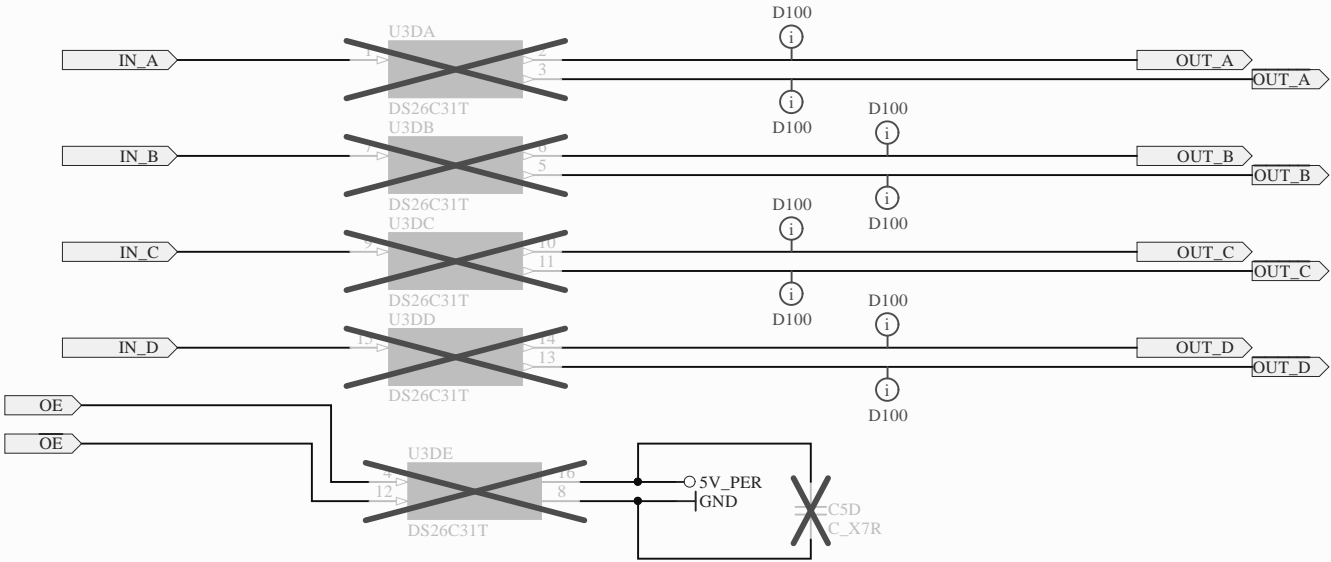
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VDD_max 5.5V

VIN_high_min = 2.0V
VIN_low_max = 0.8V



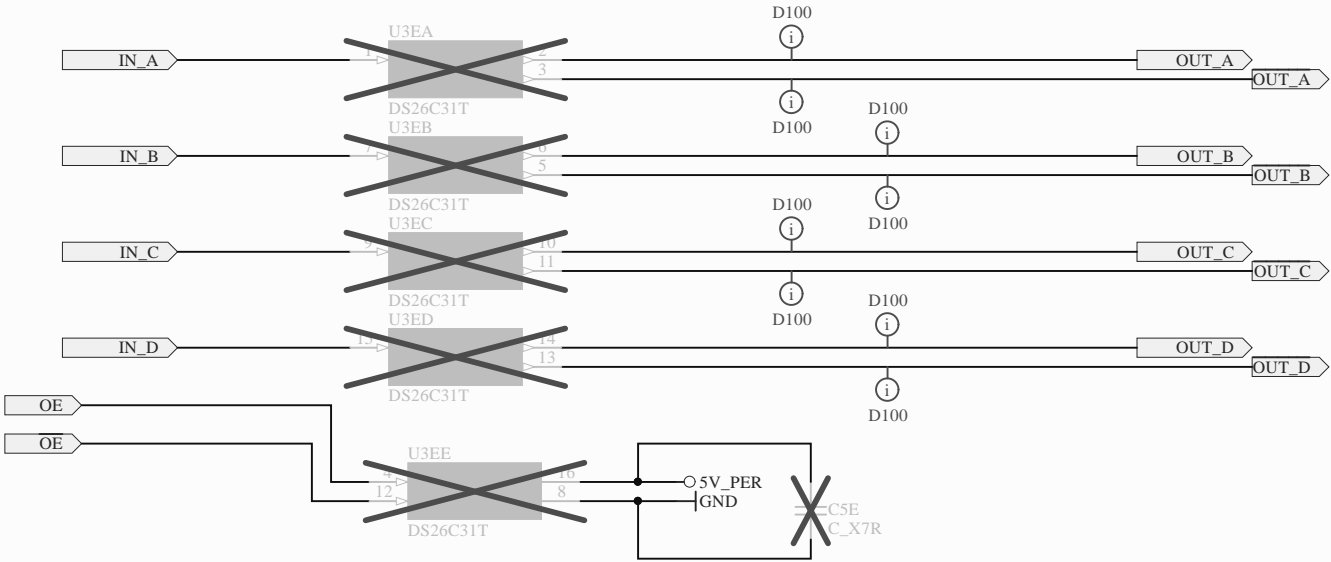
Application:
VDD_min = 4.5V
VDD_max 5.5V

VIN_high_min = 2.0V
VIN_low_max = 0.8V



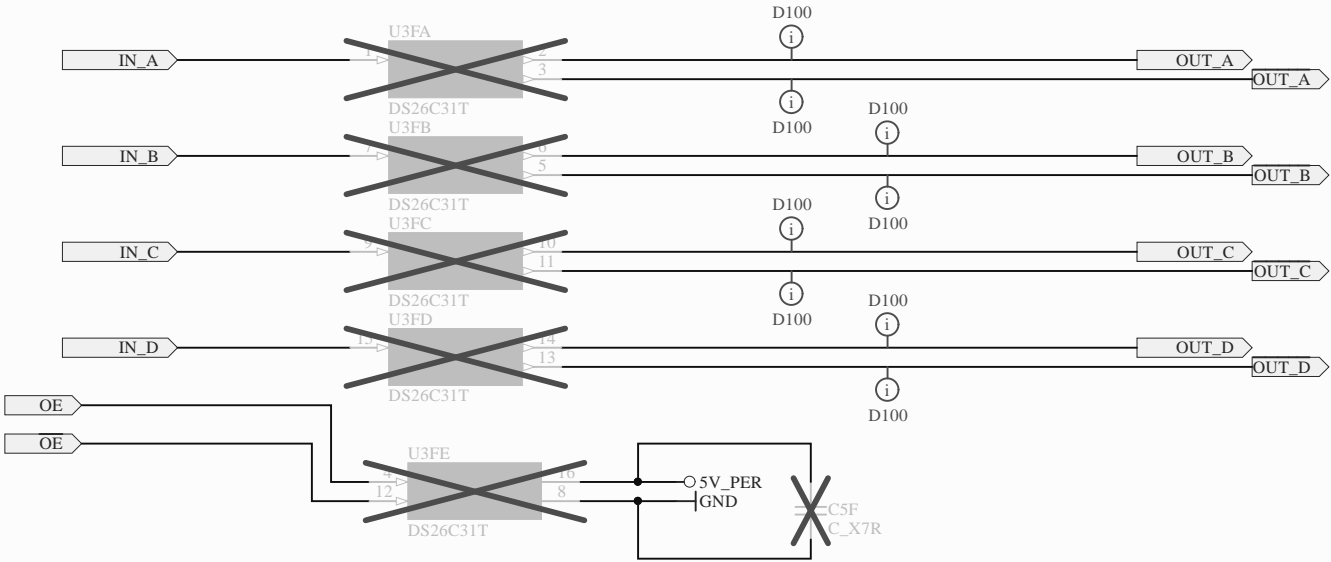
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VIN_low_max = 0.8V



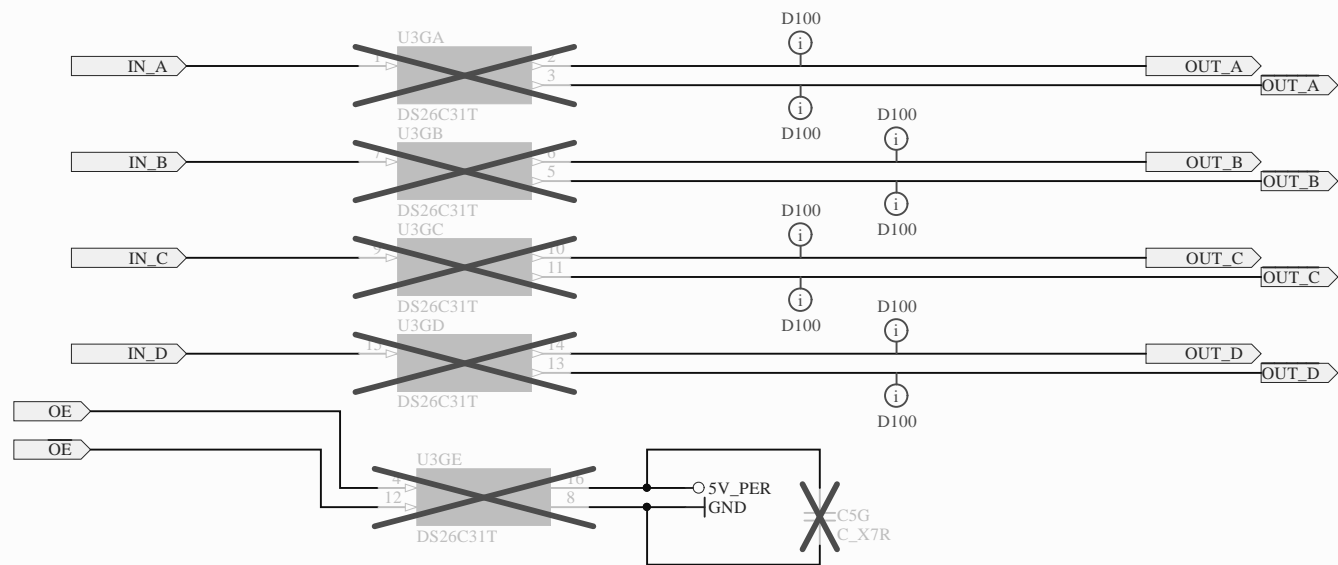
Application:
VDD_min = 4.5V
VDD_max 5.5V

VIN_high_min = 2.0V
VIN_low_max = 0.8V



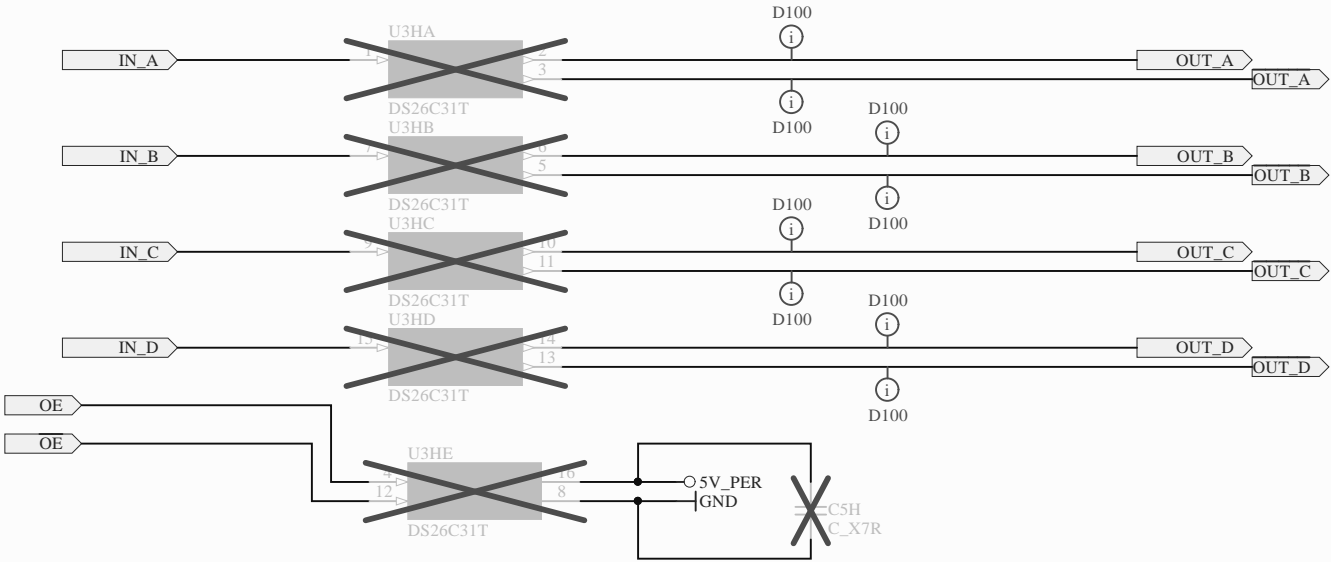
Application:
VDD_min = 4.5V
VDD_max 5.5V

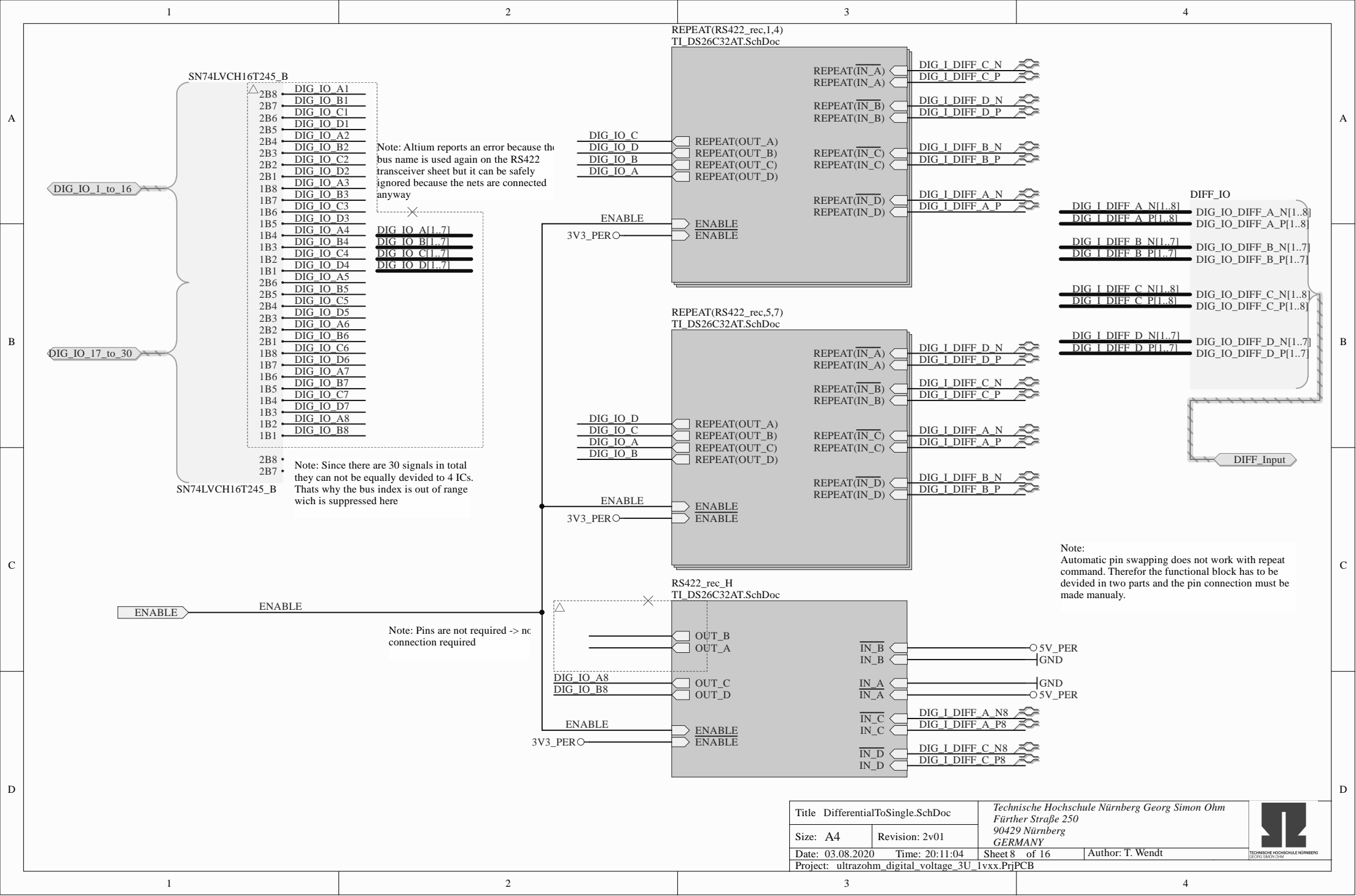
VIN_high_min = 2.0V
VIN_low_max = 0.8V

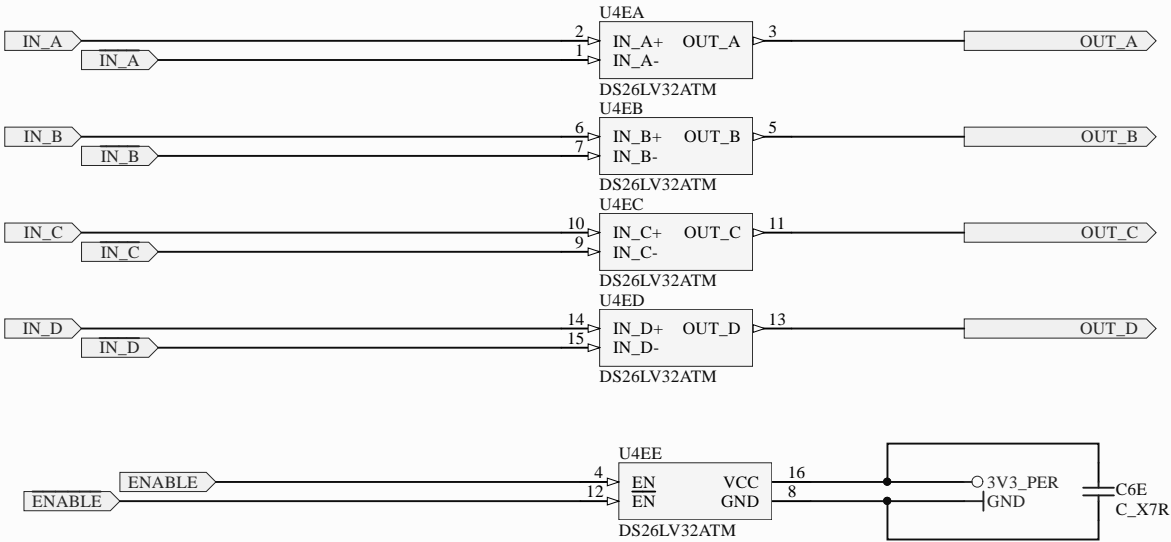


Application:
VDD_min = 4.5V
VDD_max 5.5V

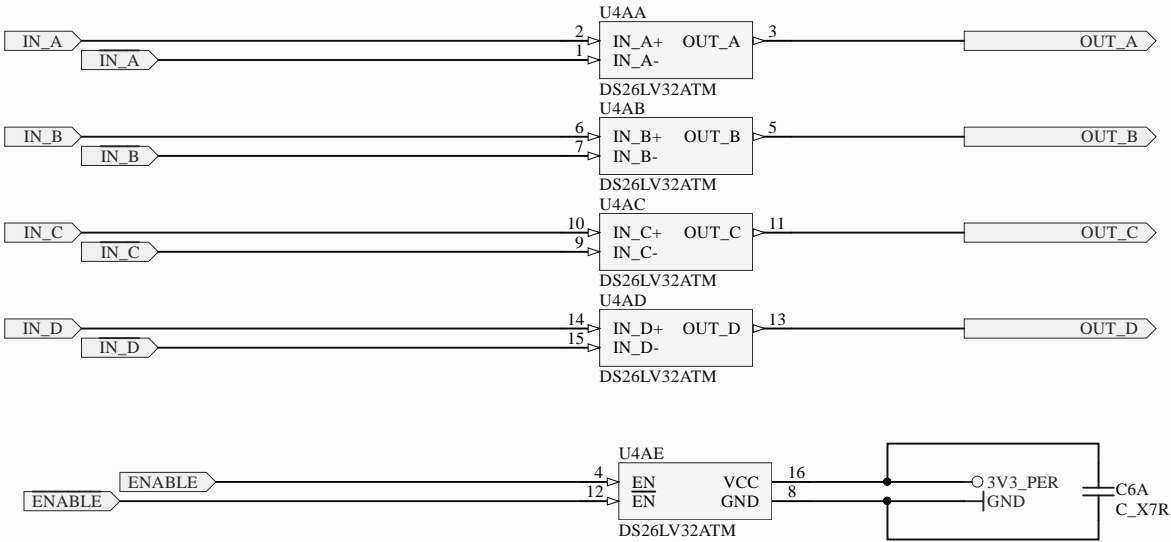
VIN_high_min = 2.0V
VIN_low_max = 0.8V



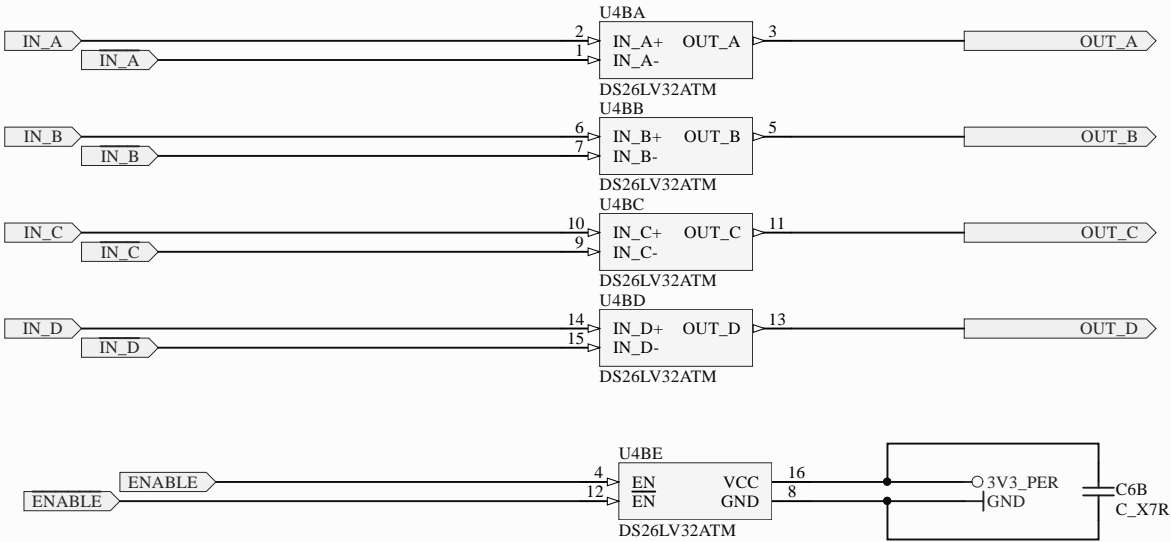




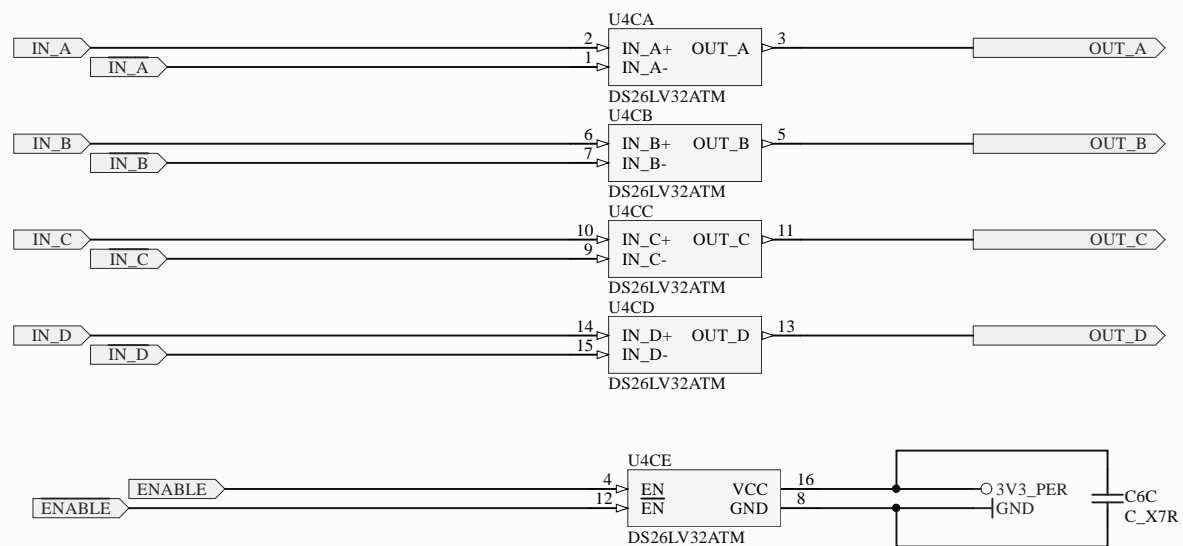
Application:
VDD_min = 3.0V
VDD_max = 3.6V



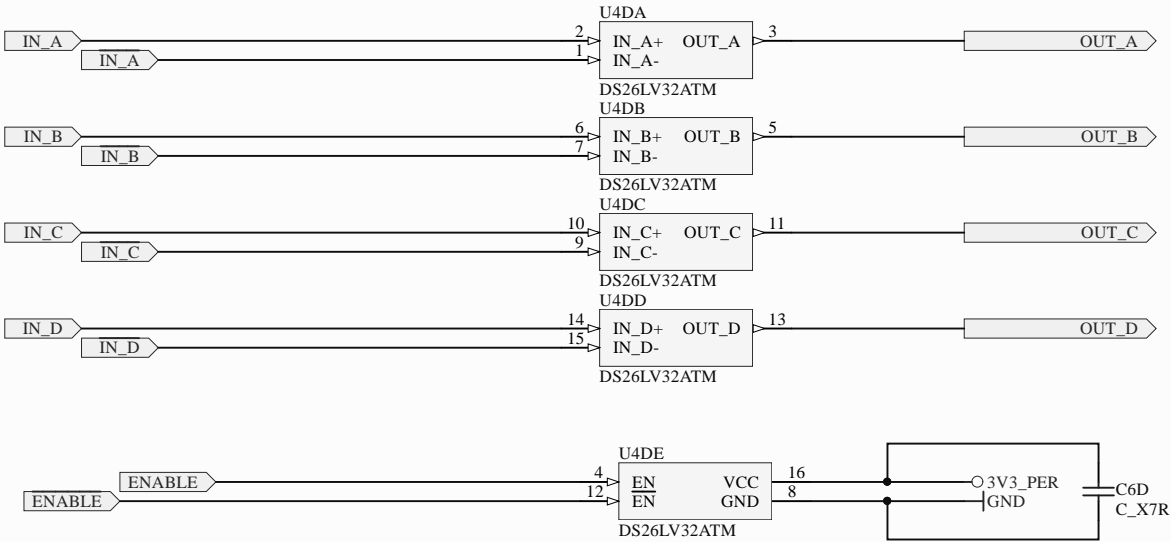
Application:
VDD_min = 3.0V
VDD_max = 3.6V



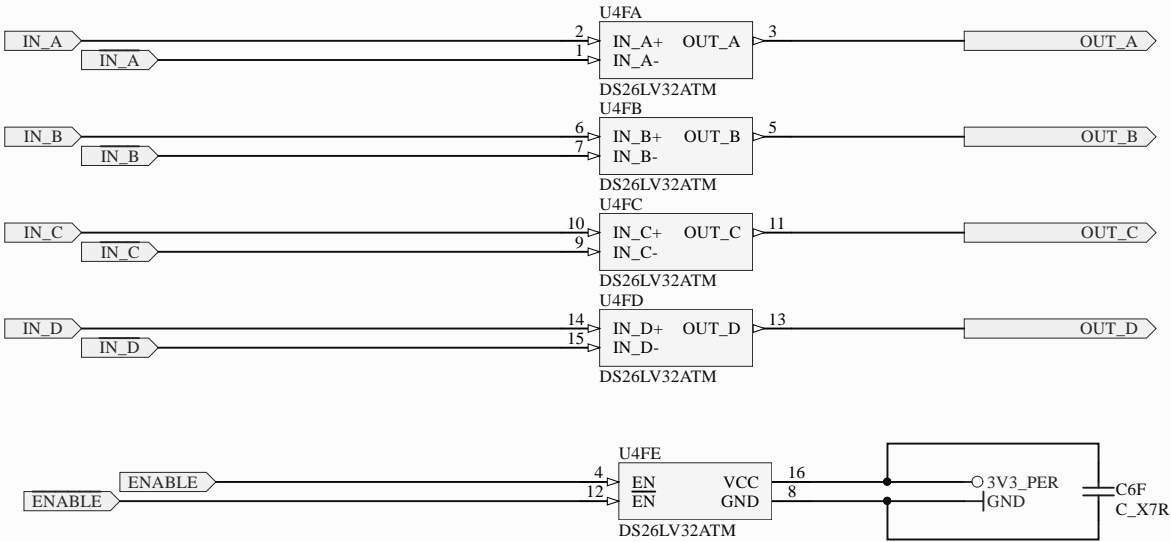
Application:
VDD_min = 3.0V
VDD_max = 3.6V



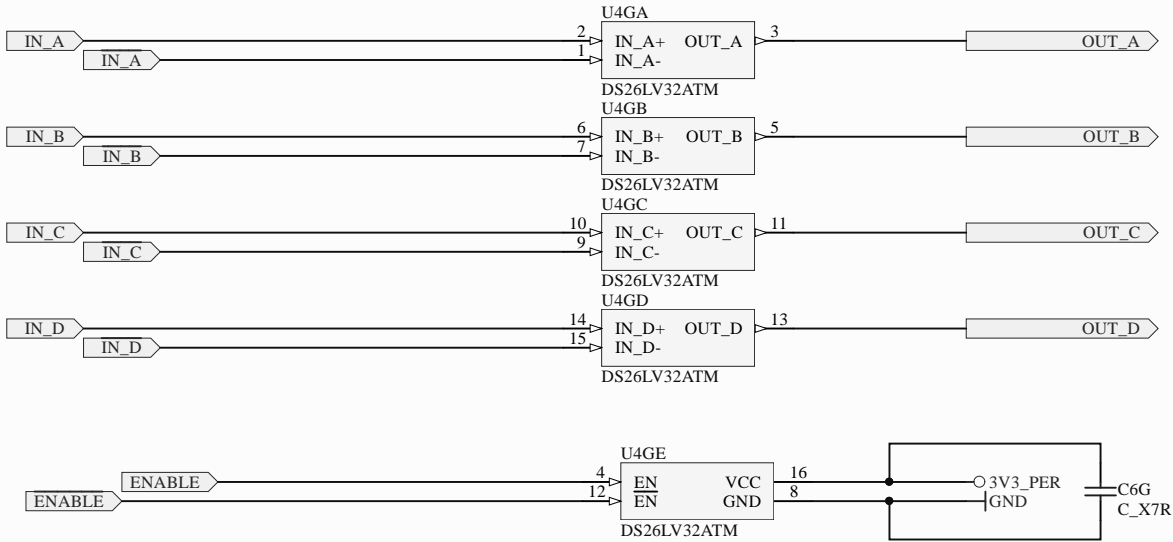
Application:
VDD_min = 3.0V
VDD_max = 3.6V



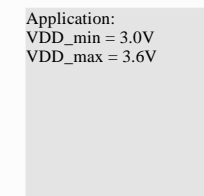
Application:
VDD_min = 3.0V
VDD_max = 3.6V




Application:
VDD_min = 3.0V
VDD_max = 3.6V



Application:
VDD_min = 3.0V
VDD_max = 3.6V



| | | | | |
|---------------------------------------|----------------|----------------------------------------------------------------------------------------------------------|------------------|---------------------------------------------------------------------------------------|
| Title TI_DS26C32AT.SchDoc | | <i>Technische Hochschule Nürnberg Georg Simon Ohm</i> Fürther Straße 250 90429 Nürnberg GERMANY | |  |
| Size: A4 | Revision: 2v01 | | | |
| Date: 03.08.2020 | Time: 20:11:05 | Sheet 9 of 16 | Author: T. Wendt | |
| Project: ultrazohm digital voltage 3U | | 1vxx.PriPCB | | |

A

B

C

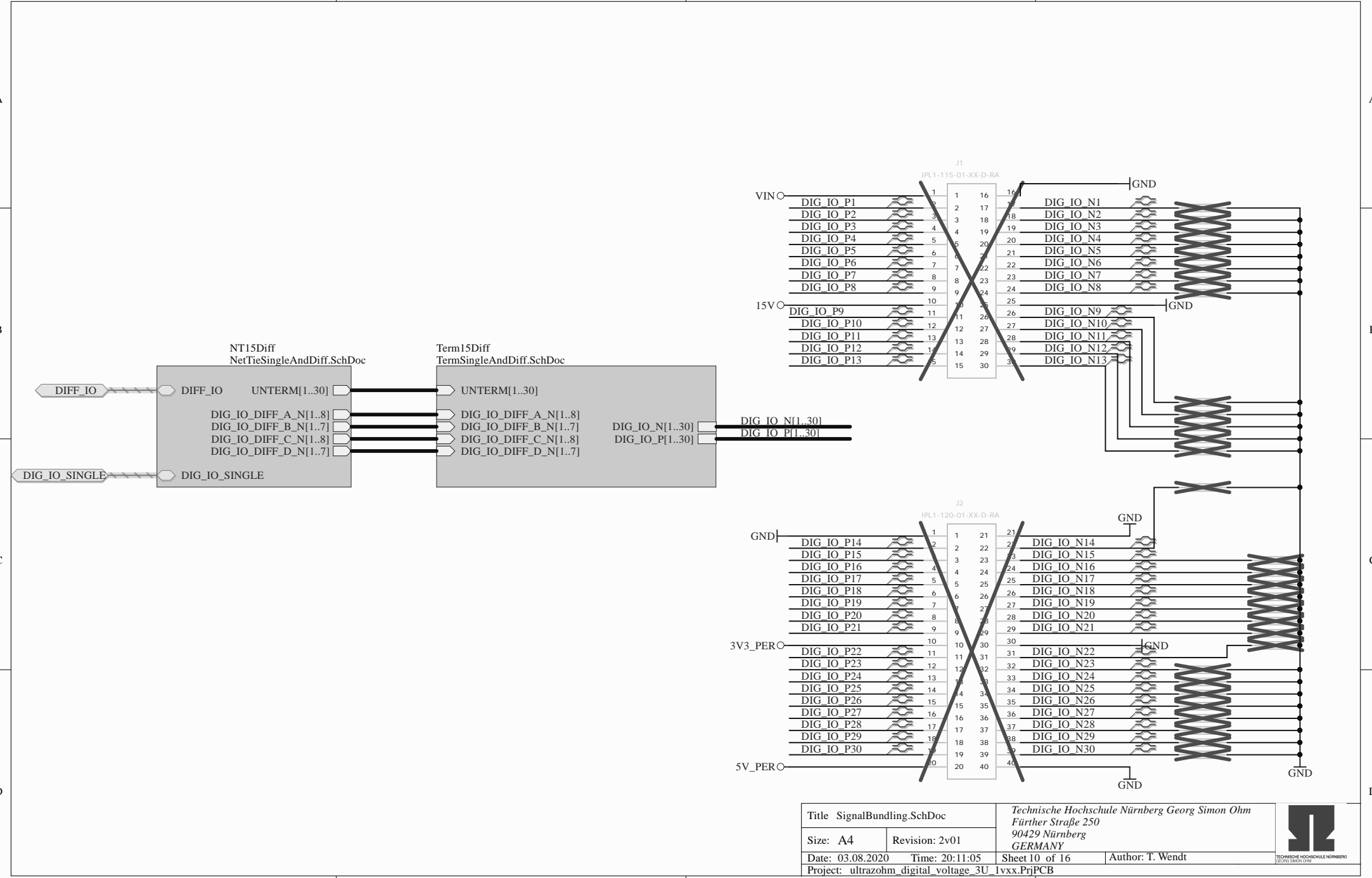
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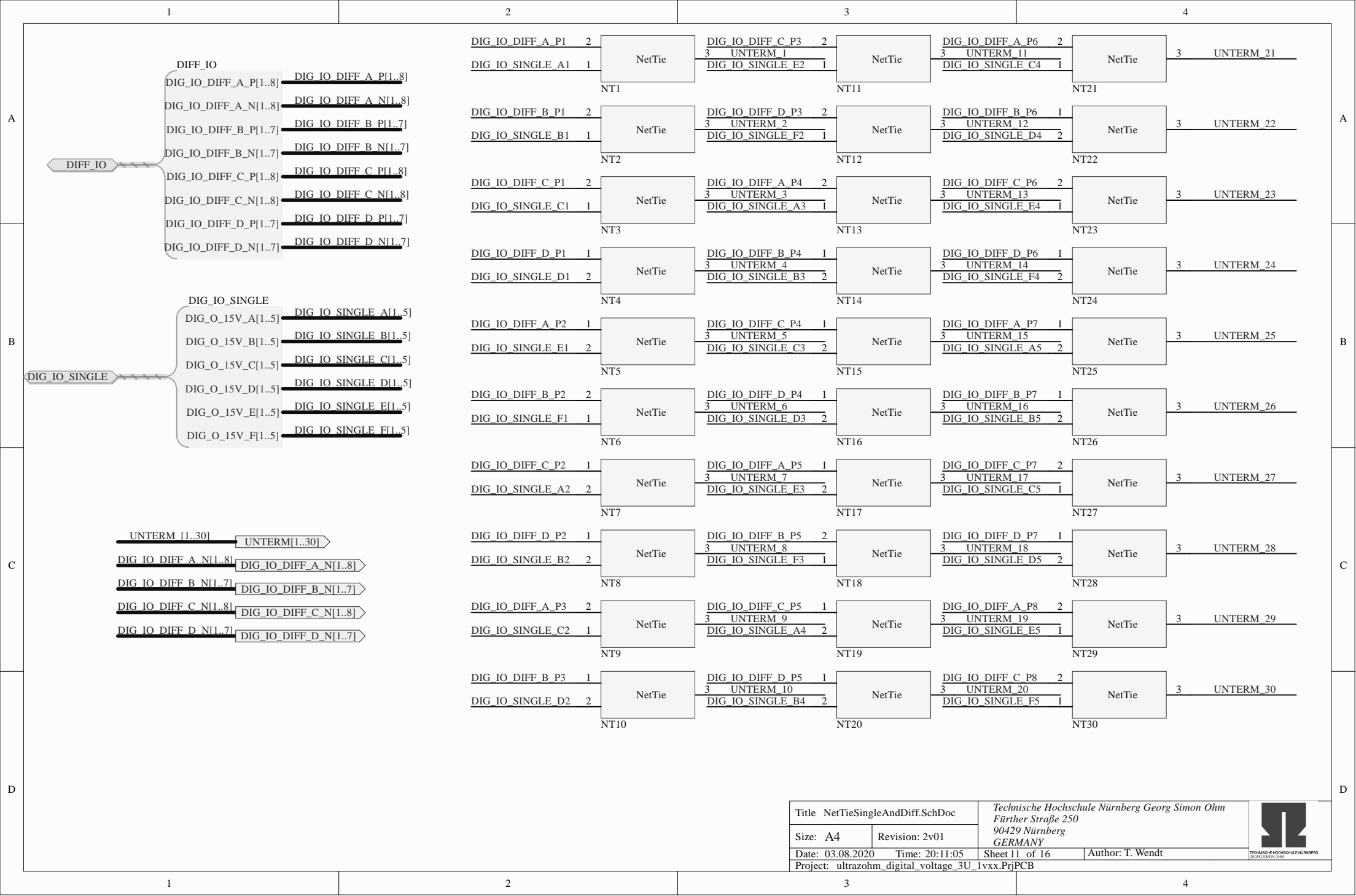
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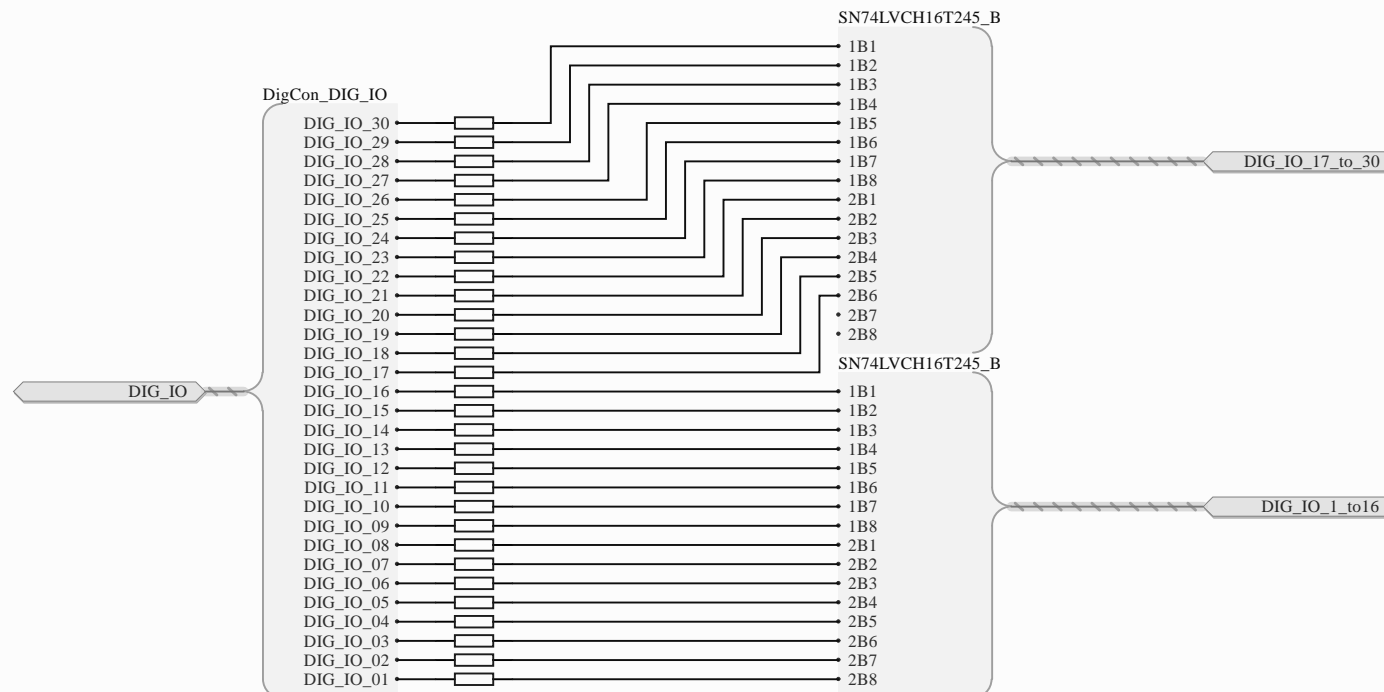
B


C

D







| | | | |
|---------------------------------------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Title Jumper5VLS.SchDoc | | Technische Hochschule Nürnberg Georg Simon Ohm Fürther Straße 250 90429 Nürnberg GERMANY | |
| Size: A4 | Revision: 2v01 |  <small>TECHNISCHE HOCHSCHULE NÜRNBERG GEORG SIMON OHM</small> | |
| Date: 03.08.2020 | Time: 20:11:05 | | |
| Project: ultrazohm_digital_voltage_3U_1vxx.PrjPCB | | Sheet 12 of 16 | Author: T. Wendt |

A

A

B

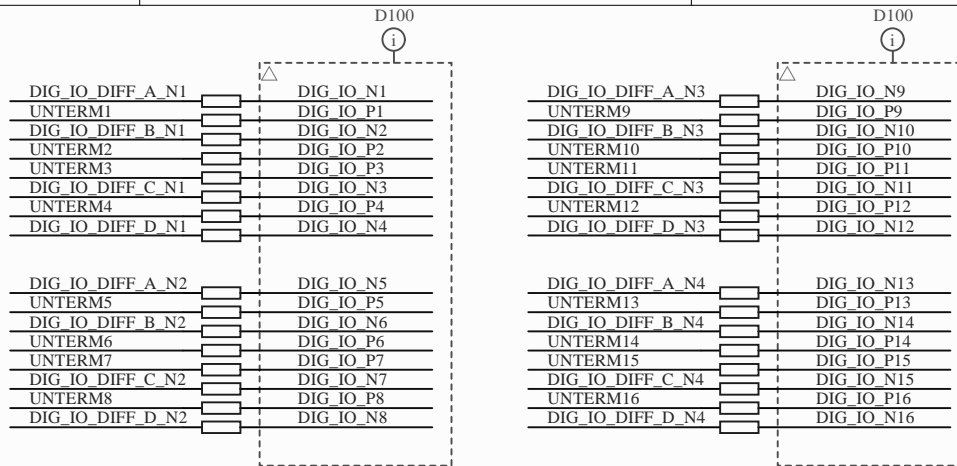
B

C

C

D

D



DIG IO P[1..30] → DIG_IO_P[1..30]

DIG IO N[1..30] → DIG_IO_N[1..30]

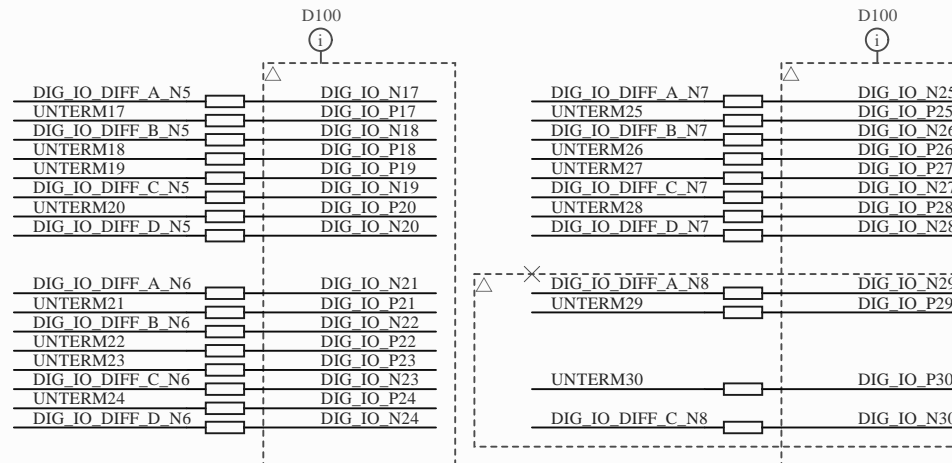
UNTERM[1..30] → UNTERM[1..30]

DIG_IO_DIFF_D_N[1..7] → DIG_IO_DIFF_D_N[1..7]

DIG_IO_DIFF_C_N[1..8] → DIG_IO_DIFF_C_N[1..8]

DIG_IO_DIFF_B_N[1..7] → DIG_IO_DIFF_B_N[1..7]

DIG_IO_DIFF_A_N[1..8] → DIG_IO_DIFF_A_N[1..8]

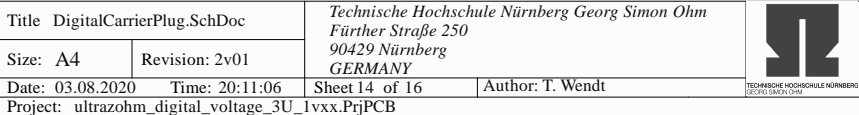


Note: The serial termination resistors are placed at the IO interface and not directly behind the level shifter from 3V3 to 5V, because 30 extra resistors would be required which implies additional assembly effort.

Note: If the board is configured as a receiver, the termination resistors can be replaced with jumpers.

| | | | |
|---------------------------------------------------|----------------|---------------------------------------------------------------------------------------------------|------------------|
| Title TermSingleAndDiff.SchDoc | | Technische Hochschule Nürnberg Georg Simon Ohm Fürther Straße 250 90429 Nürnberg GERMANY | |
| Size: A4 | Revision: 2v01 | | |
| Date: 03.08.2020 | Time: 20:11:06 | Sheet 13 of 16 | Author: T. Wendt |
| Project: ultrazohm_digital_voltage_3U_1vxx.PrjPCB | | | |





A

B

C

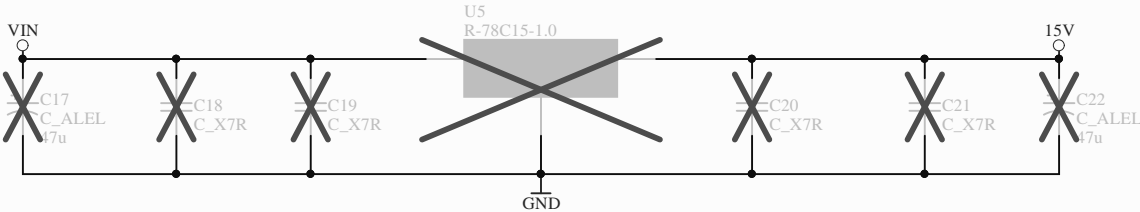
D

A

B

C

D



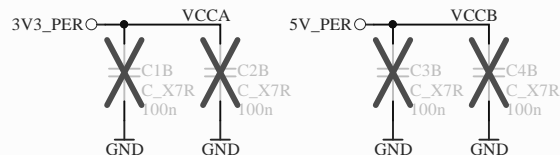
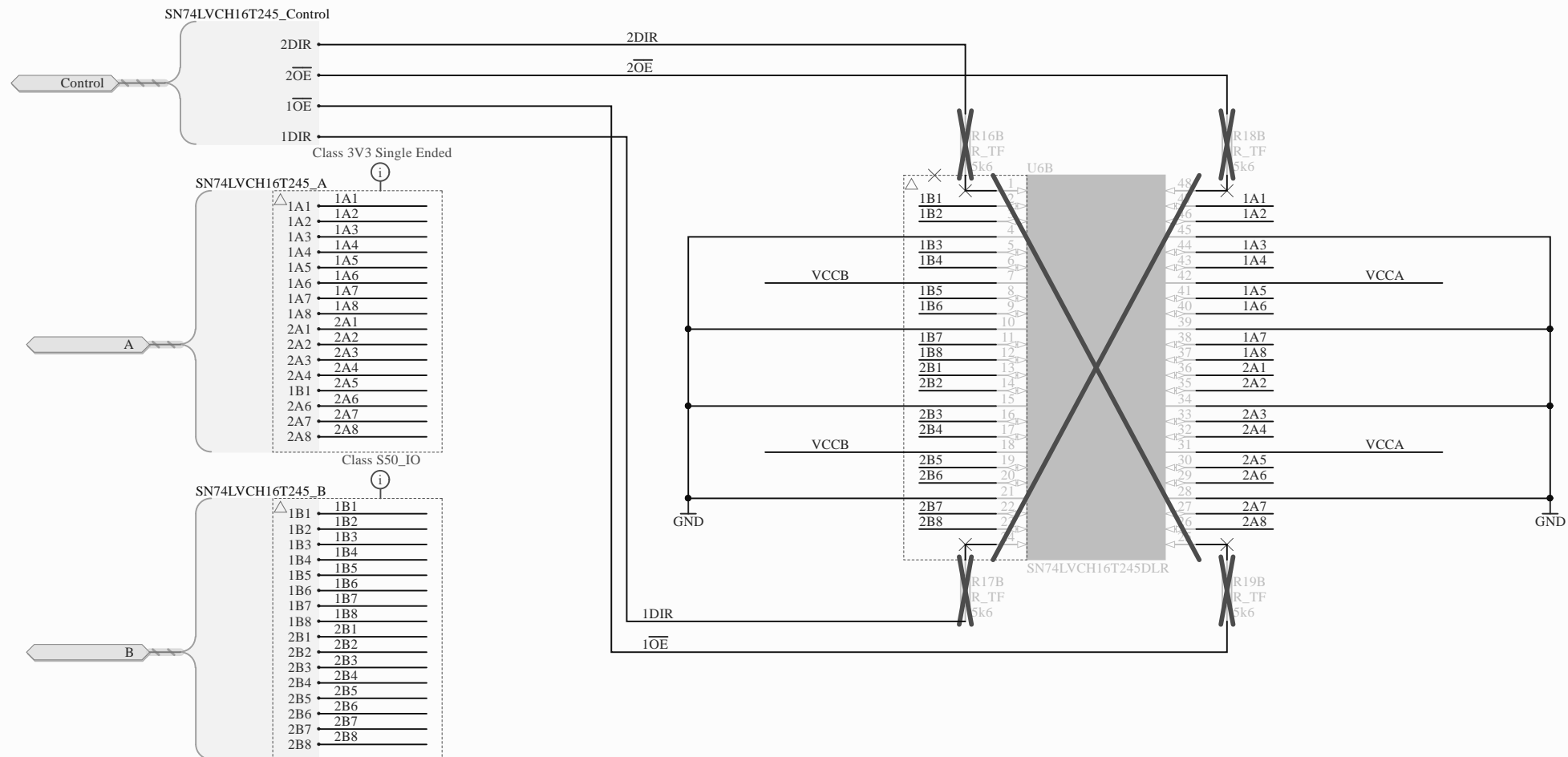
Totally integrated DCDC swichting converter.

Voltages:
Vin_max = 42V
Vin_min = 18V

Vout = 15V

Current:
Iout_max = 1A

Parameters:
VoutName = Name of the net of Vout
VinName = Name of the net of Vin



Application:

Voltages:
 $V_{CCA_min} = V_{CCB_min} = 1.65V$
 $V_{CCA_max} = V_{CCB_max} = 5.5V$

Note: Altium warns, that an IO pin (from the 5V LS) is connected to an output pin (from the RS422 transceivers). This does not matter because these parts are not assembled together. It can be suppressed.

Direction pins are driven trough the resistors