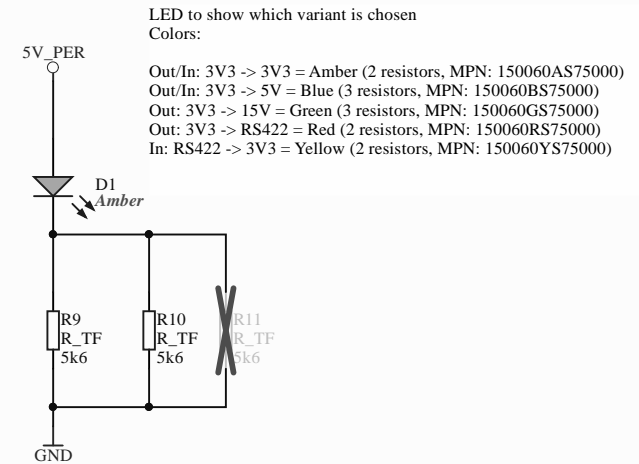


Note: Driving source is external (carrier board or just voltage)



### Revision

2v01

Serial  
Serial  
Serial #

Project


UltraZohm\_DigitalVoltage

Designer

T. Wendt

Date \_\_\_\_\_

08/2020

Title: TopSheet.SchDoc		Technische Hochschule Nürnberg Georg Simon Ohm Fürther Straße 250 90429 Nürnberg GERMANY		
Size: A4	Revision: 2v01			
Date: 03.08.2020	Time: 20:10:03	Sheet 1 of 16	Author: T. Wendt	
Project: ultrazohm_digital_voltage_3U_1vxx.PrjPCB				

A

B

C

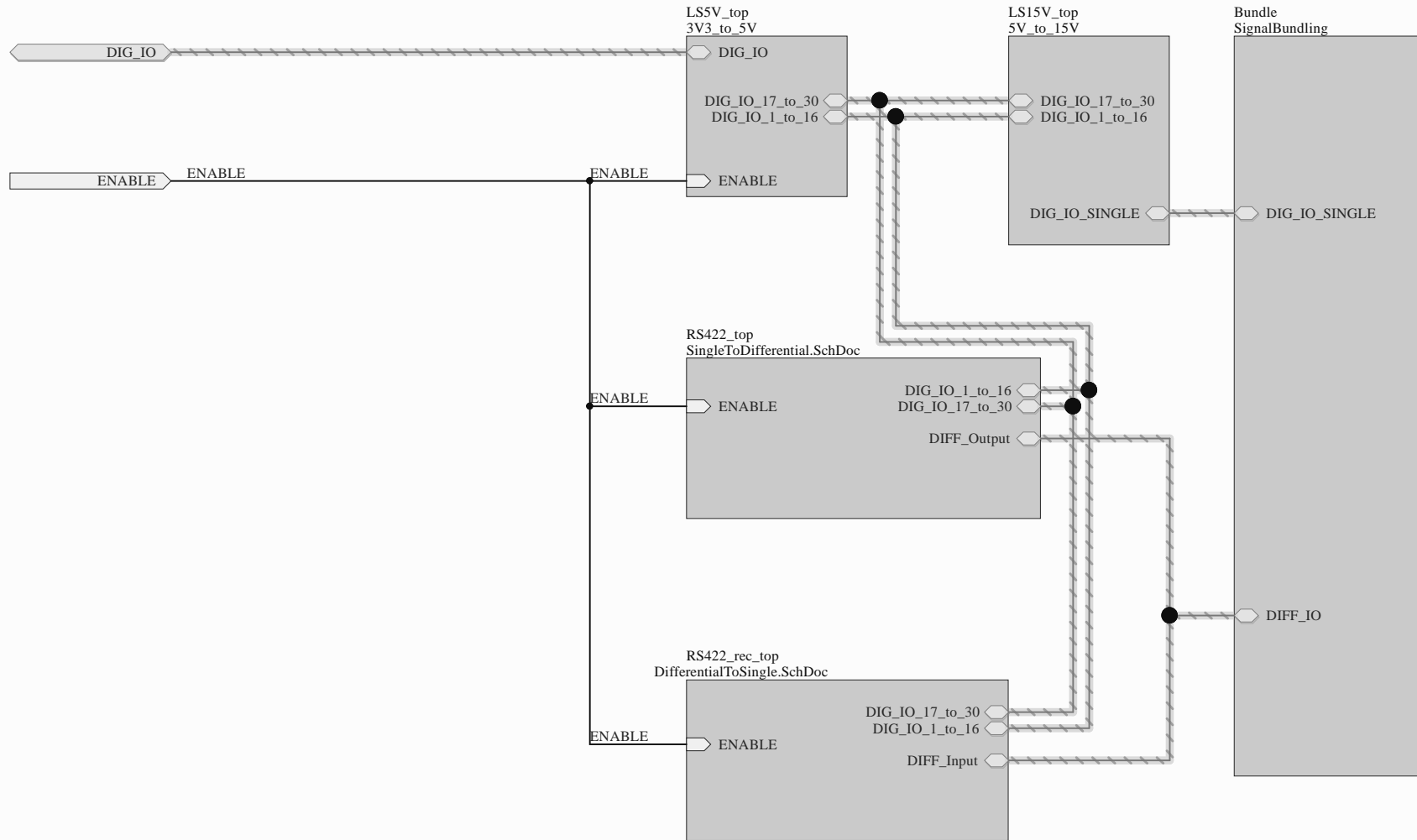
D

A

B

C

D



A

A

B

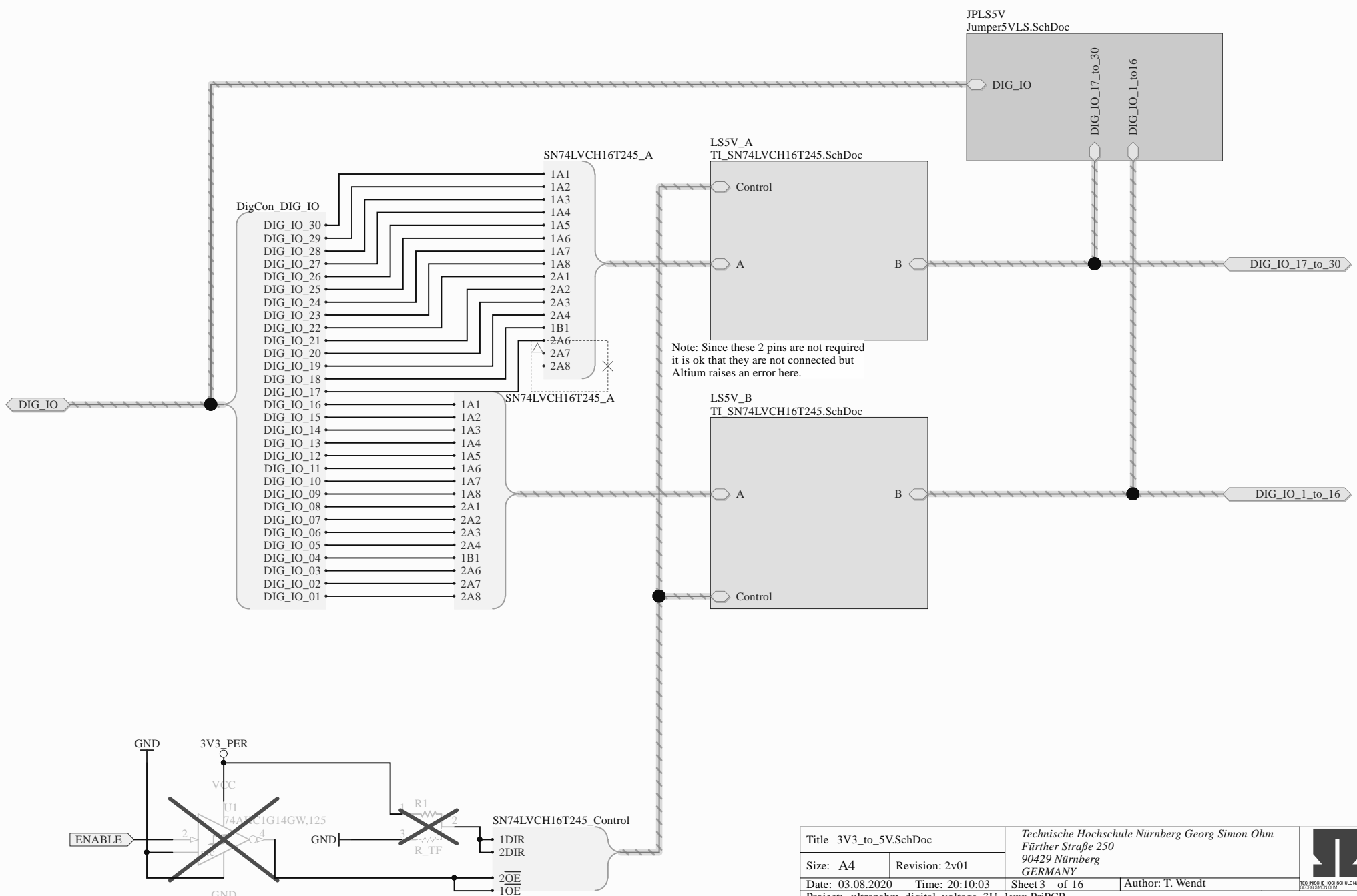
B

C

C

D

D



SN74LVCH16T245\_B

2B8 DIG\_IO\_5V\_A1  
2B7 DIG\_IO\_5V\_B1  
2B6 DIG\_IO\_5V\_C1  
2B5 DIG\_IO\_5V\_D1  
2B4 DIG\_IO\_5V\_E1  
2B3 DIG\_IO\_5V\_F1  
2B2 DIG\_IO\_5V\_A2  
2B1 DIG\_IO\_5V\_B2  
1B8 DIG\_IO\_5V\_C2  
1B7 DIG\_IO\_5V\_D2  
1B6 DIG\_IO\_5V\_E2  
1B5 DIG\_IO\_5V\_F2  
1B4 DIG\_IO\_5V\_A3  
1B3 DIG\_IO\_5V\_B3  
1B2 DIG\_IO\_5V\_C3  
1B1 DIG\_IO\_5V\_D3

DIG\_IO\_1\_to\_16

~~DIG\_IO\_5V\_A[1..5]~~  
~~DIG\_IO\_5V\_B[1..5]~~  
~~DIG\_IO\_5V\_C[1..5]~~  
~~DIG\_IO\_5V\_D[1..5]~~  
~~DIG\_IO\_5V\_E[1..5]~~  
~~DIG\_IO\_5V\_F[1..5]~~

DIG\_IO\_SINGLE

~~DIG\_IO\_SINGLE\_A[1..5]~~  
~~DIG\_IO\_SINGLE\_B[1..5]~~  
~~DIG\_IO\_SINGLE\_C[1..5]~~  
~~DIG\_IO\_SINGLE\_D[1..5]~~  
~~DIG\_IO\_SINGLE\_E[1..5]~~  
~~DIG\_IO\_SINGLE\_F[1..5]~~

DIG\_O\_15V\_A[1..5]  
DIG\_O\_15V\_B[1..5]  
DIG\_O\_15V\_C[1..5]  
DIG\_O\_15V\_D[1..5]  
DIG\_O\_15V\_E[1..5]  
DIG\_O\_15V\_F[1..5]

DIG\_IO\_SINGLE

Note: Since these 2 pins are not required  
it is ok that they are not connected but  
Altium raises an error here.

SN74LVCH16T245\_B

2B8  
2B7 DIG\_IO\_5V\_E3  
2B6 DIG\_IO\_5V\_F3  
2B5 DIG\_IO\_5V\_A4  
2B4 DIG\_IO\_5V\_B4  
2B3 DIG\_IO\_5V\_C4  
2B2 DIG\_IO\_5V\_D4  
2B1 DIG\_IO\_5V\_E4  
1B8 DIG\_IO\_5V\_F4  
1B7 DIG\_IO\_5V\_A5  
1B6 DIG\_IO\_5V\_B5  
1B5 DIG\_IO\_5V\_C5  
1B4 DIG\_IO\_5V\_D5  
1B3 DIG\_IO\_5V\_E5  
1B2 DIG\_IO\_5V\_F5  
1B1

DIG\_IO\_17\_to\_30

REPEAT(LS15V,1,5)  
ONSEMI\_MC14504BDR2G

DIG\_IO\_5V\_A  
DIG\_IO\_5V\_B  
DIG\_IO\_5V\_C  
DIG\_IO\_5V\_E  
DIG\_IO\_5V\_F  
DIG\_IO\_5V\_D

REPEAT(AIN)  
REPEAT(BIN)  
REPEAT(CIN)  
REPEAT(DIN)  
REPEAT(EIN)  
REPEAT(FIN)  
REPEAT(AOUT)  
REPEAT(BOUT)  
REPEAT(COUT)  
REPEAT(DOUT)  
REPEAT(EOUT)  
REPEAT(FOUT)

DIG\_IO\_SINGLE A  
DIG\_IO\_SINGLE B  
DIG\_IO\_SINGLE C  
DIG\_IO\_SINGLE E  
DIG\_IO\_SINGLE F  
DIG\_IO\_SINGLE D

S50  
S50  
S50  
S50  
S50  
S50

5V\_PERO  
GND  
R2  
R\_TF

MODE

A

A

B

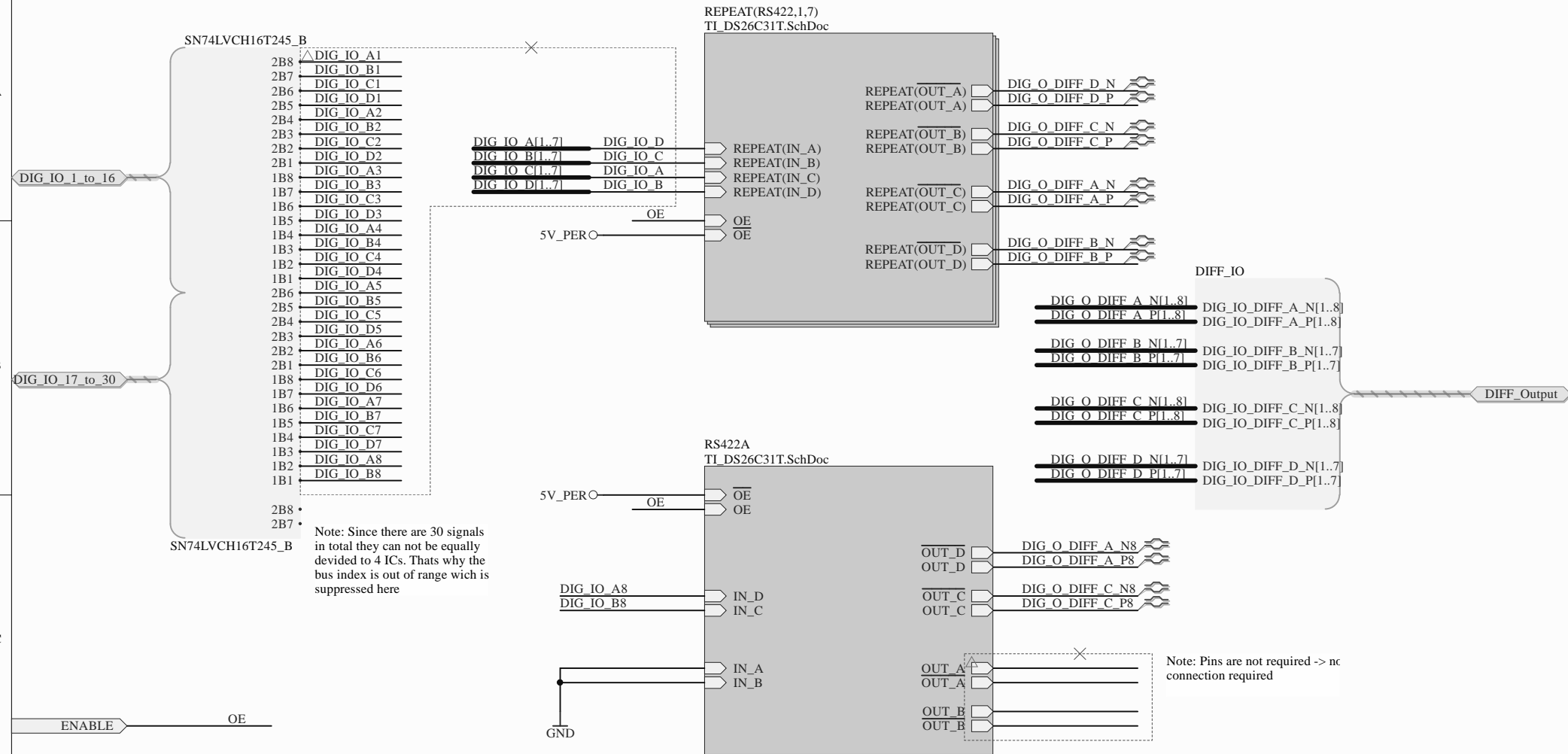
B

C

C

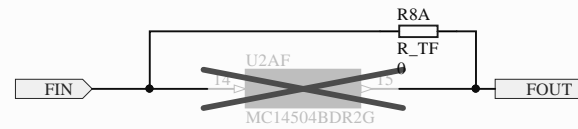
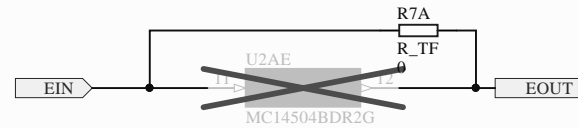
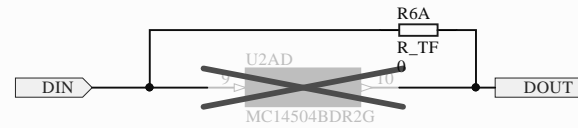
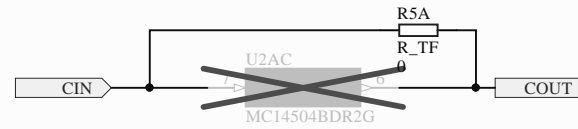
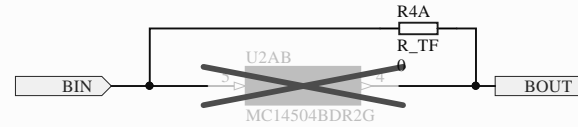
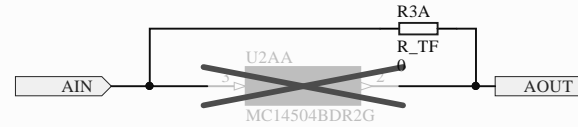
D

D



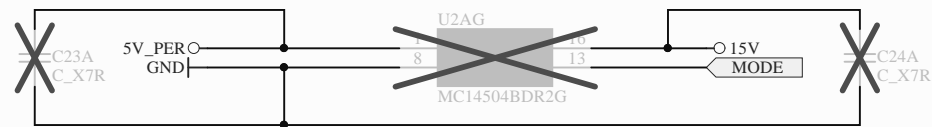
A

A




Voltages:  
VCC = voltage level of the input signal  
VDD = output voltage level

Application:  
MODE = VCC -> TTL logic level input  
MODE = VSS -> CMOS logic level input



D

D

Title		ONSEMI_MC14504BDR2G.SchDoc		<i>Technische Hochschule Nürnberg Georg Simon Ohm</i> Fürther Straße 250 90429 Nürnberg GERMANY		
Size:	A4	Revision:	2v01			
Date:	03.08.2020	Time:	20:10:03	Sheet 6 of 16	Author: T. Wendt	
Project: ultrazohm_digital_voltage_3U_1vxx.PrjPCB						

A

A

B

B

C

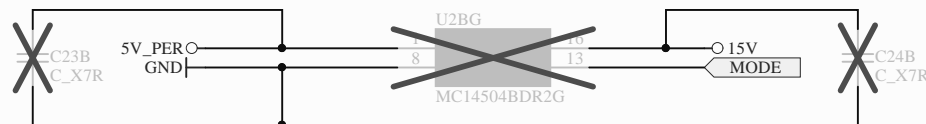
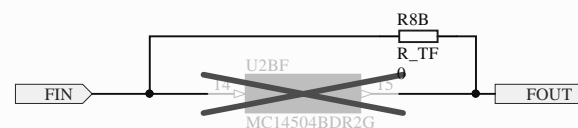
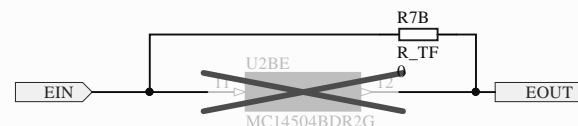
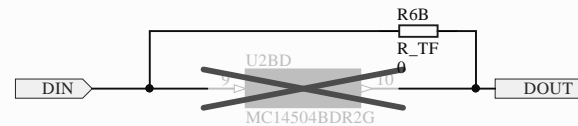
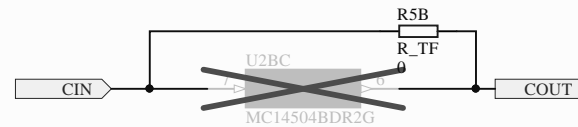
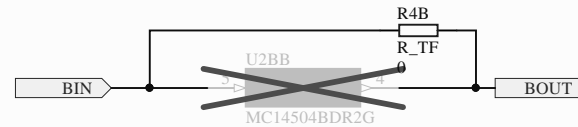
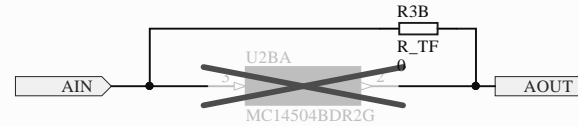
C

D

D

Voltages:  
VCC = voltage level of the input signal  
VDD = output voltage level

Application:  
MODE = VCC -> TTL logic level input  
MODE = VSS -> CMOS logic level input



A

A

B

B

C

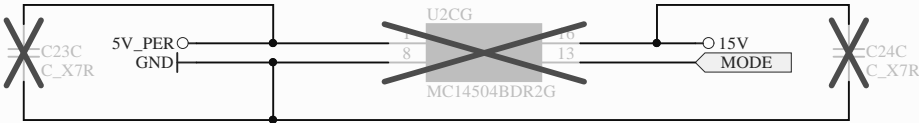
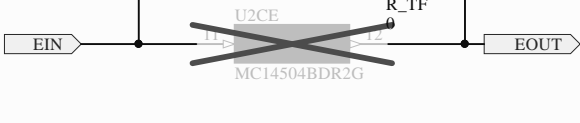
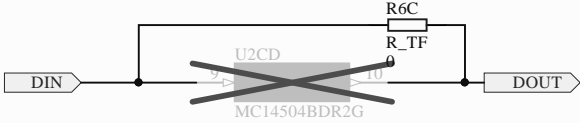
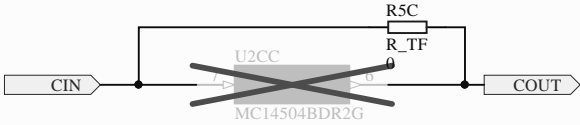
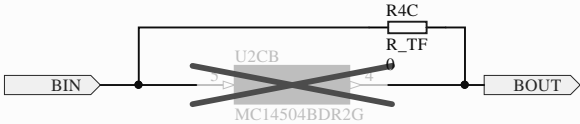
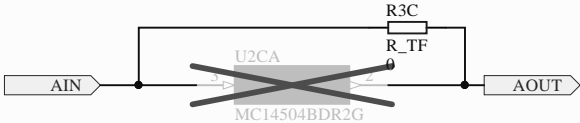
C

D

D

Voltages:  
VCC = voltage level of the input signal  
VDD = output voltage level

Application:  
MODE = VCC -> TTL logic level input  
MODE = VSS -> CMOS logic level input





A

A

B

B

C

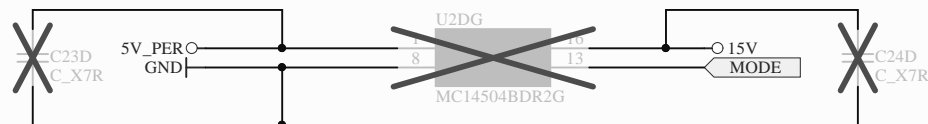
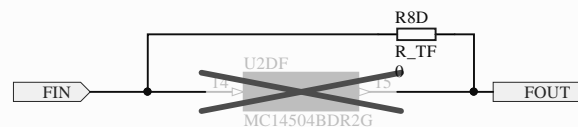
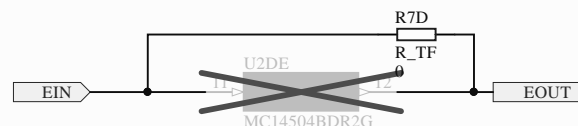
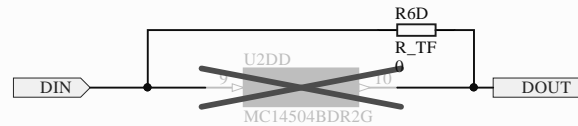
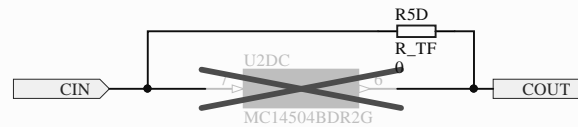
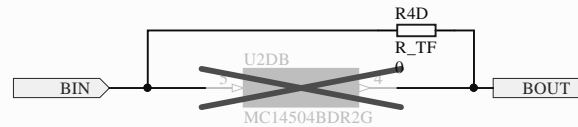
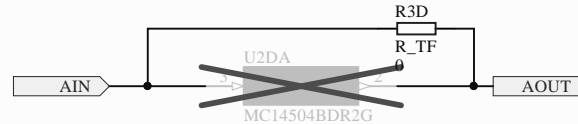
C

D

D

Voltages:  
VCC = voltage level of the input signal  
VDD = output voltage level

Application:  
MODE = VCC -> TTL logic level input  
MODE = VSS -> CMOS logic level input



A

A

B

B

C

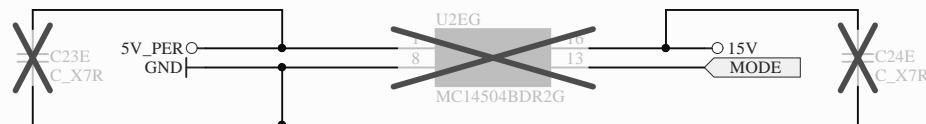
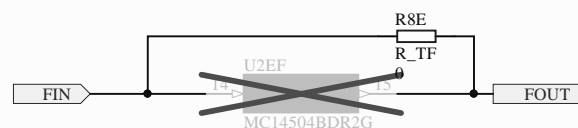
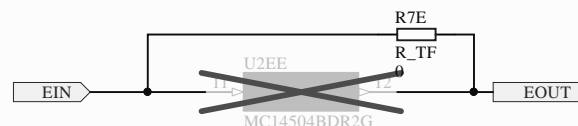
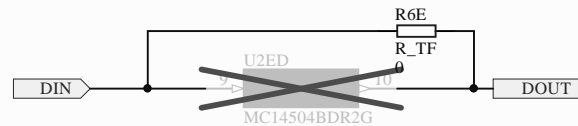
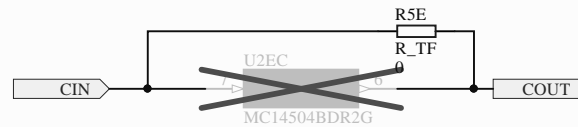
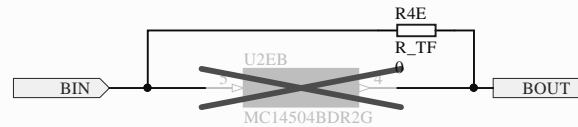
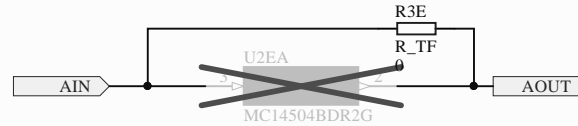
C

D

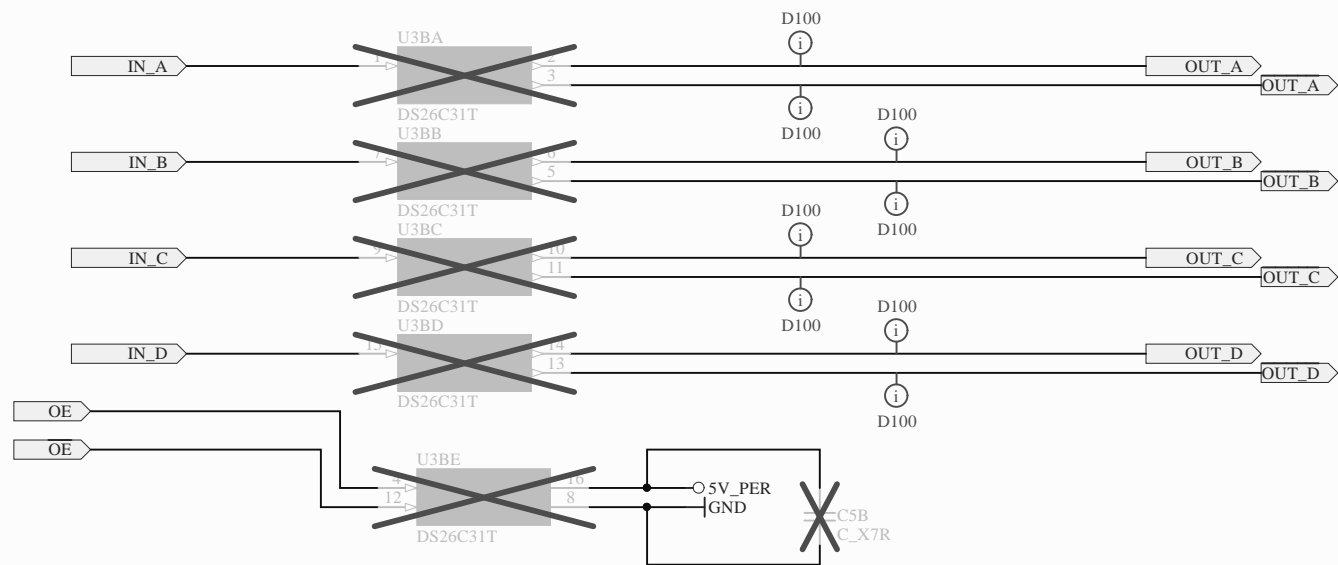
D

Voltages:  
VCC = voltage level of the input signal  
VDD = output voltage level

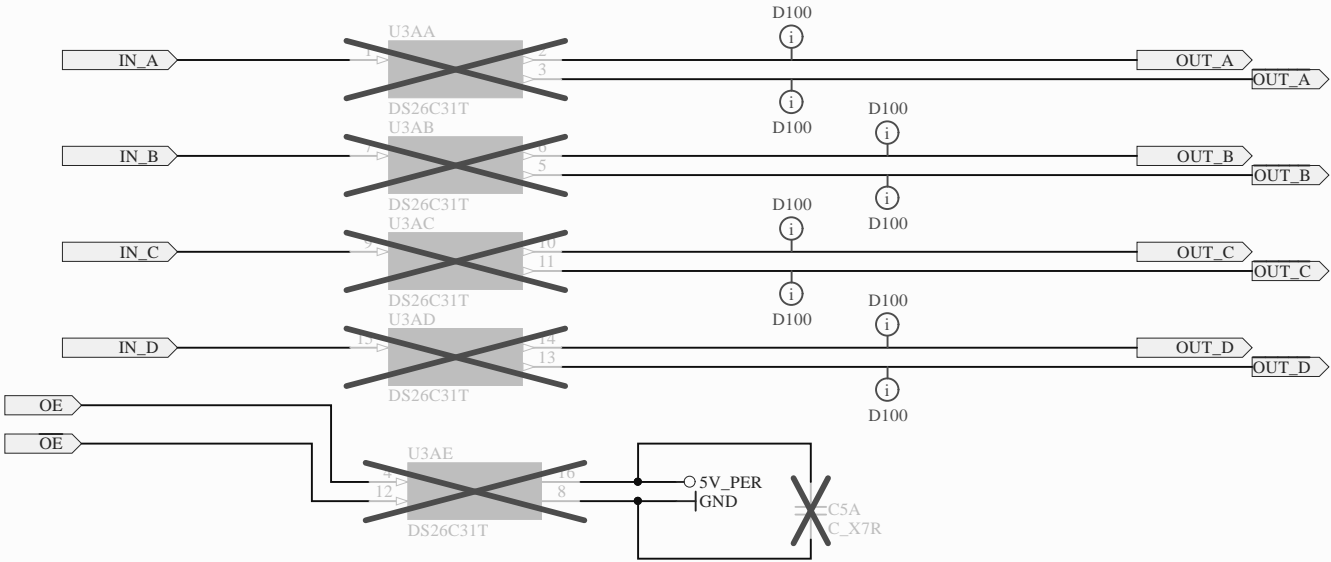
Application:  
MODE = VCC -> TTL logic level input  
MODE = VSS -> CMOS logic level input



Application:  
VDD\_min = 4.5V  
VDD\_max 5.5V  
  
VIN\_high\_min = 2.0V  
VIN\_low\_max = 0.8V

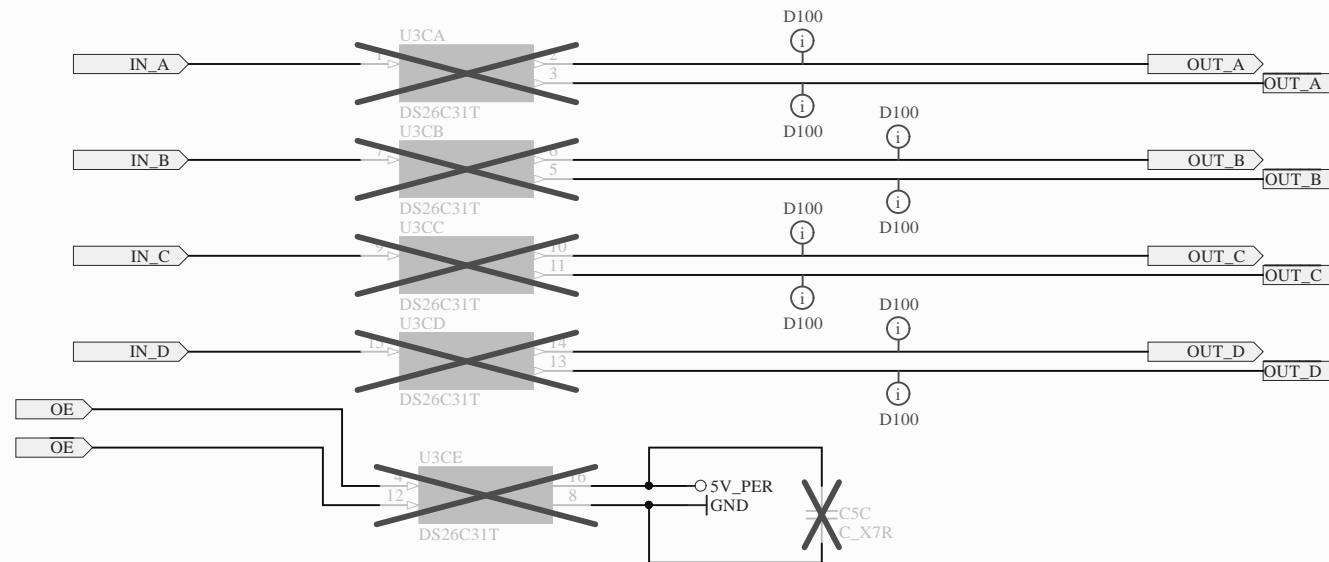


Application:  
VDD\_min = 4.5V  
VDD\_max 5.5V  
  
VIN\_high\_min = 2.0V  
VIN\_low\_max = 0.8V

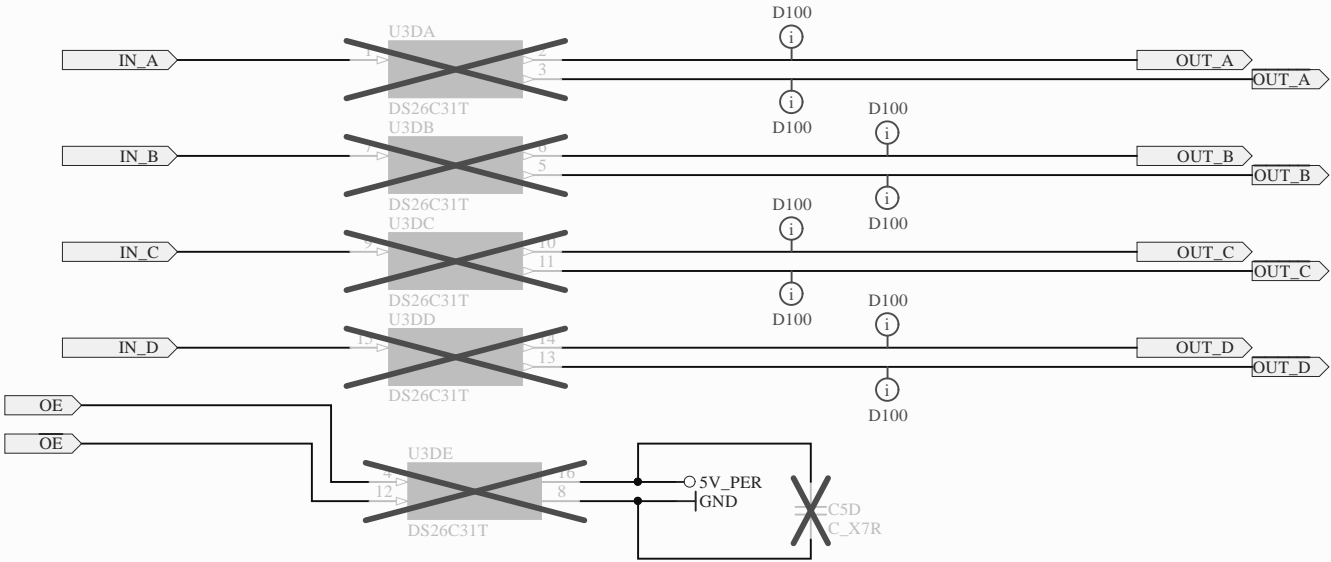


Application:  
VDD\_min = 4.5V  
VDD\_max 5.5V

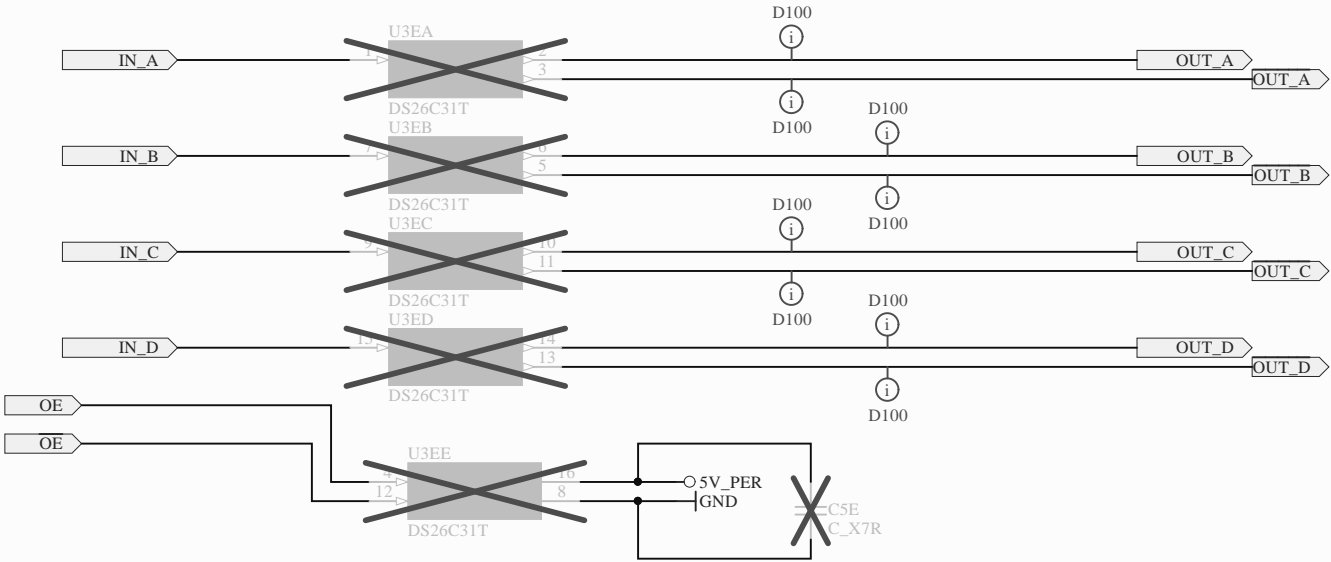
VIN\_high\_min = 2.0V  
VIN\_low\_max = 0.8V



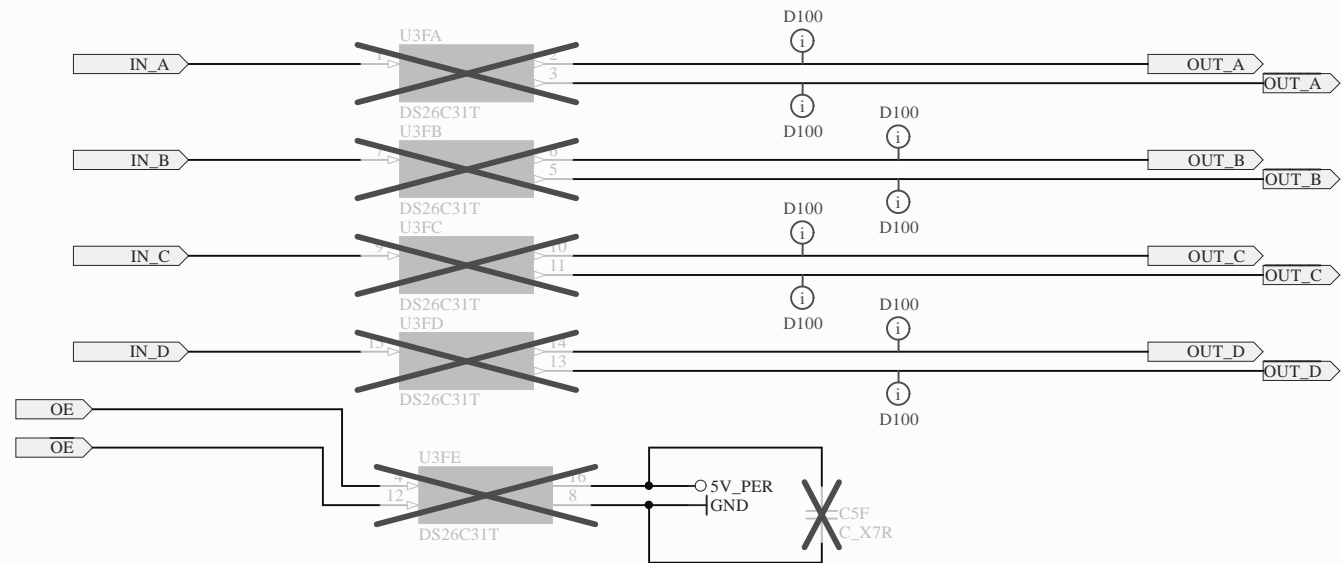
Application:  
VDD\_min = 4.5V  
VDD\_max 5.5V  
  
VIN\_high\_min = 2.0V  
VIN\_low\_max = 0.8V



Application:  
VDD\_min = 4.5V  
VDD\_max 5.5V  
  
VIN\_high\_min = 2.0V  
VIN\_low\_max = 0.8V

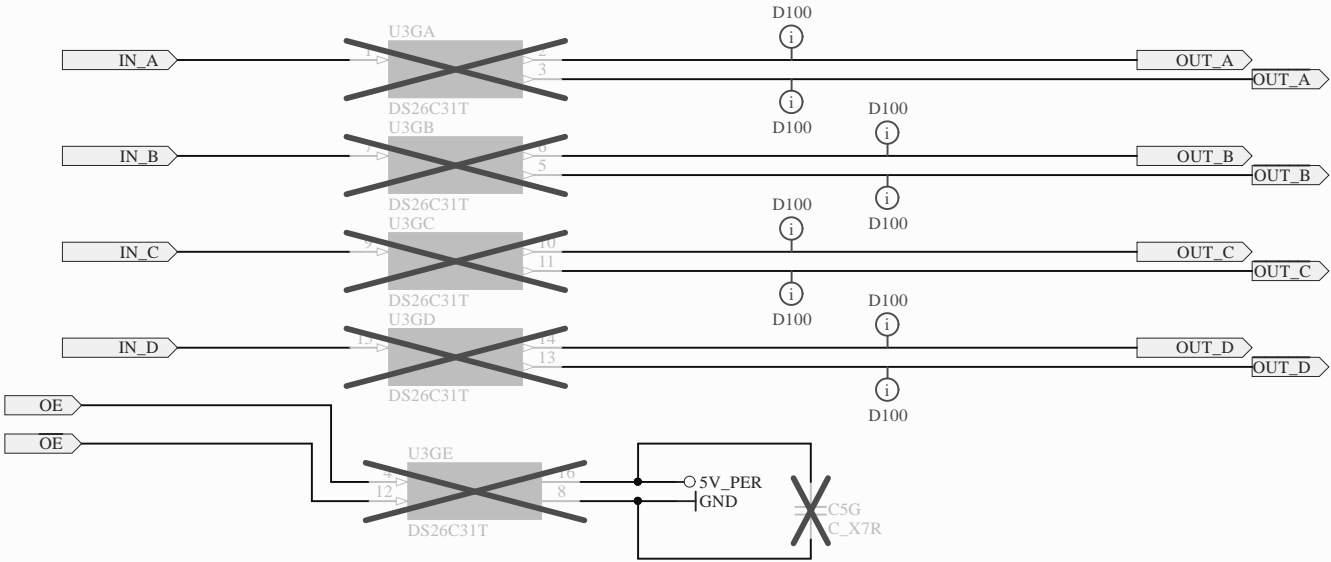


Application:  
VDD\_min = 4.5V  
VDD\_max 5.5V  
  
VIN\_high\_min = 2.0V  
VIN\_low\_max = 0.8V

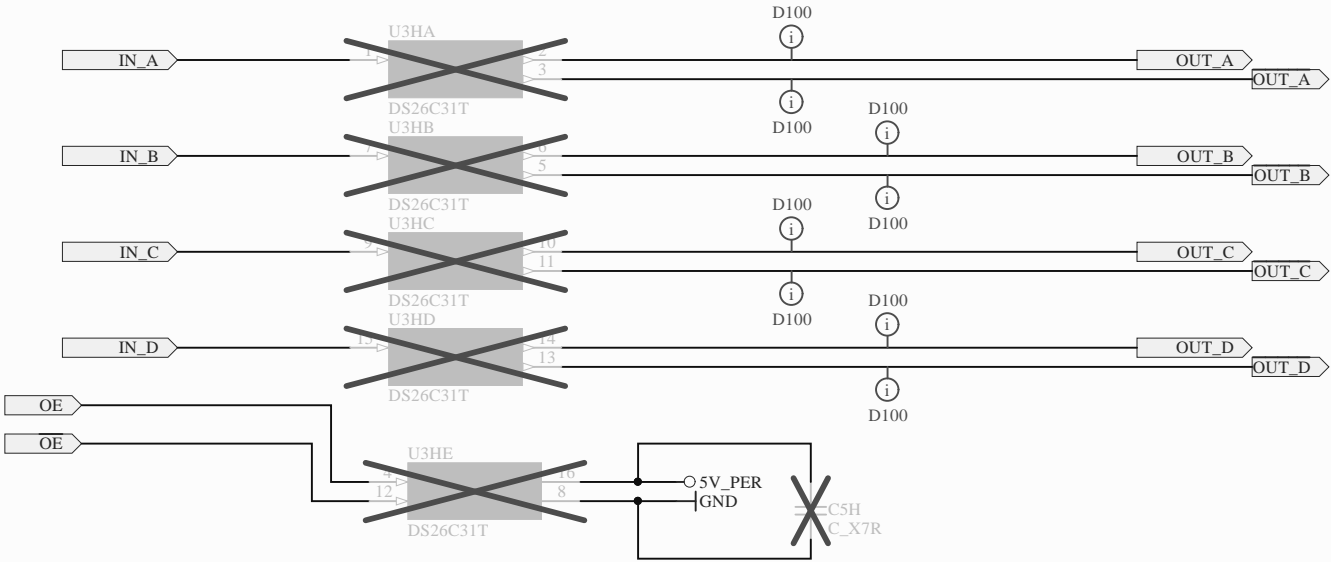


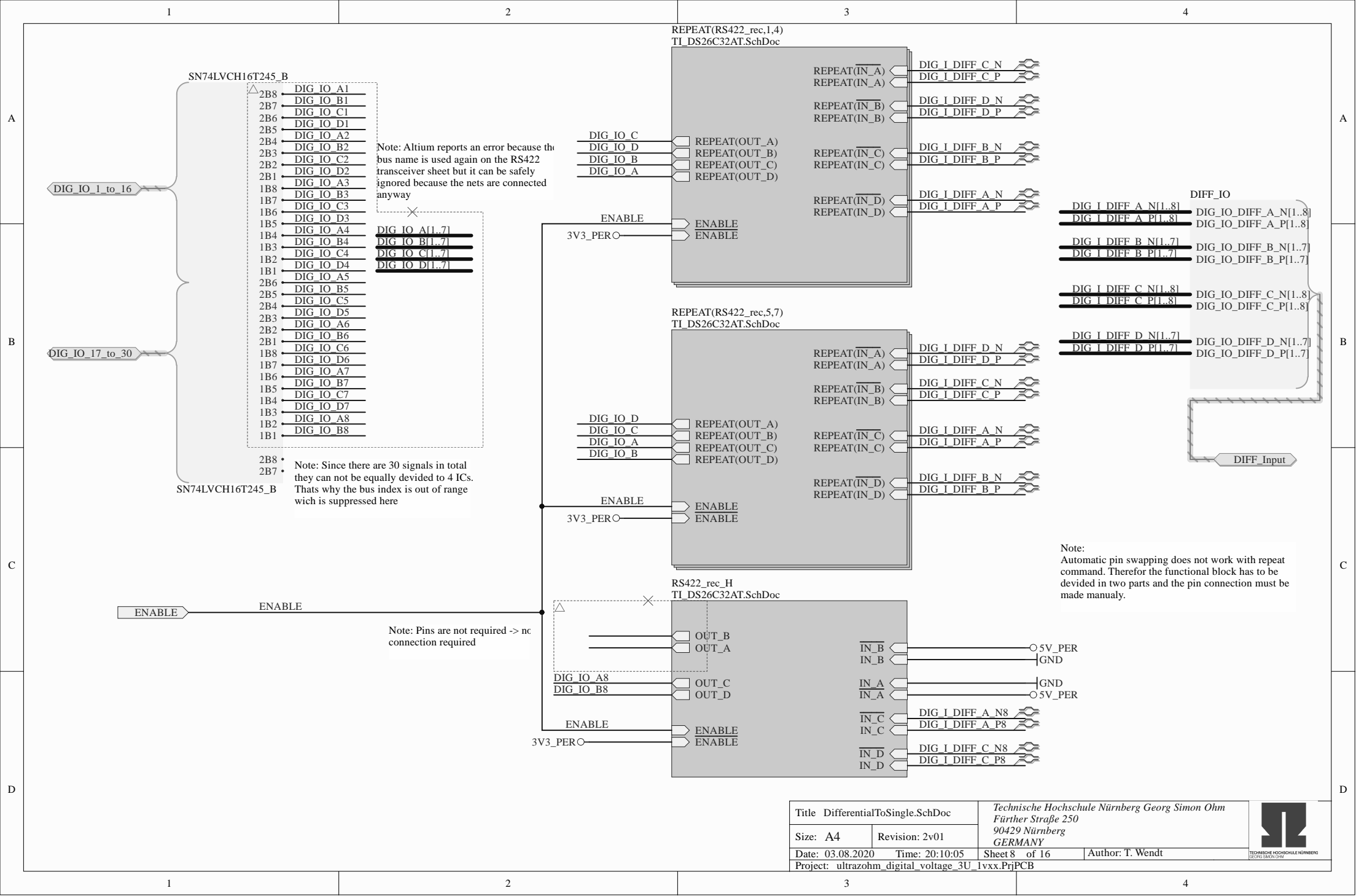


Application:  
VDD\_min = 4.5V  
VDD\_max 5.5V  
  
VIN\_high\_min = 2.0V  
VIN\_low\_max = 0.8V



Application:  
VDD\_min = 4.5V  
VDD\_max 5.5V  
  
VIN\_high\_min = 2.0V  
VIN\_low\_max = 0.8V





A

A

B

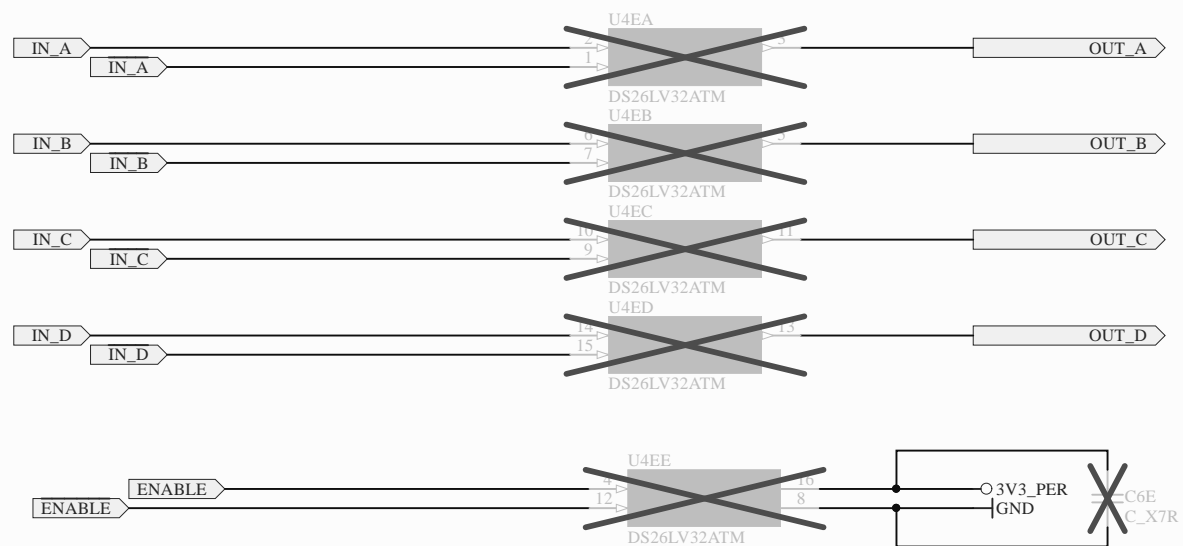
B

C



C

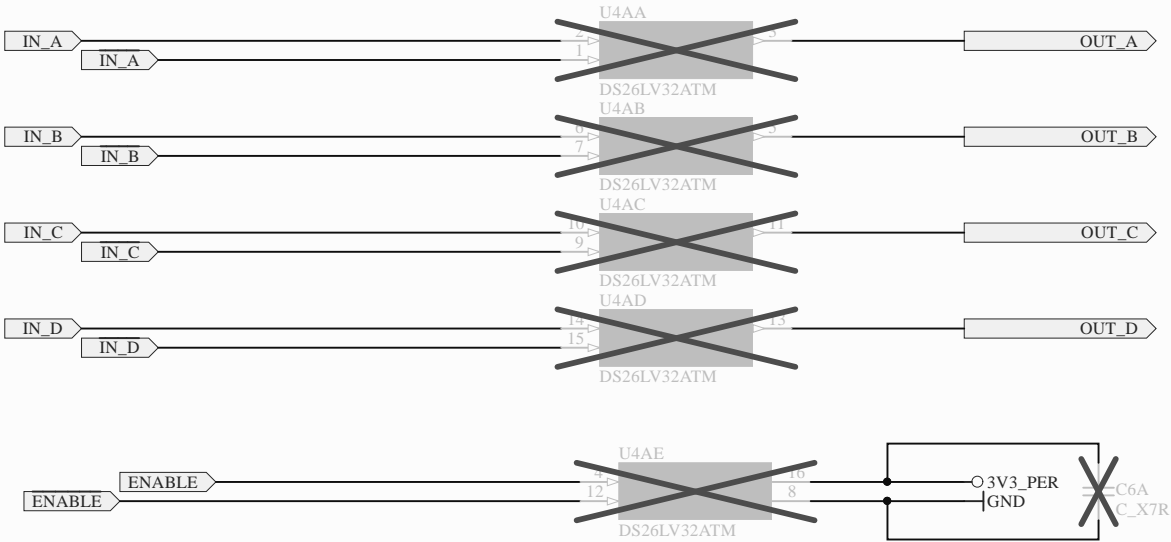
D

D

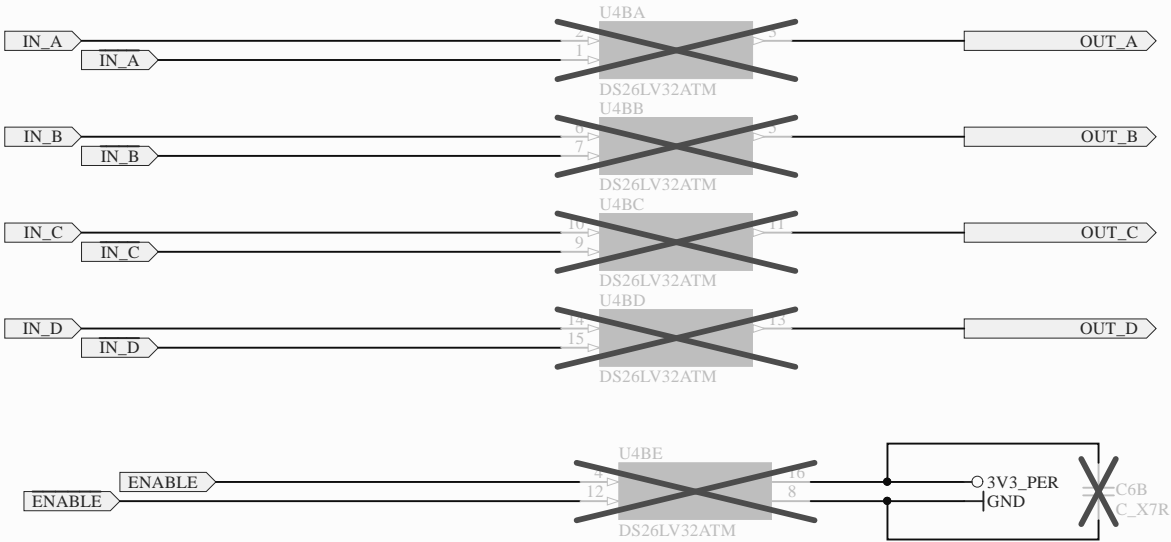


Application:  
VDD\_min = 3.0V  
VDD\_max = 3.6V

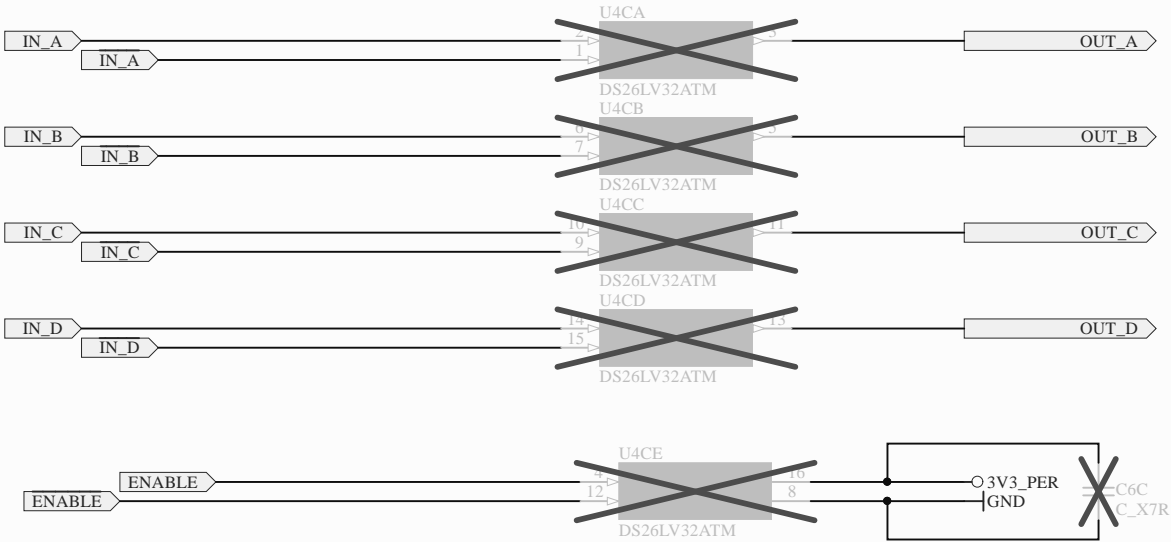
Title TI_DS26C32AT.SchDoc		<i>Technische Hochschule Nürnberg Georg Simon Ohm</i> Fürther Straße 250 90429 Nürnberg GERMANY		
Size: A4	Revision: 2v01			
Date: 03.08.2020	Time: 20:10:05	Sheet 9 of 16	Author: T. Wendt	
Project: ultrazohm_digital_voltage_3U_1vxx.PrjPCB				



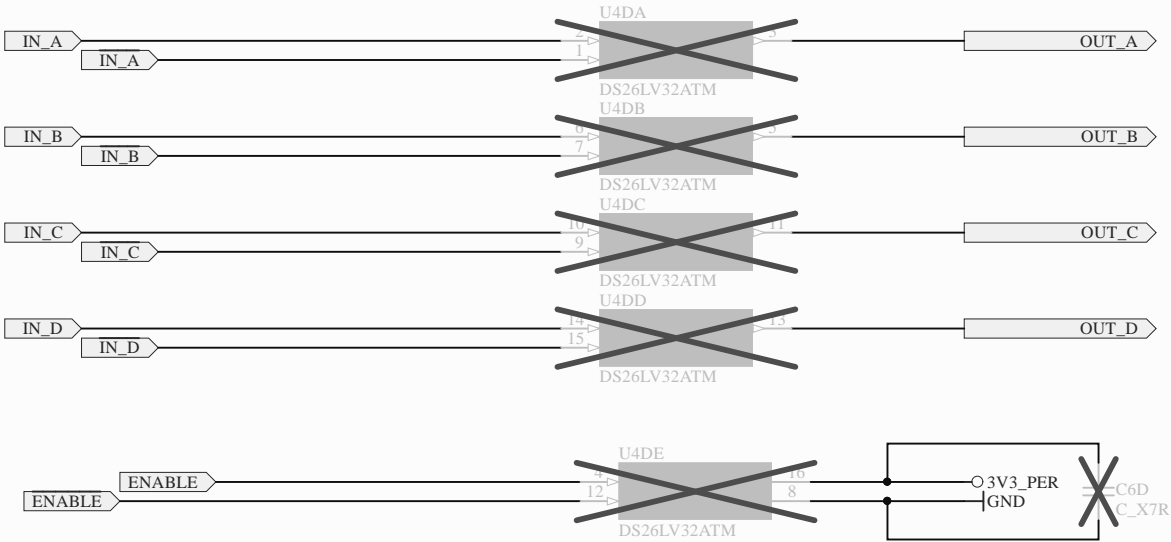
Application:  
VDD\_min = 3.0V  
VDD\_max = 3.6V



Application:  
VDD\_min = 3.0V  
VDD\_max = 3.6V

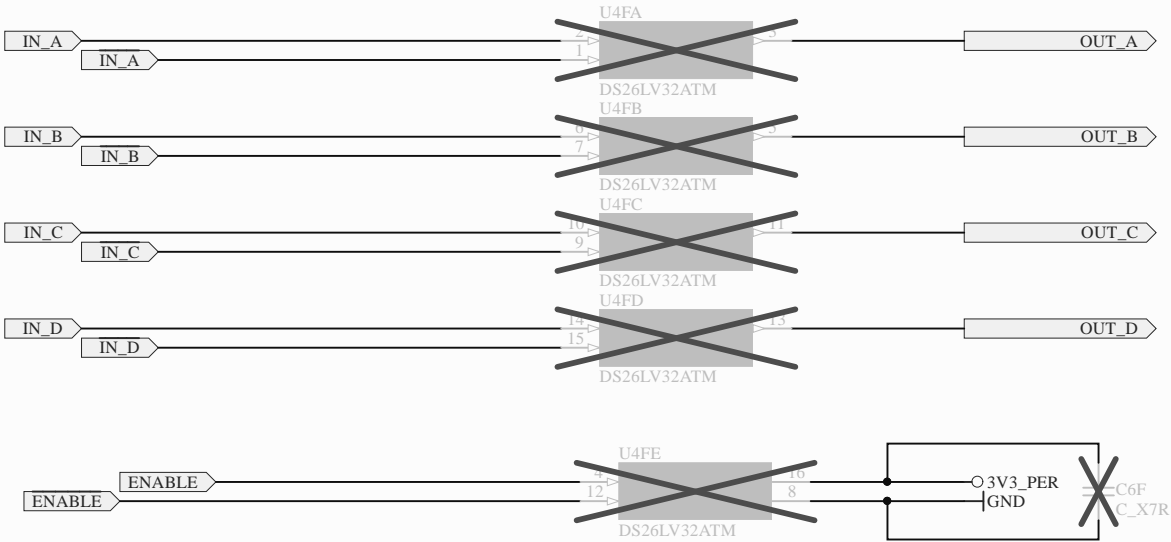


Application:  
VDD\_min = 3.0V  
VDD\_max = 3.6V

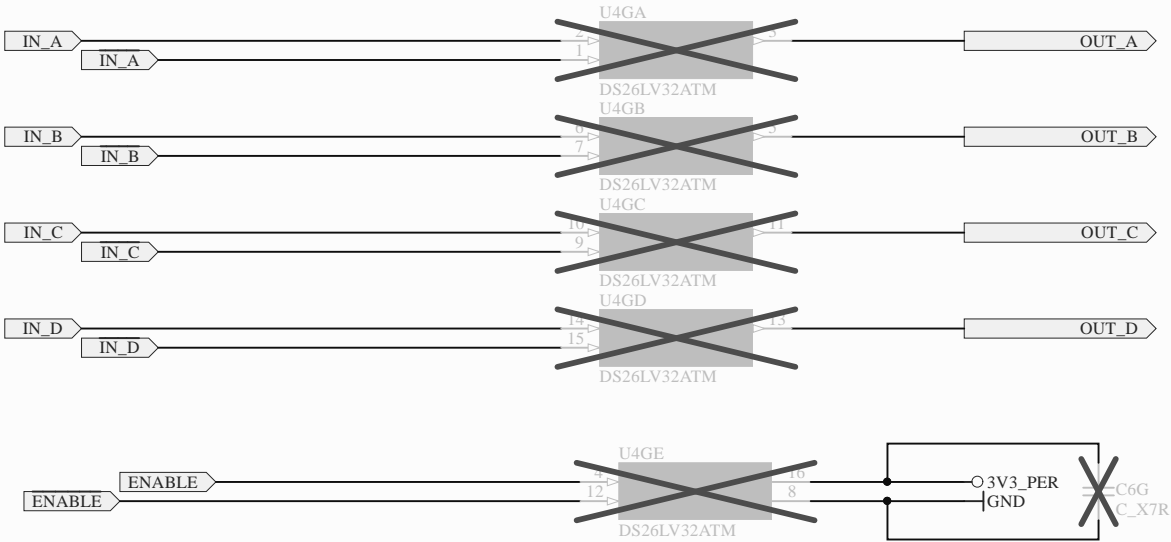


Application:  
VDD\_min = 3.0V  
VDD\_max = 3.6V

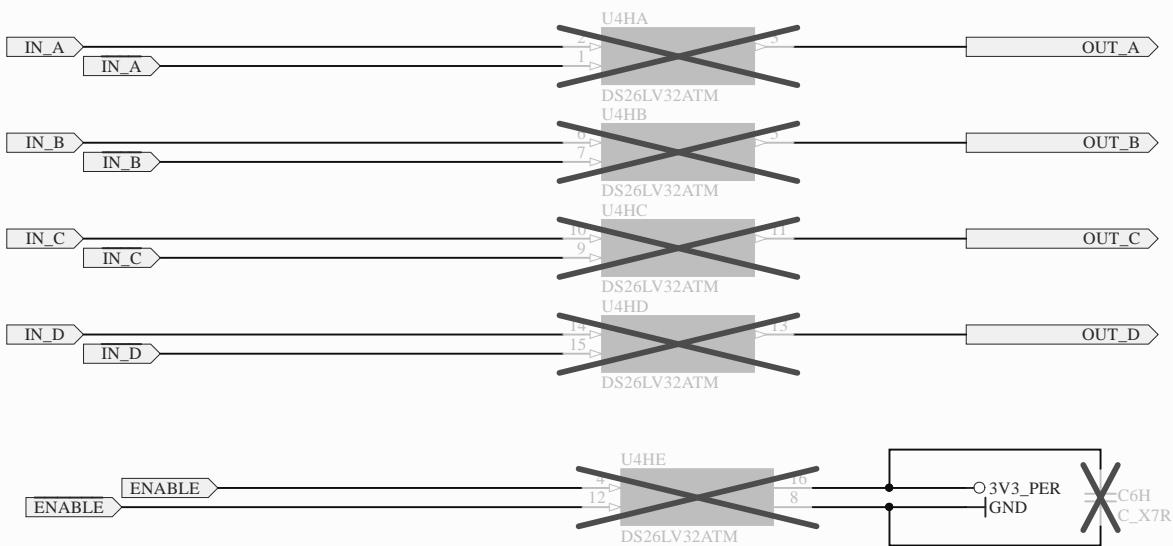




Application:  
VDD\_min = 3.0V  
VDD\_max = 3.6V



Application:  
VDD\_min = 3.0V  
VDD\_max = 3.6V



Application:  
VDD\_min = 3.0V  
VDD\_max = 3.6V

A

A

B

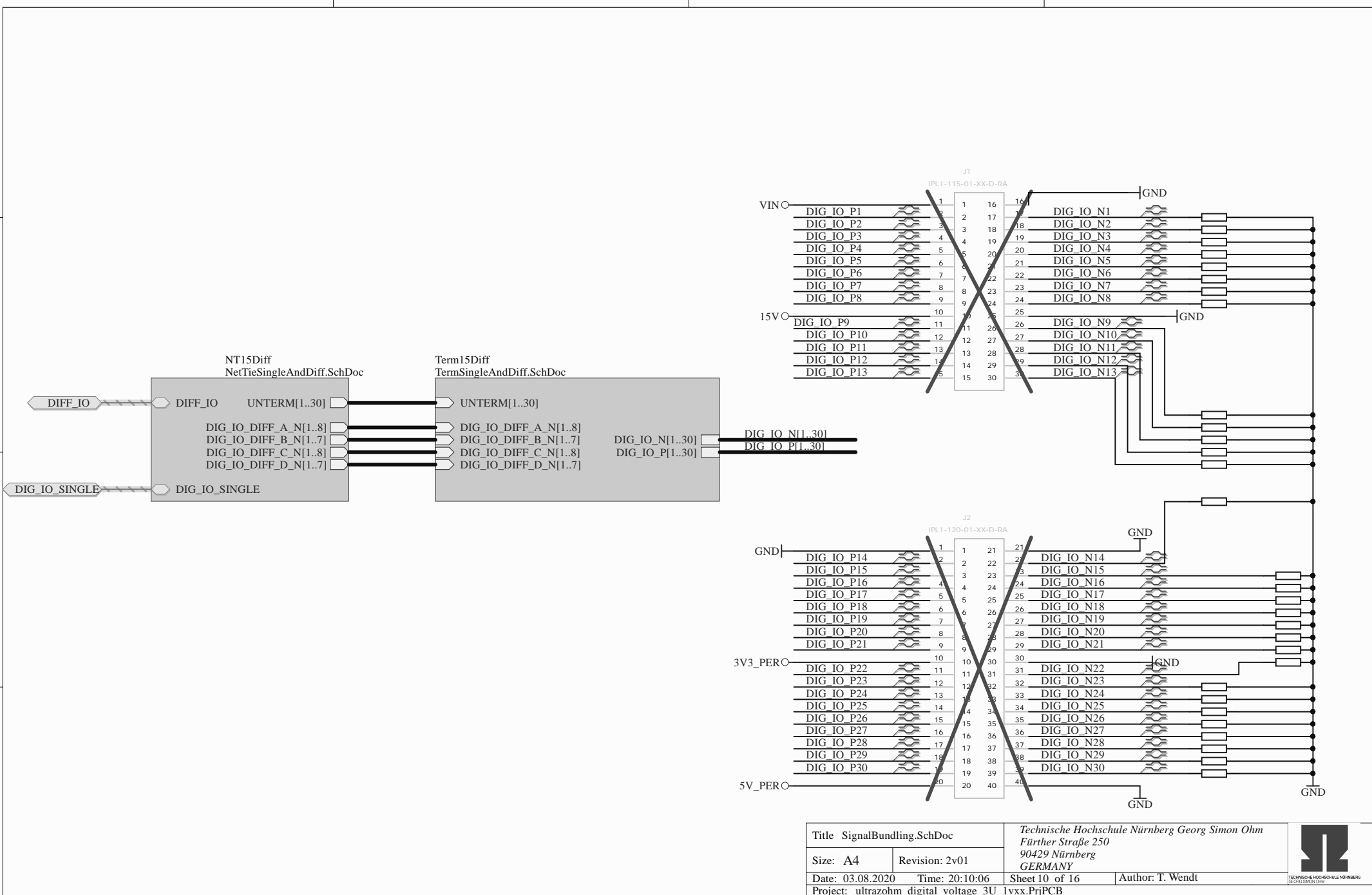
B

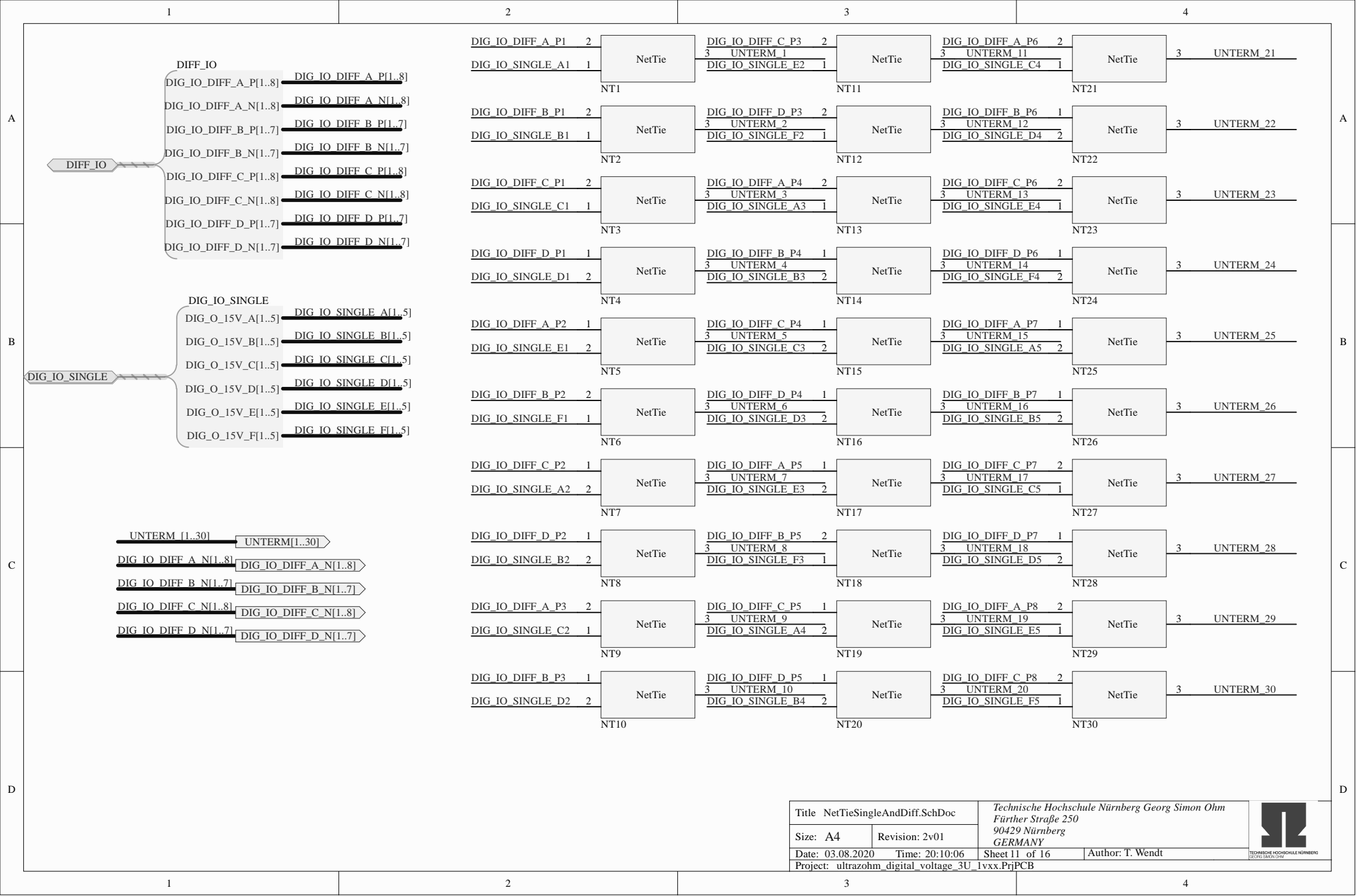
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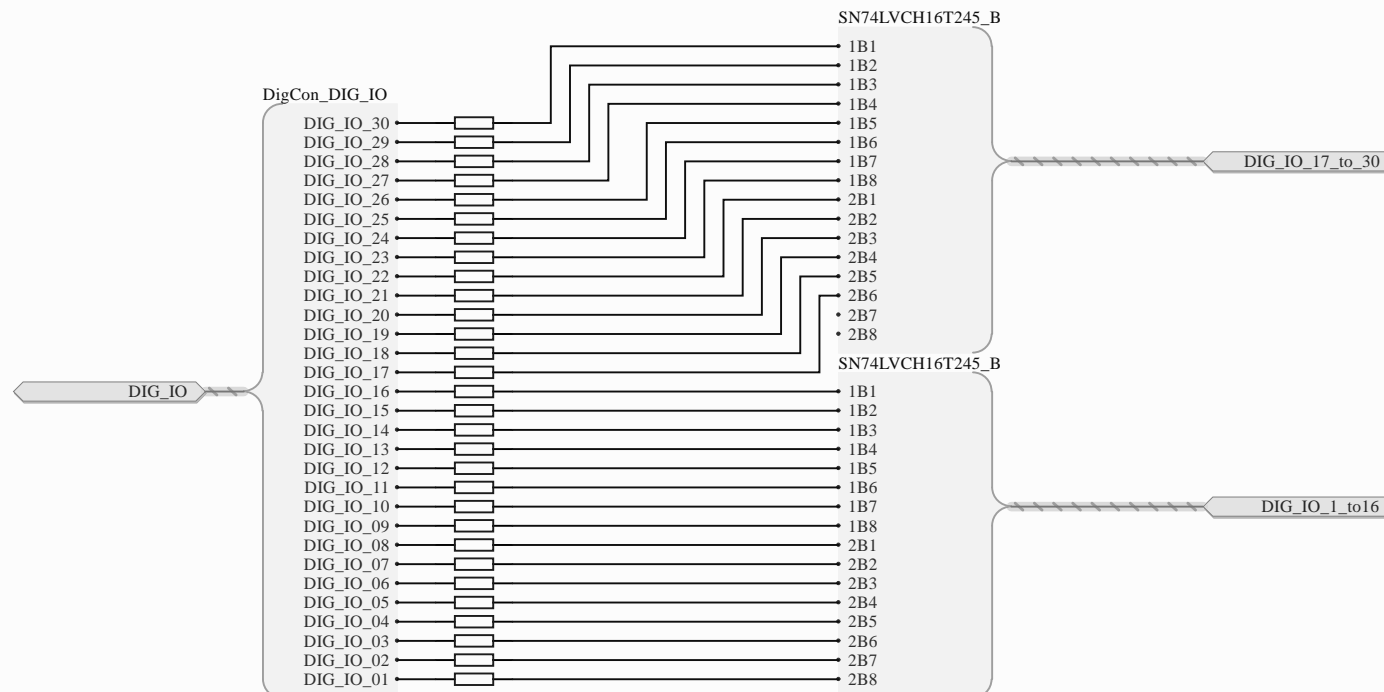
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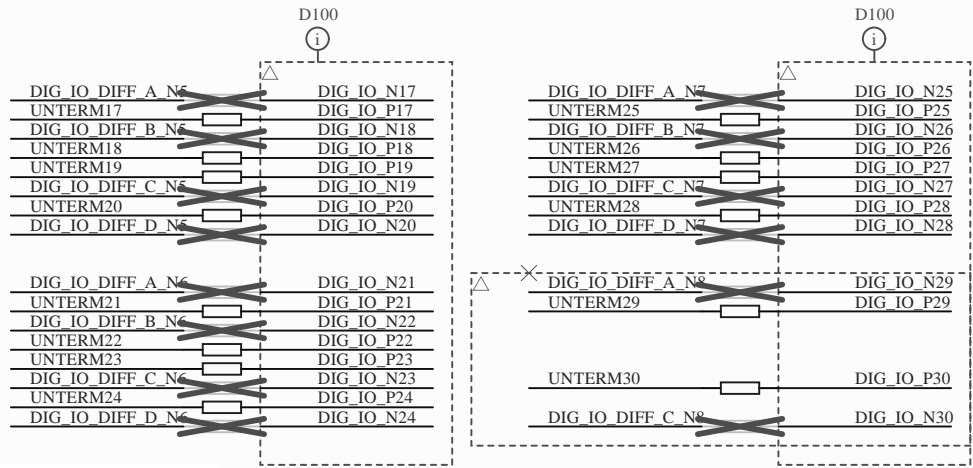
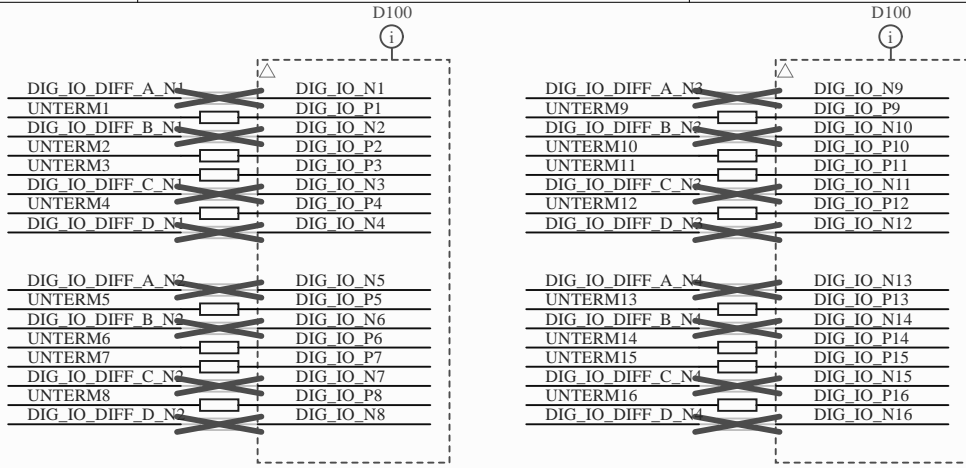
D

D



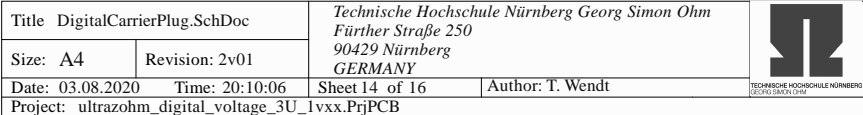






Note: The serial termination resistors are placed at the IO interface and not directly behind the level shifter from 3V3 to 5V, because 30 extra resistors would be required which implies additional assembly effort.

Note: If the board is configured as a receiver, the termination resistors can be replaced with jumpers.





A

B

C

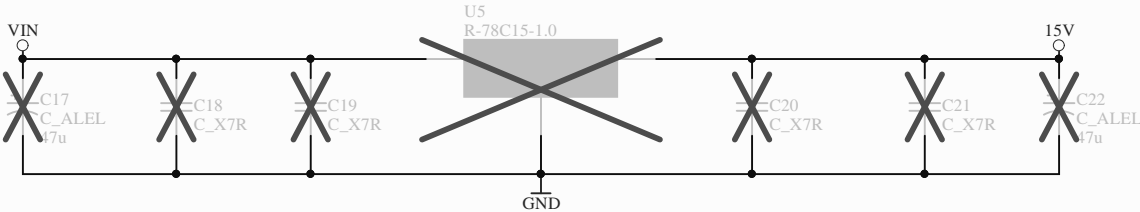
D

A

B

C

D

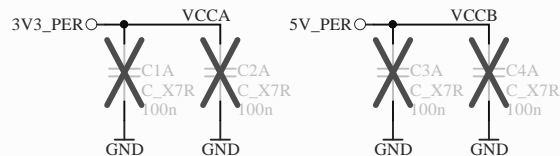
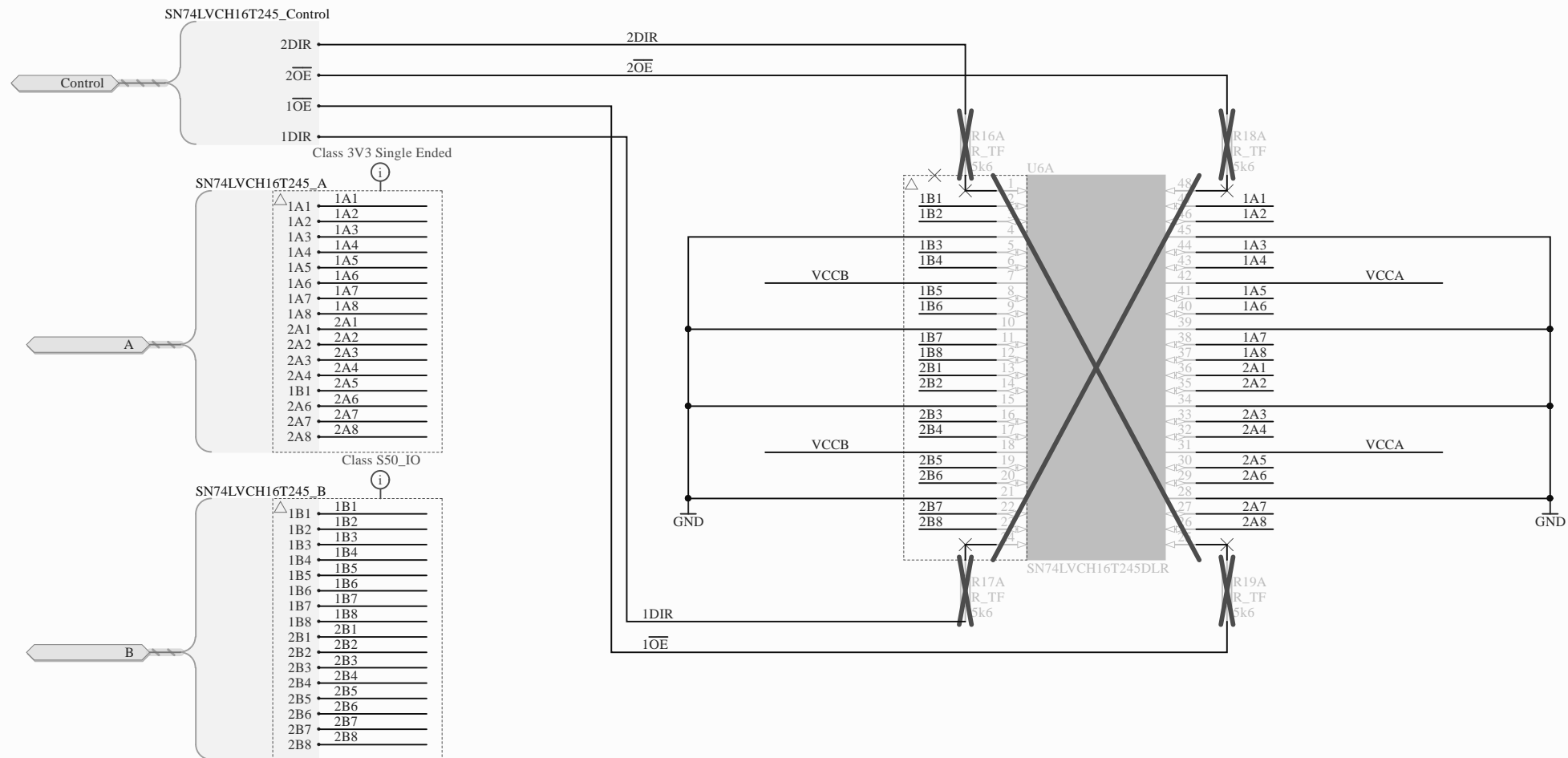


Totally integrated DCDC swichting converter.

Voltages:  
Vin\_max = 42V  
Vin\_min = 18V  
  
Vout = 15V

Current:  
Iout\_max = 1A

Parameters:  
VoutName = Name of the net of Vout  
VinName = Name of the net of Vin

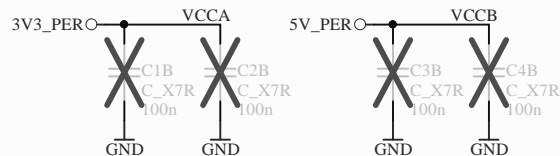
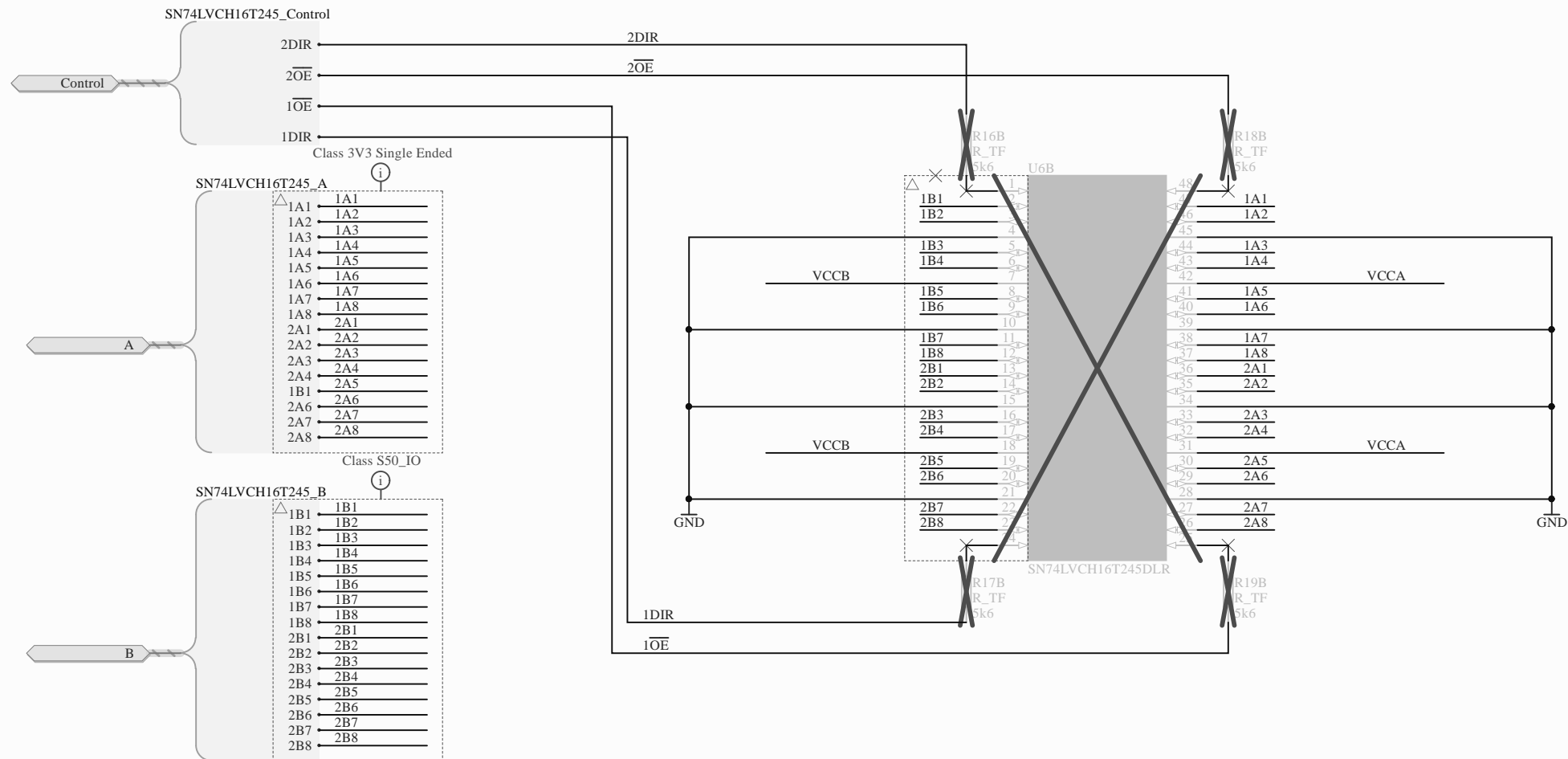


#### Application:

Voltages:  
 $V_{CCA\_min} = V_{CCB\_min} = 1.65V$   
 $V_{CCA\_max} = V_{CCB\_max} = 5.5V$

Note: Altium warns, that an IO pin (from the 5V LS) is connected to an output pin (from the RS422 transceivers). This does not matter because these parts are not assembled together. It can be suppressed.

Direction pins are driven trough the resistors



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