

A

A

B

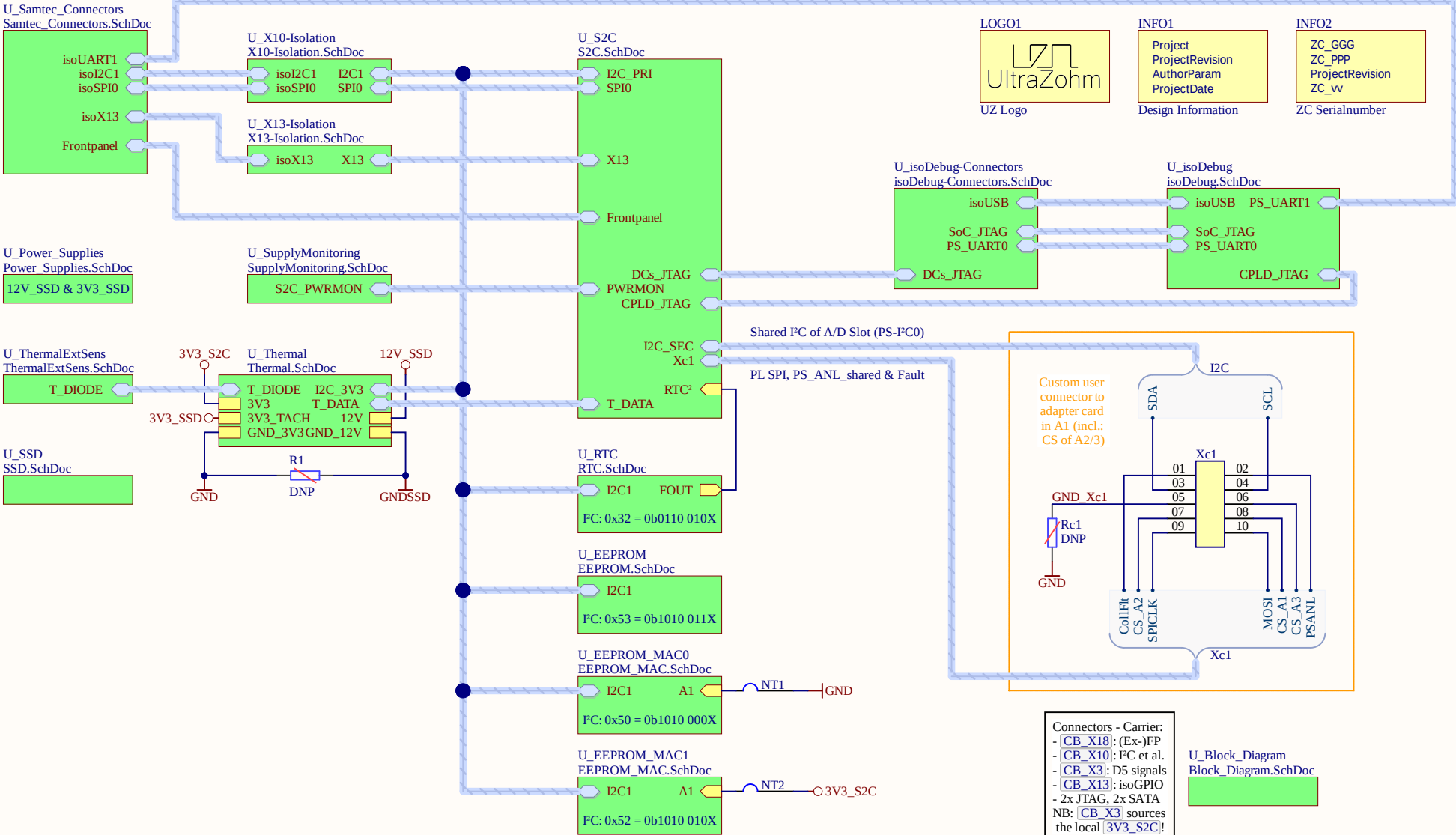
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C

C

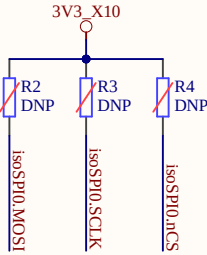
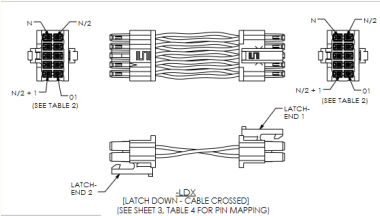
D

D

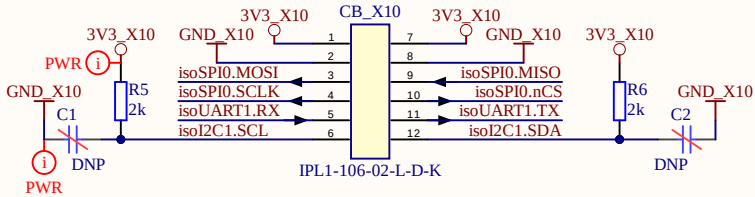


IPL1-106-01-L-D-RA-K
mmsd-06-30-f-04.00-d-k-ldx

Table 4- Pin Mapping		
End Option (Double)	END 1	END 2
-LUS	01	N/2
-LDS	01	N/2+1
-LUX	01	N
-LDX	01	01
-MUS	01	N/2
-MDS	01	N/2+1
-MUX	01	N
-MDX	01	01



From/to Carrierboard X10 (cf. CB's XMOD.SchDoc - 1:1 link)

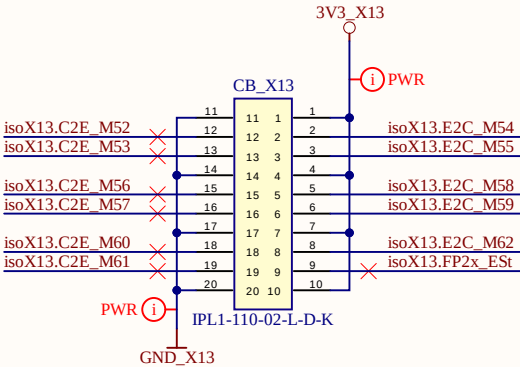


Level shifting on CB: TXS0108EQPWRQ1

← Notes on this:

On the CB, the PC lines have pull-up spots
On the CB's primary/1V8 side, this is fixed
This board links to the CB's secondary side
This board thus is able to add 3V3 pull-ups
No pull-ups needed on push/pull outputs(!)
Pull-ups on A ins (MISO/RX) may be req'd
Pull-up spots for B ins could be added here

X1 on Rev01: IPL1-106-01-X-D-RA-K

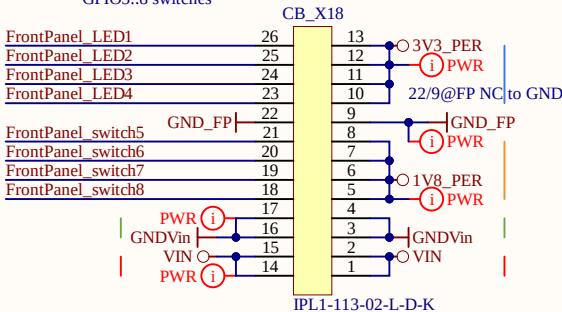


Aka: M(IO)31...



From/to CarrierBoard X18 (taken from FP's frontpanel.SchDoc)

GPIO1..4 leds
GPIO5..8 switches

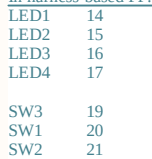


Regular wiring: Cable from CB connected here...

From/to Front Panel (taken from CB's FrontPanel.SchDoc)

GPIO1..4 leds
GPIO5..8 switches

In harness-based FP:



All other pins are NC :-)

In harness-based FP:

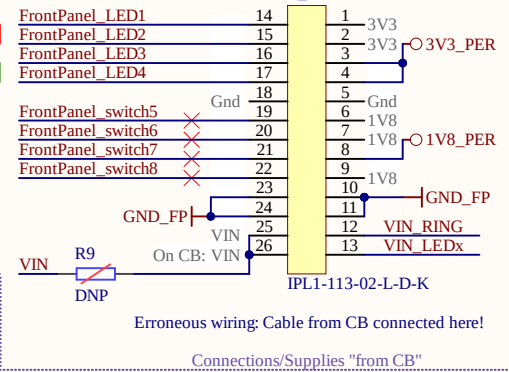
All other pins are NC :-)

08: SWx com. (1V8)

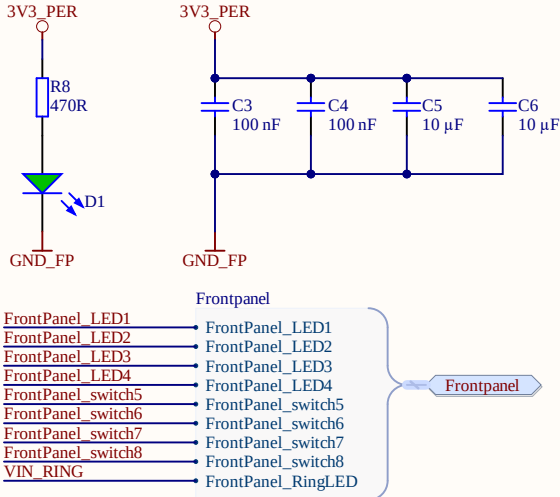
10: SW3 LED GND

12: SW3 LED 24V

13: LEDx com. (24V)

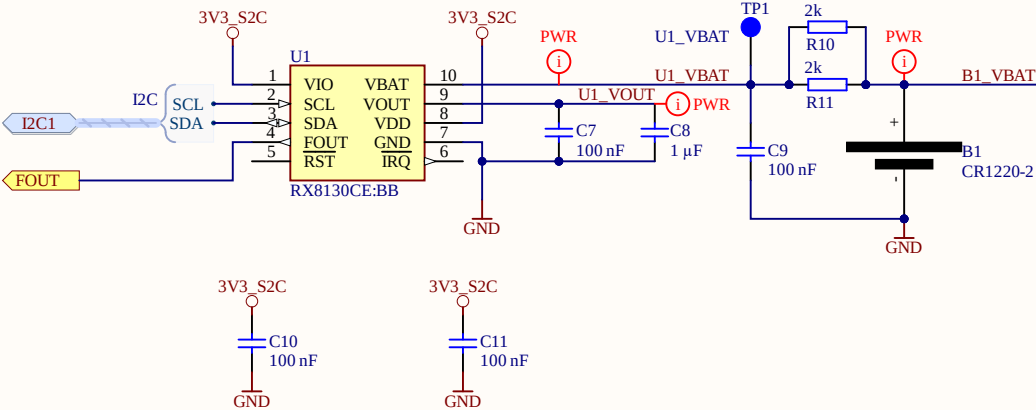


Note to installer:
- v4a (harness): 0R
- v4b (zBoard): DNP



NB: Connector CB_X3 (cf. S2C_IOS1V8) also has to be linked to carrier at all times!

PC address: 0x32 = 0b0110 010X



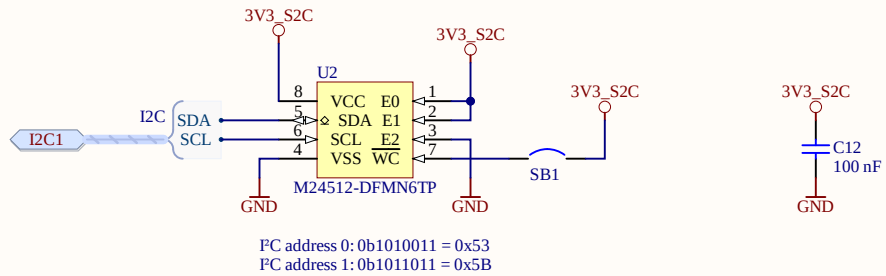
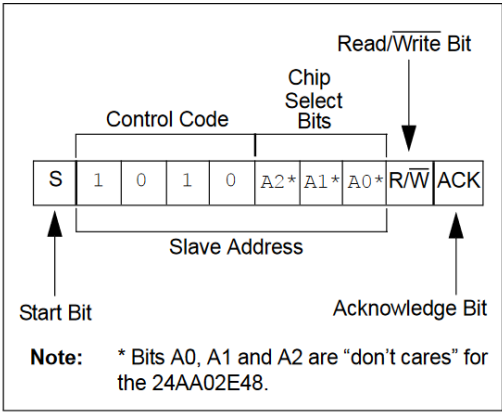


FIGURE 5-1: CONTROL BYTE ALLOCATION



I2C-bus slave address: 0xAz = 0b1010 zzzX

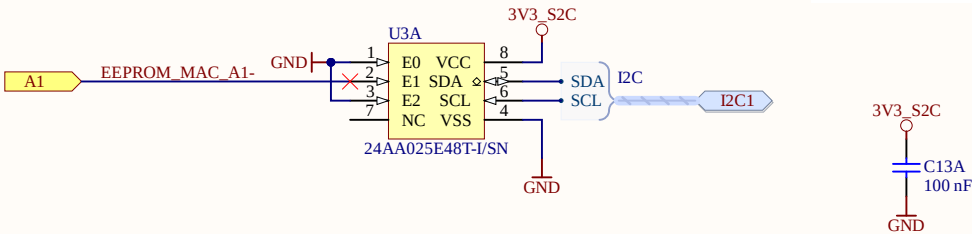
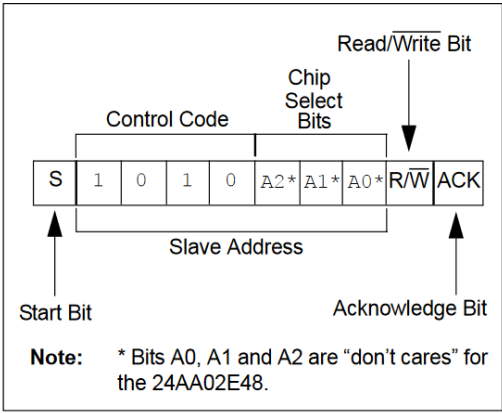
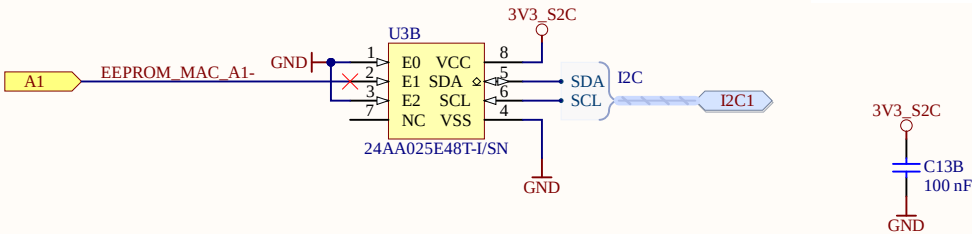


FIGURE 5-1: CONTROL BYTE ALLOCATION



I2C-bus slave address: 0xAz = 0b1010 zzzX



UZ(C/Ext.) Rev04/02 UZ(C/Ext.) Rev04/03

GTR0: SATA 2280 GTR0: SATA 2242
GTR1: SATA 2242 GTR1: SATA 2280
GTR2: SGMII
GTR3: N/A

NB: GTR0 (@X17A) is the non-crossed one

X17B @ CB

CB_X17

GTR1_RX_P SA2
GTR1_RX_N SA3

GTR1_TX_N SA5
GTR1_TX_P SA6

SA1
SA4
SA7

GND
GND
GND

A+
A-
B-
B+

A+
A-
B-
B+

TX
TX
RX
RX

A+
A-
B-
B+

GND
GND
GND

GND
GND
GND

MH1
MH2

GND
GND
GND

SB2
SB3

GTR0_TX_P
GTR0_TX_N

SB5
SB6

GTR0_RX_N
GTR0_RX_P

SB1
SB4
SB7

NB: "CB un-crossing" directly at connector above
Mechanical: Pin 7 at notch (i.e., the L's short side)

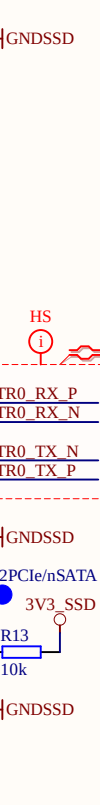
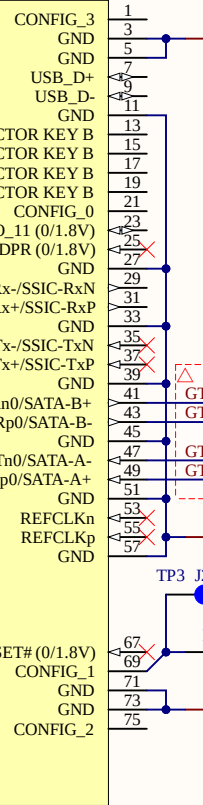
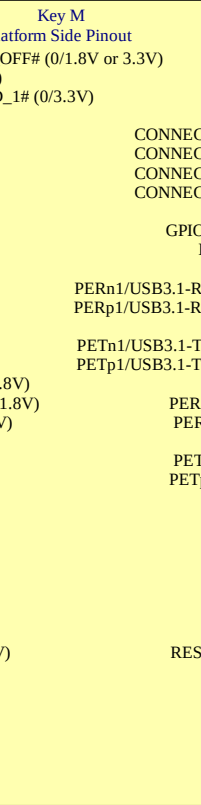
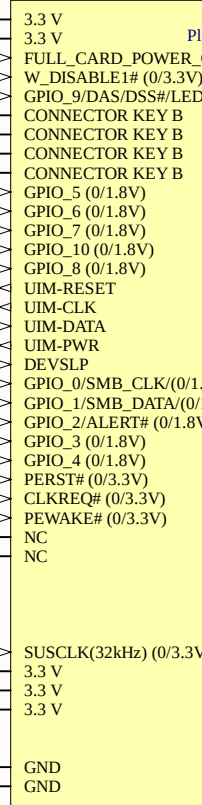
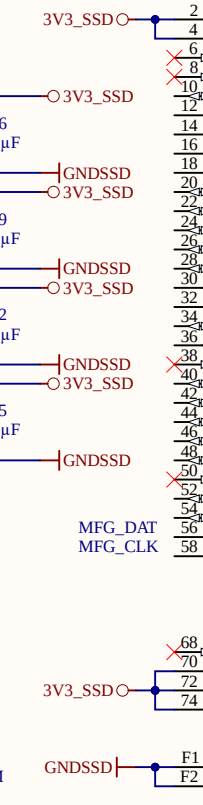
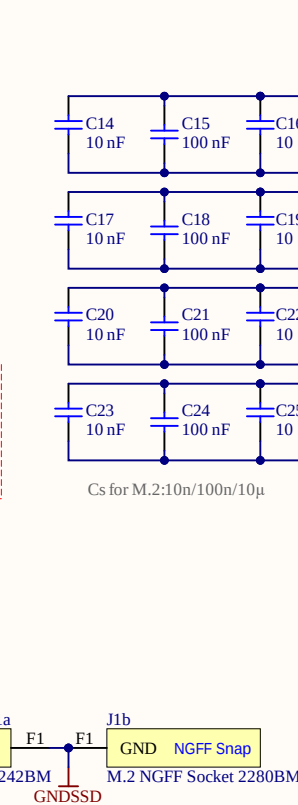
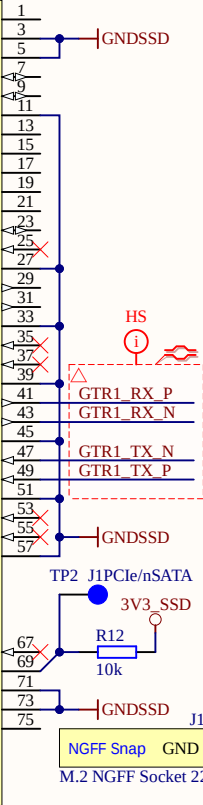
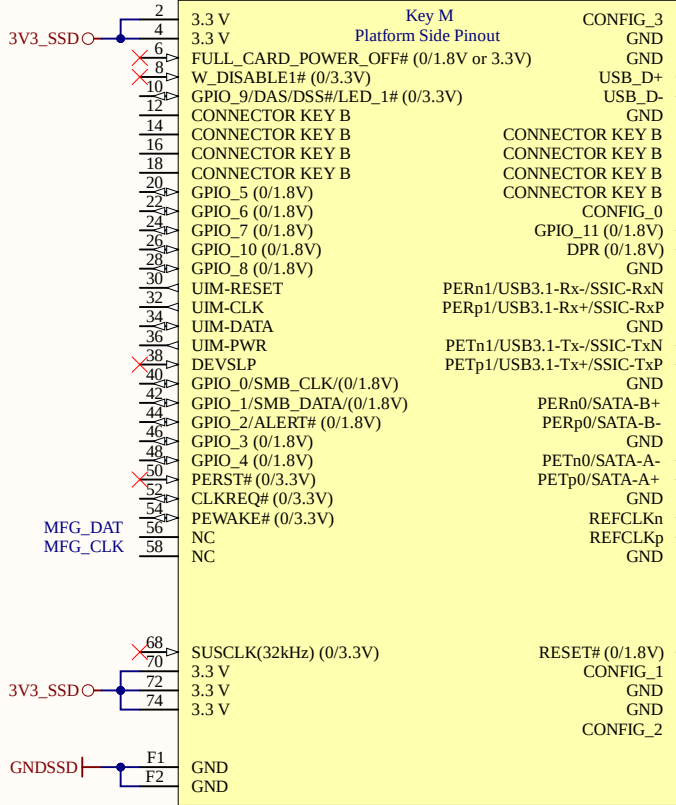
X17A @ CB

UZ(C) Rev05 (w/ FP)

GTR0: M.2 !SATA
GTR1: SATA 2280
GTR2: SGMII
GTR3: NC

Valid for FP Rev01/2

J1 1-2199230-5



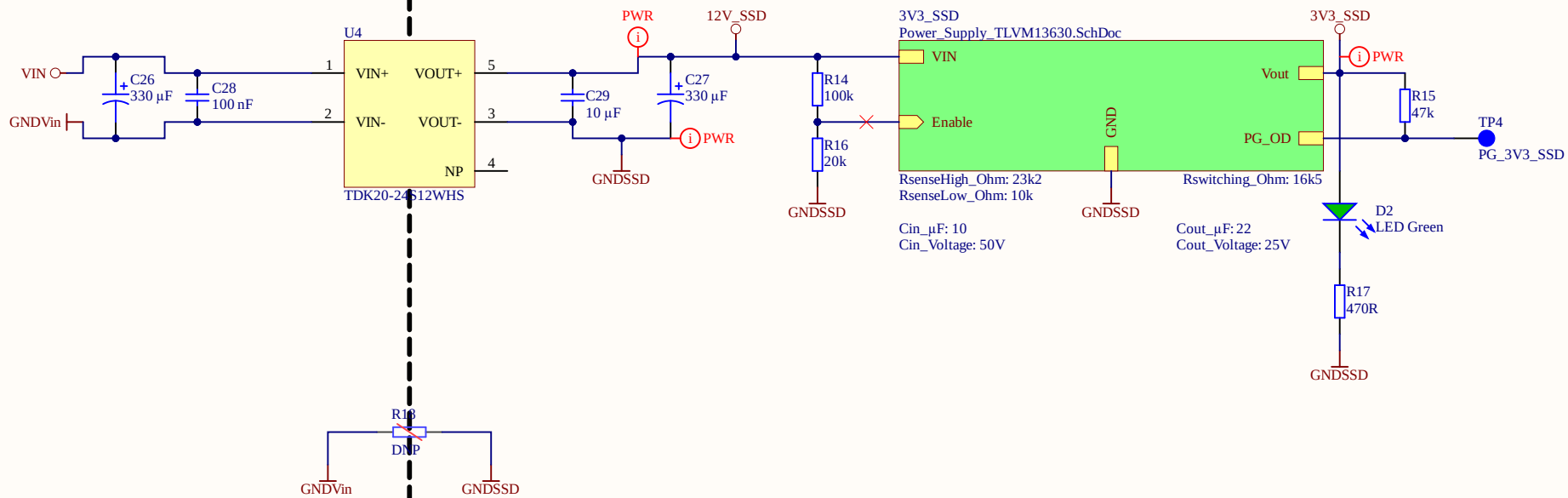
MECH1a
SMTSOM325BTR

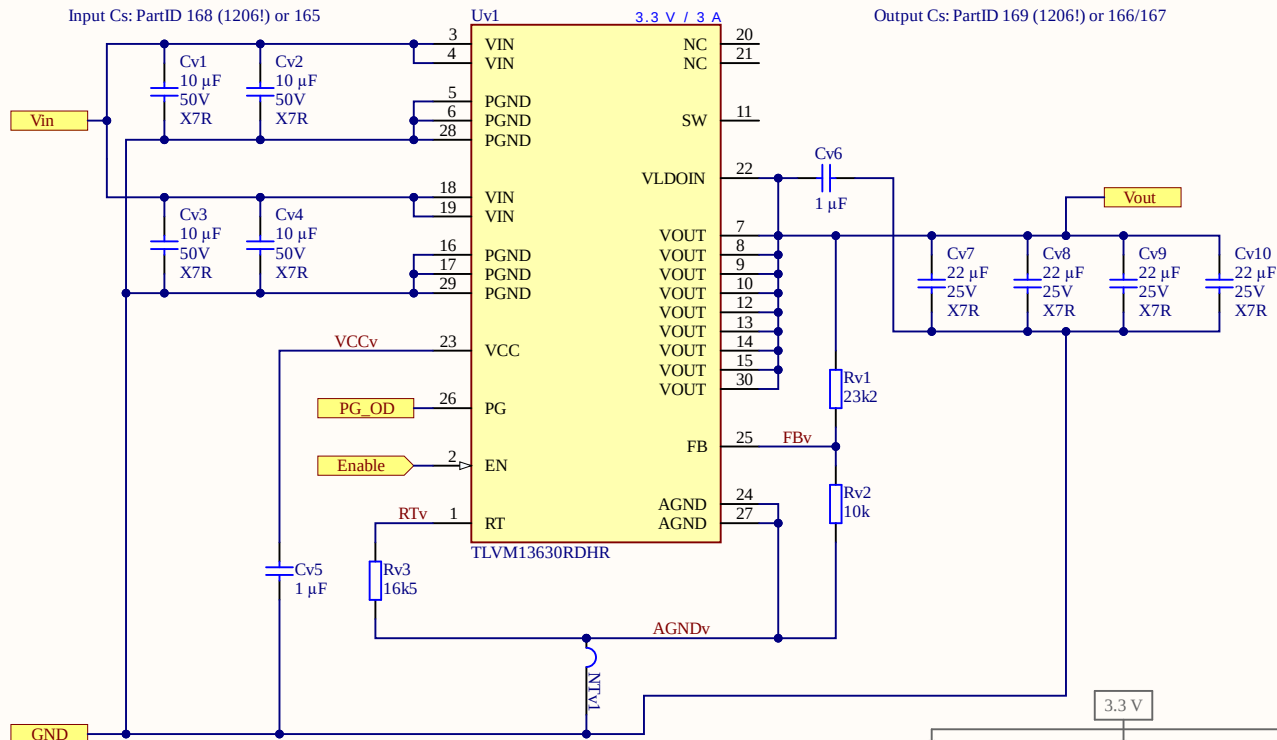
MECH1b
SMTSOM325BTR

MECH2a
SMTSOM325BTR

Title SSD.SchDoc	
Revision: 03	Design Engineer: E. Aufderheide, M. Geier
Project: UZ_per_cb_upgrade.PriPcb	

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Date: 31/07/2025	
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RsenseHigh (Rv1) Value (Ohm)	23k2
RsenseLow (Rv2) Value (Ohm)	10k
Rswitching (Rv3) Value (Ohm)	16k5

NB: No need to set MPN as parameter!

A

B

C

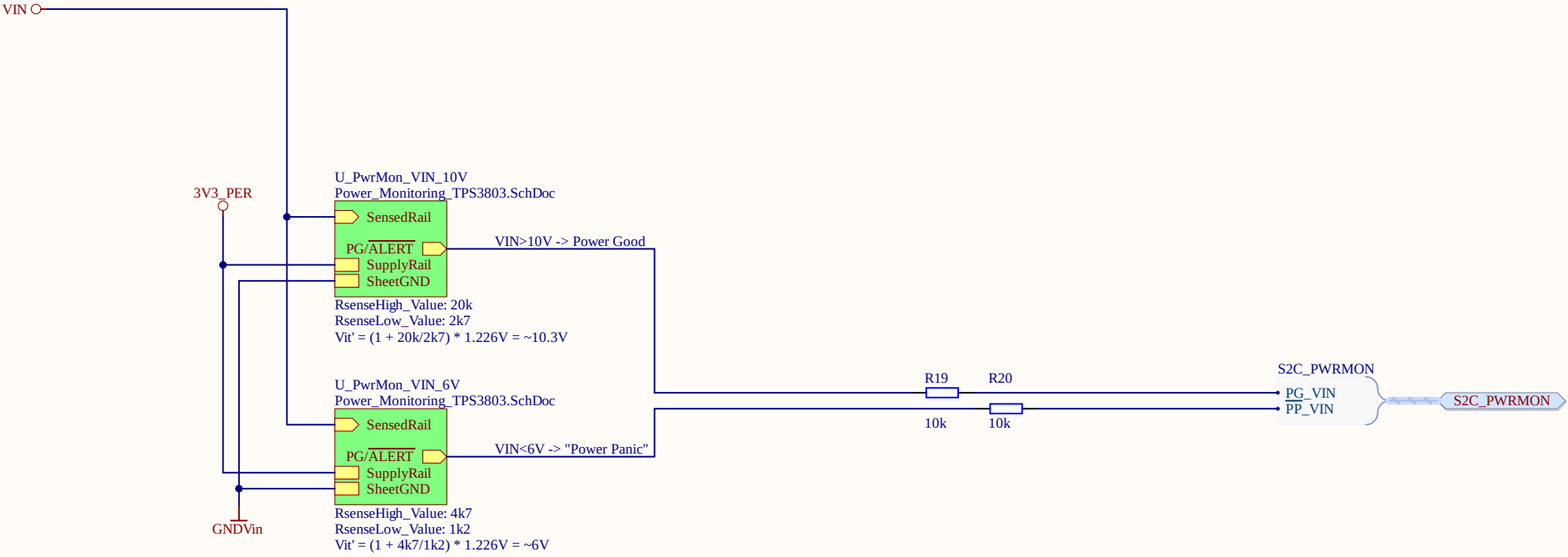
D

A

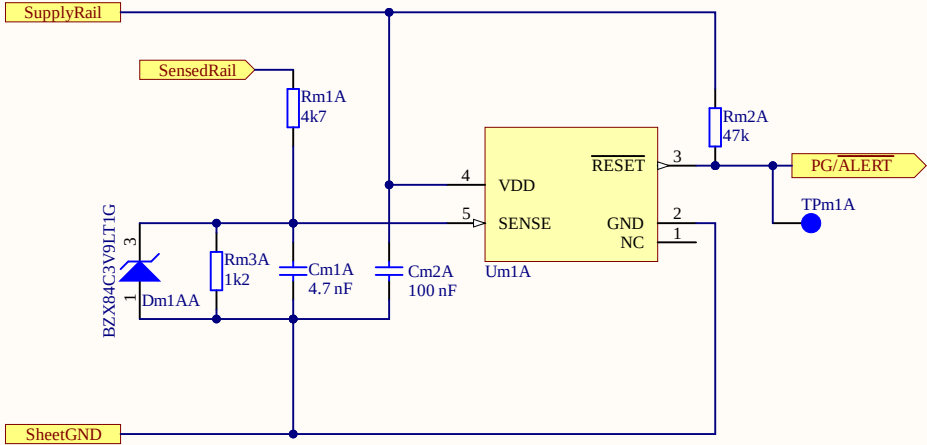
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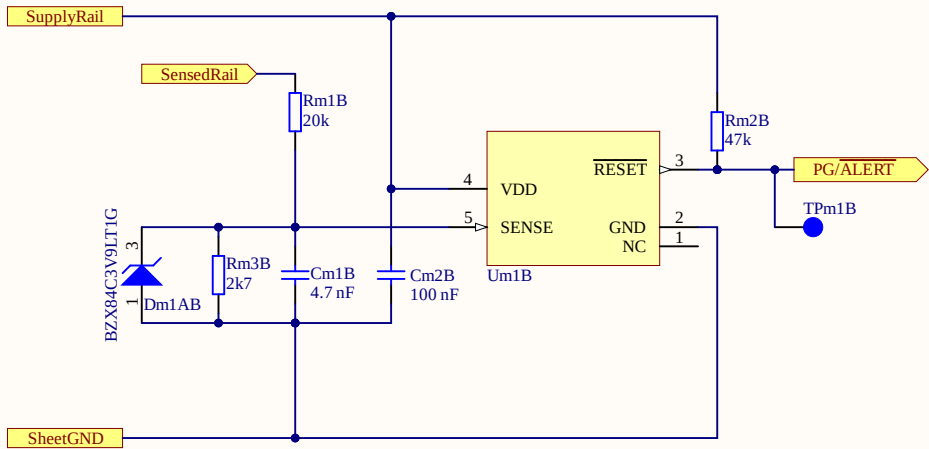
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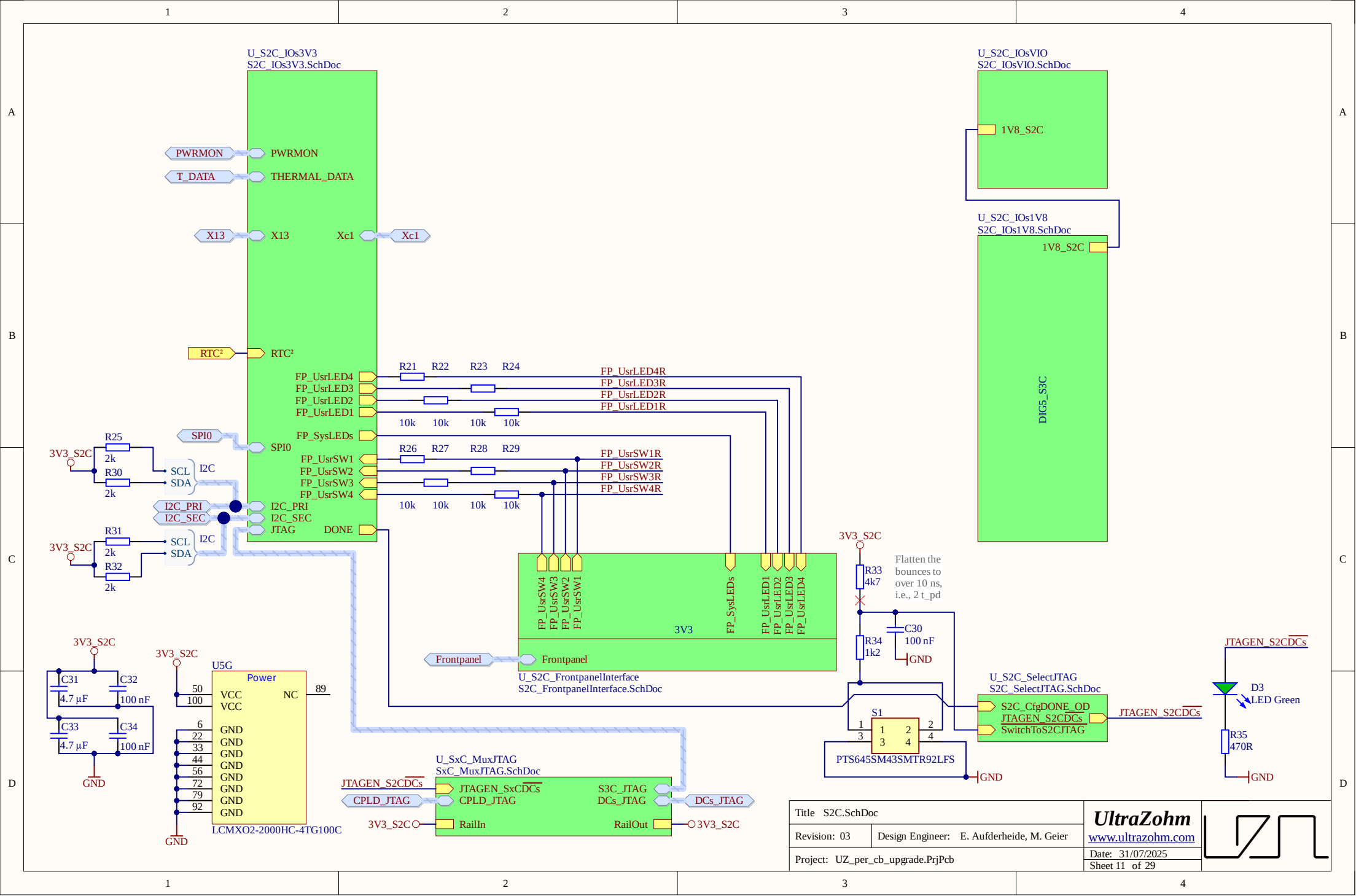
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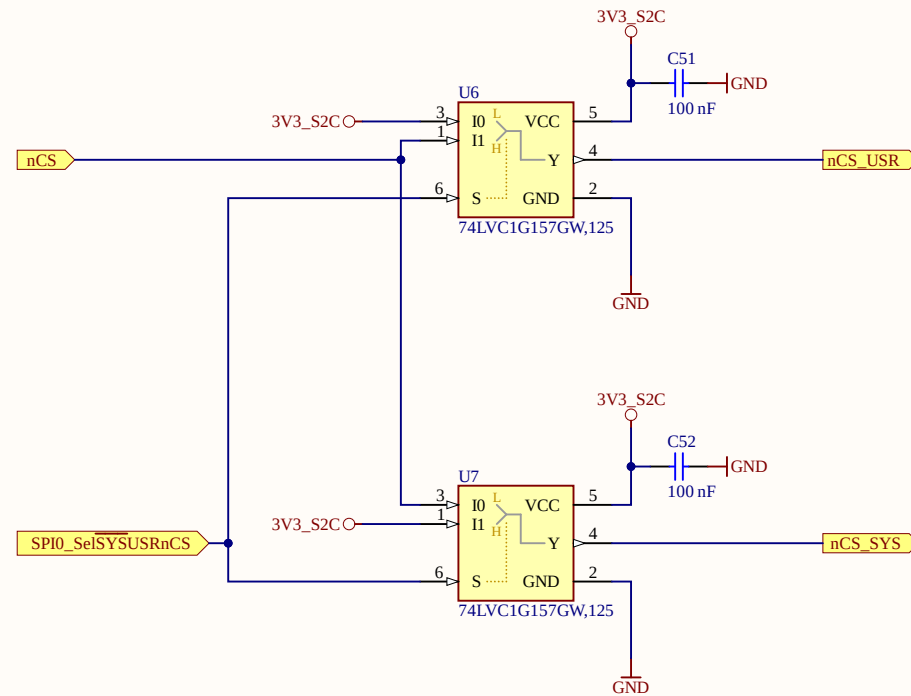


NB: GDC from 3V3_PER (via ICs & RCs) to GNDVin such that the sense rail is correct









Title S2C_IOs3V3_SelectSPI.SchDoc

Revision: 03

Design Engineer: E. Aufderheide, M. Geier

Project: UZ_per_cb_upgrade.PrfPcb

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Date: 31/07/2025

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A

A

B

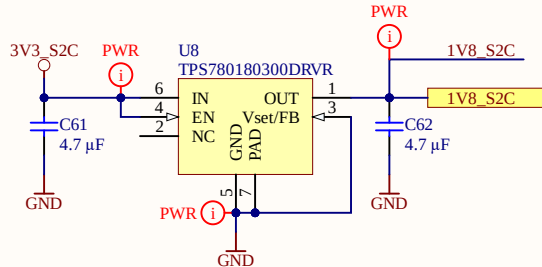
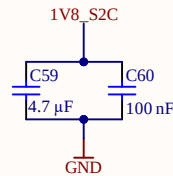
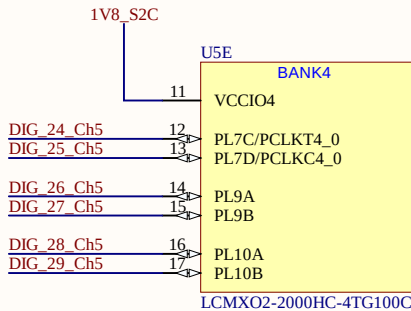
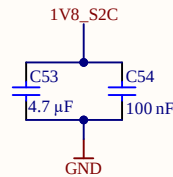
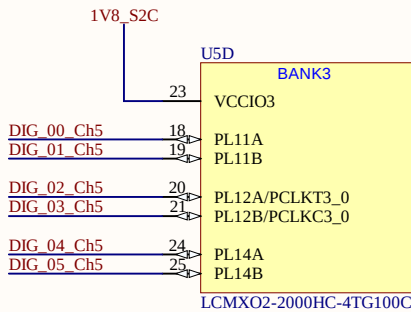
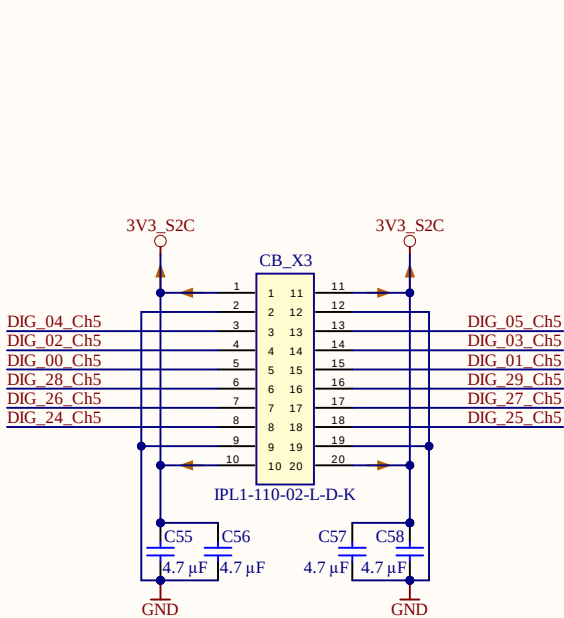
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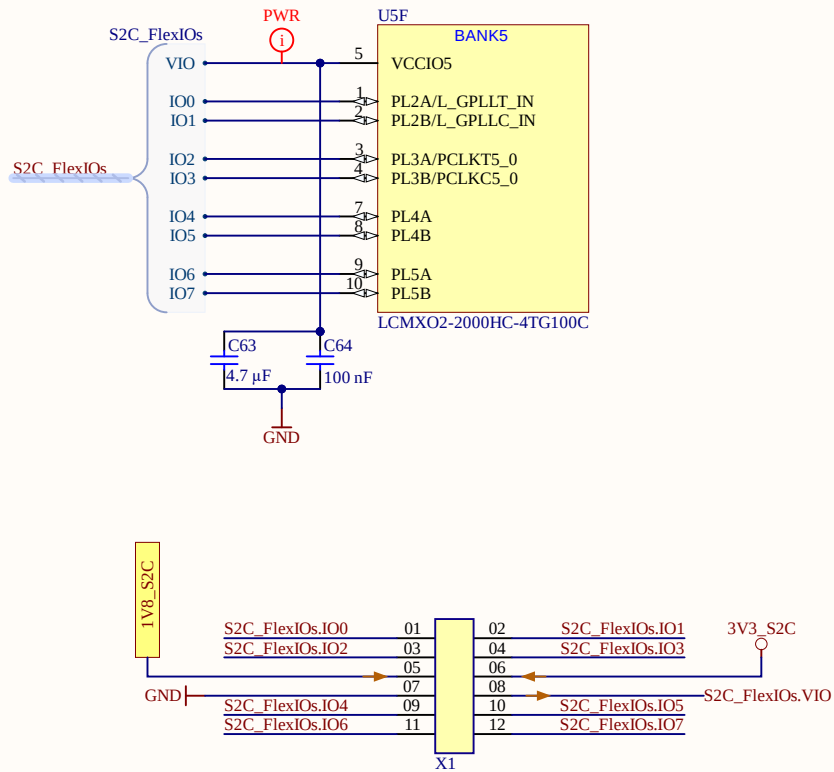
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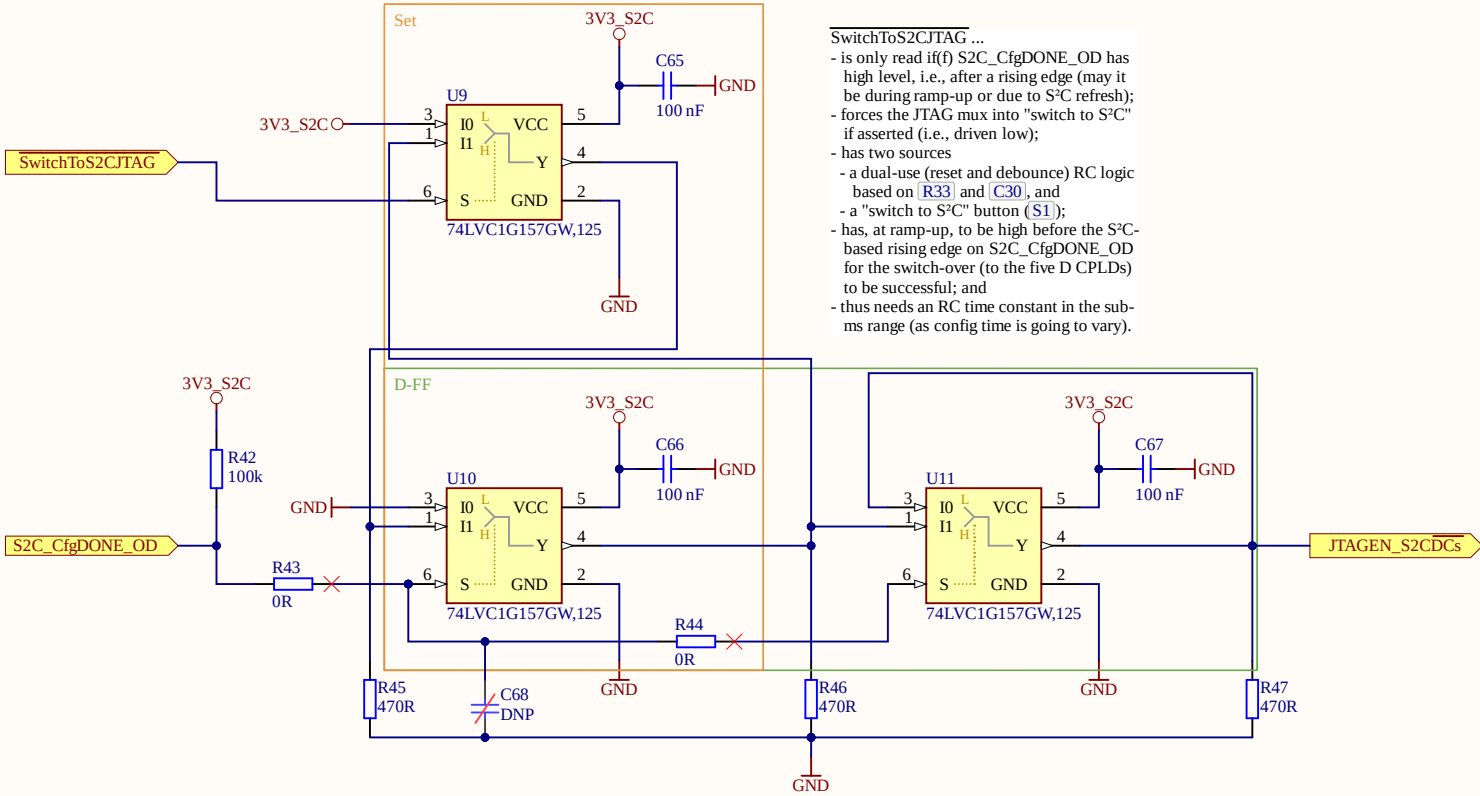
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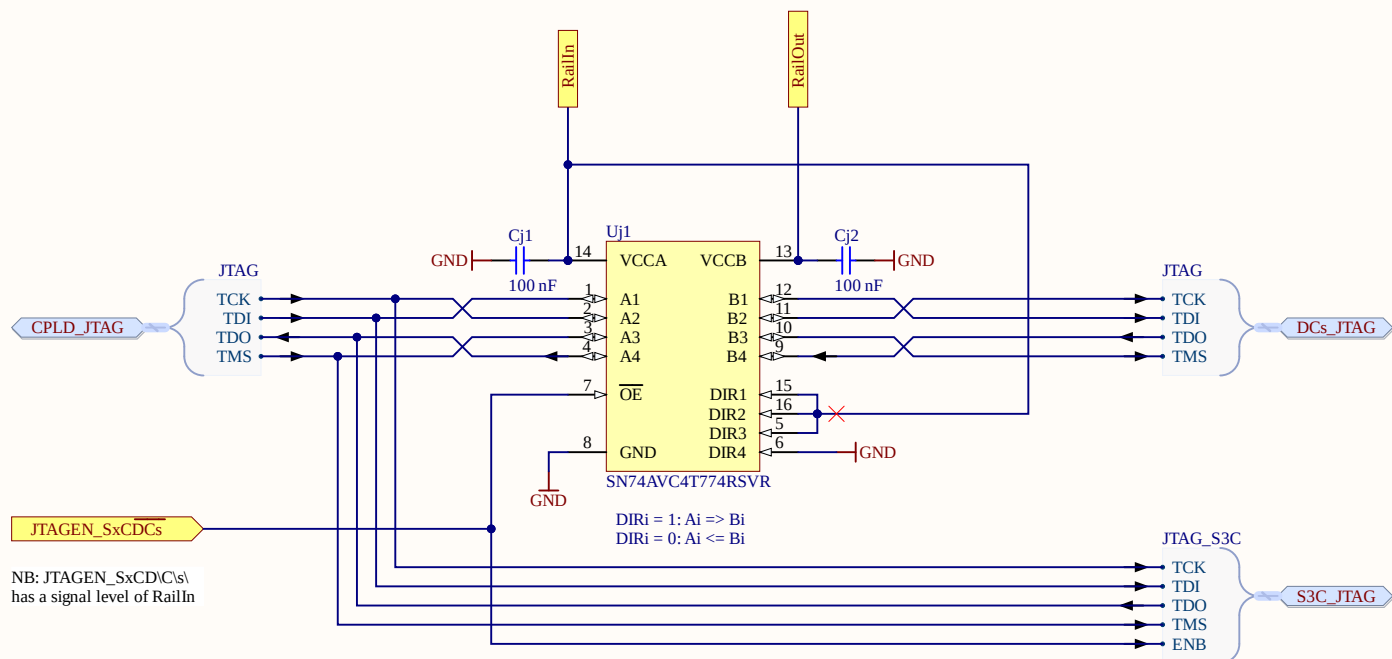
D

D









Title SxC_MuxJTAG.SchDoc

Revision: 03

Design Engineer: E. Aufderheide, M. Geier

Project: UZ_per_cb_upgrade.PrjPcb

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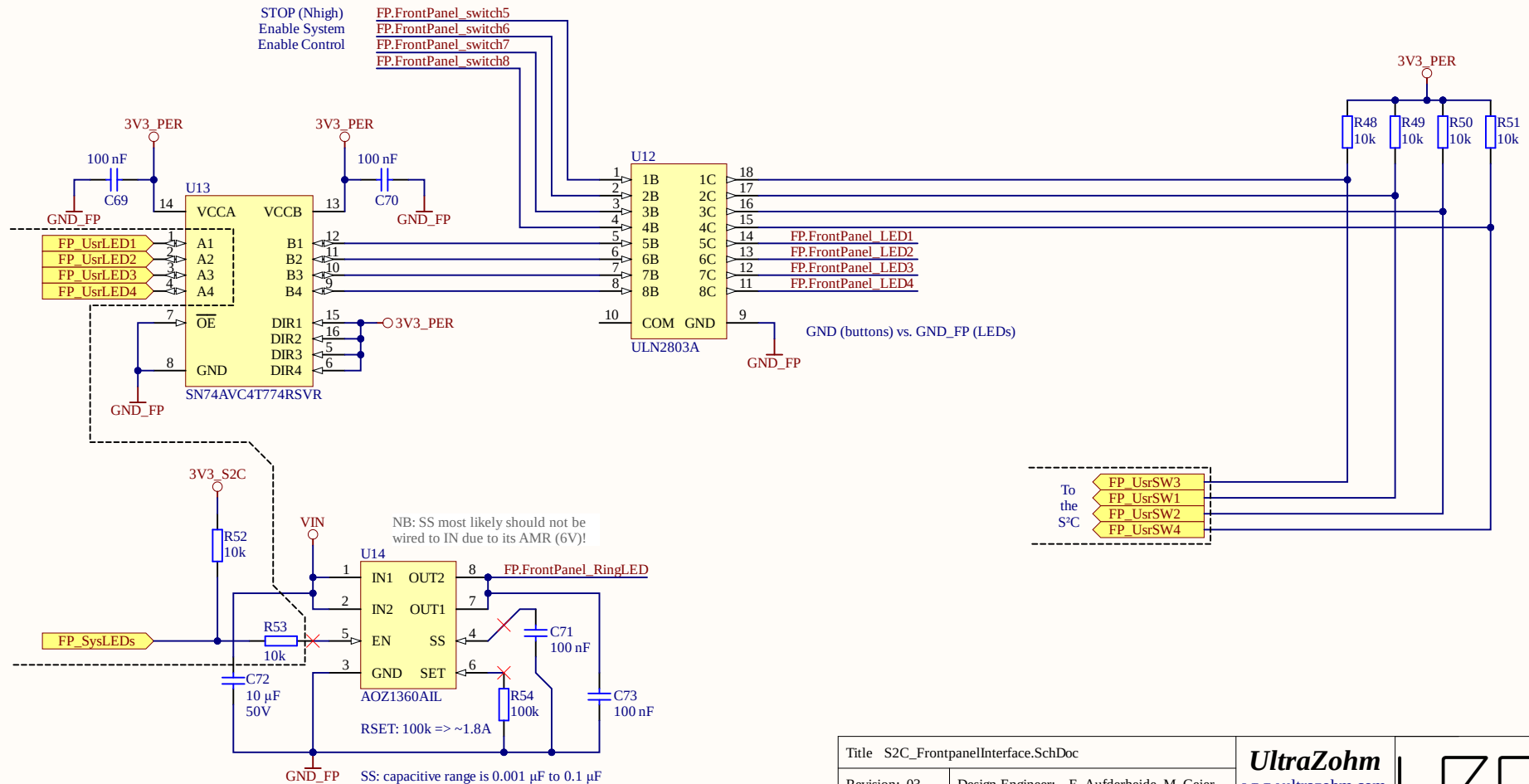
Date: 31/07/2025

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LED[1-4]:
- "a": From 24V to GND
- "b": From 3V3 to GND

Frontpanel FP
switch[5-8]:
- "a": To 1V8
- "b": Same
RingLED: To 24V



Title S2C_FrontpanelInterface.SchDoc

Revision: 03

Design Engineer: E. Aufderheide, M. Geier

Project: UZ_per_cb_upgrade.PrjPcb

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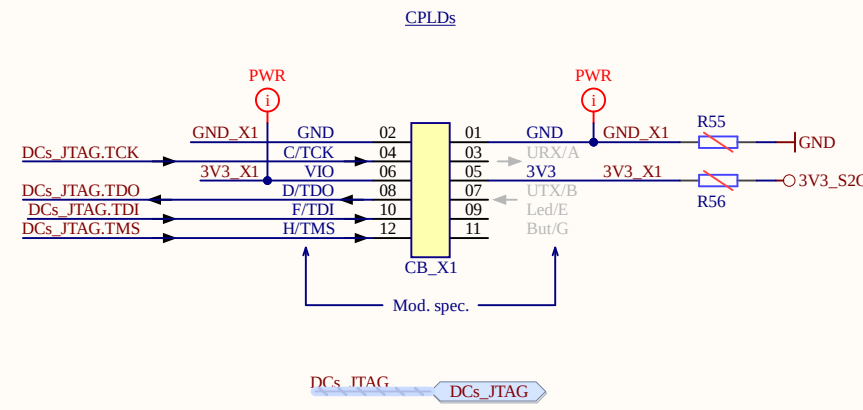
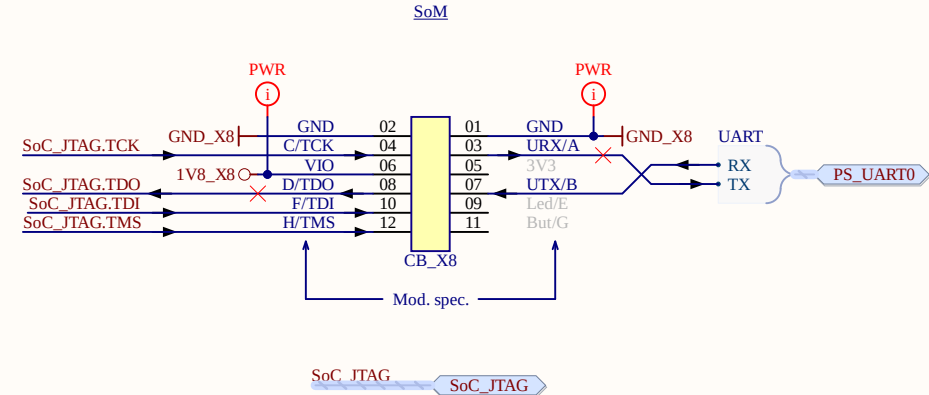
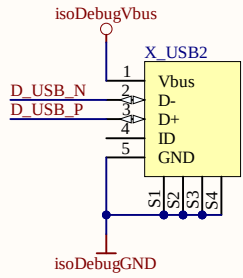
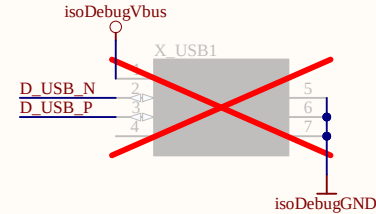
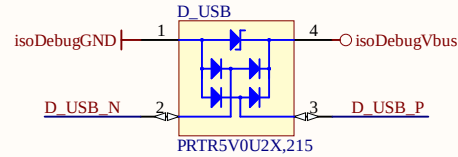
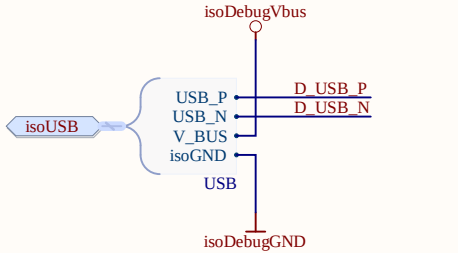
Date: 31/07/2025

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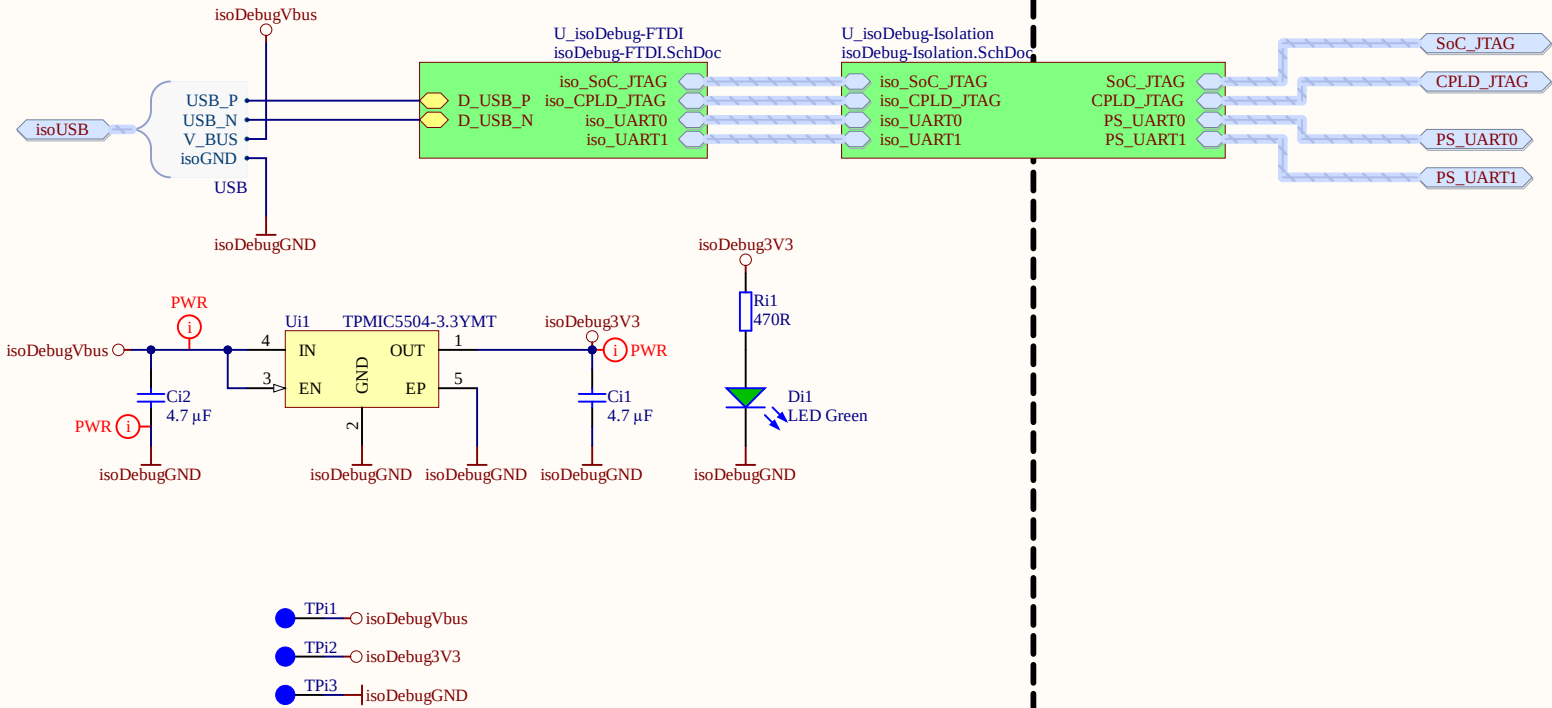
Isolated side

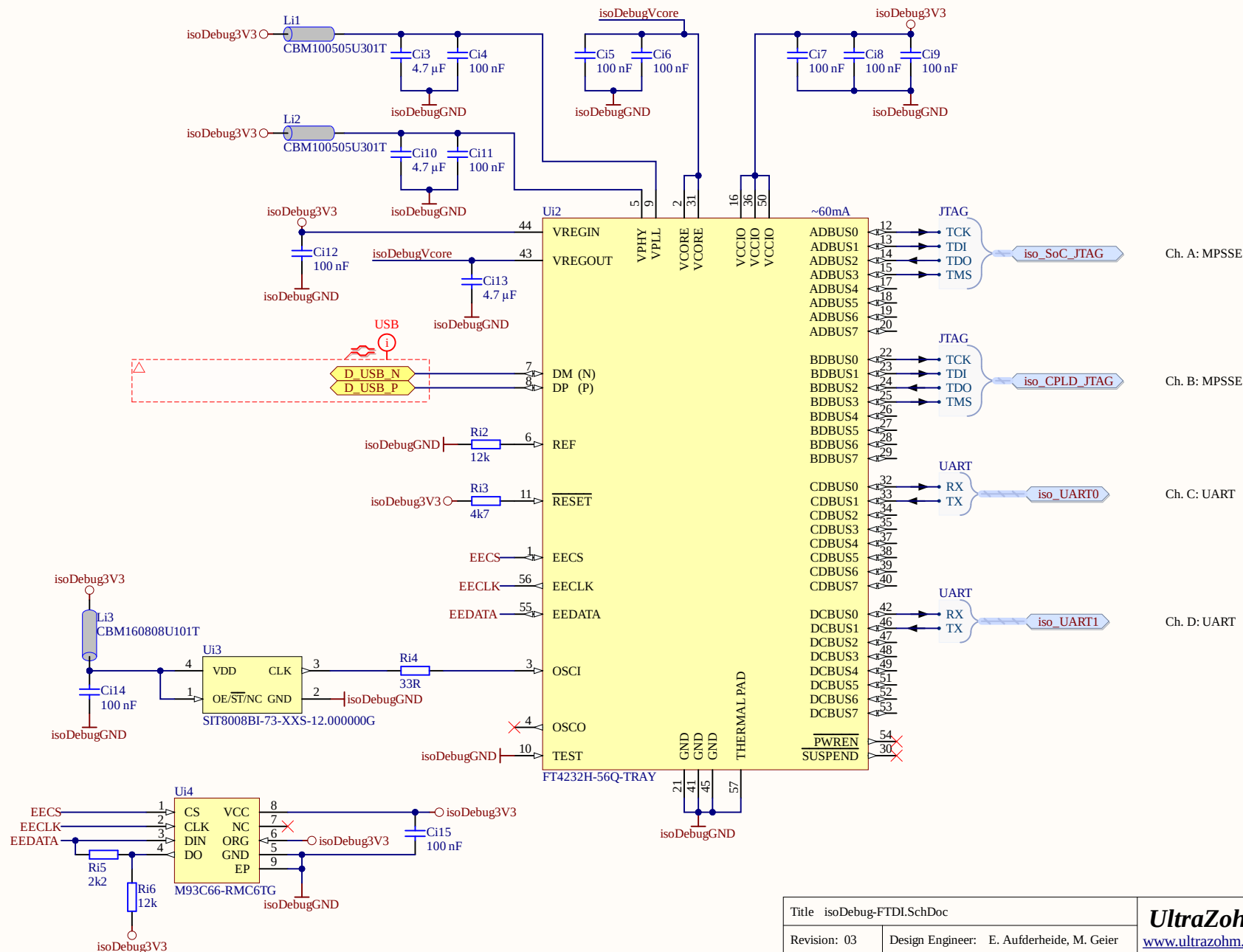
UZ Carrier/Extension side



Isolated side

Processor side





Title isoDebug-FTDI.SchDoc

Revision: 03

Design Engineer: E. Aufderheide, M. Geier

Project: UZ_per_cb_upgrade.PrjPcb

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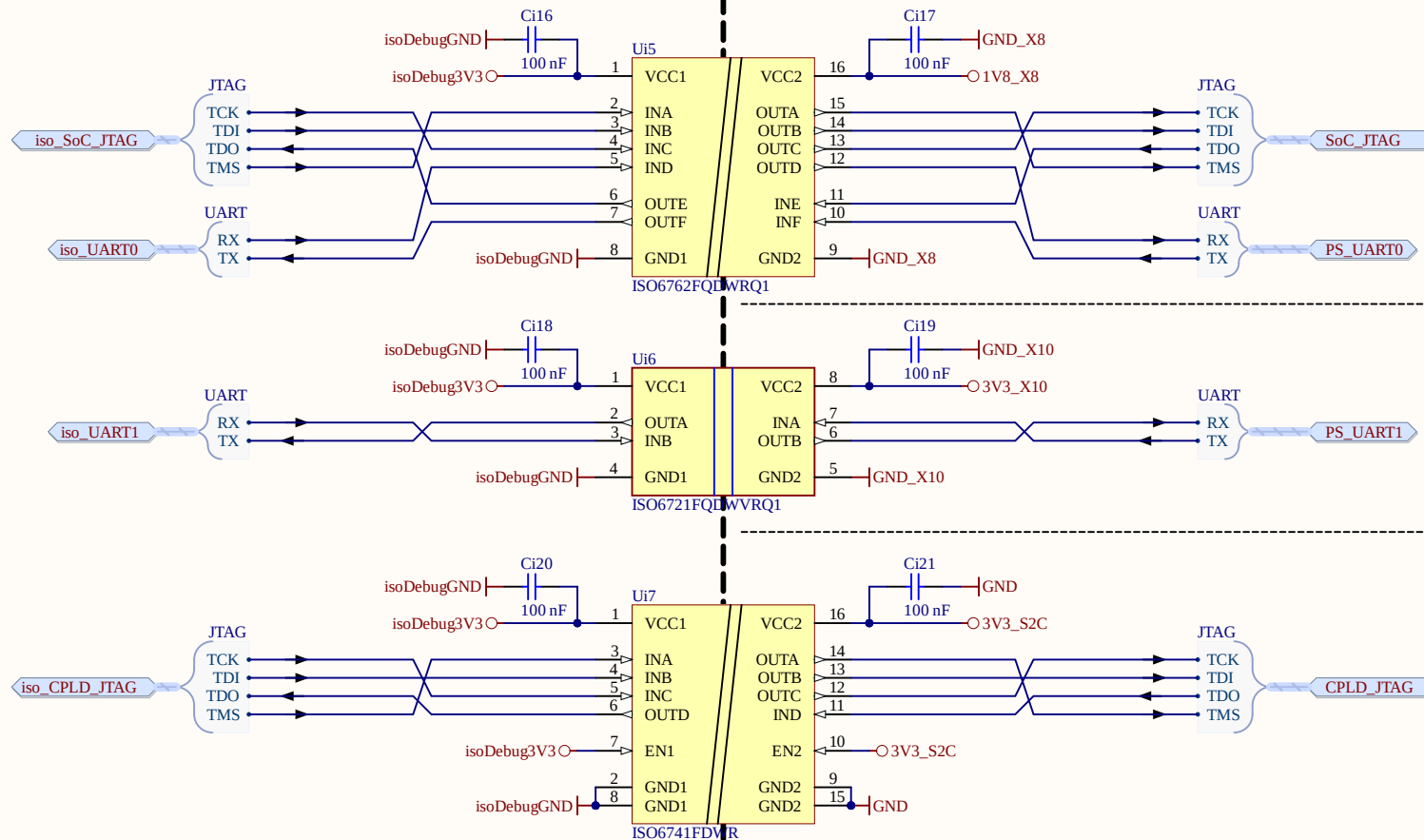
Date: 31/07/2025

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Isolated side

UZ Carrier/Extension side



Title isoDebug-Isolation.SchDoc

Revision: 03

Design Engineer: E. Aufderheide, M. Geier

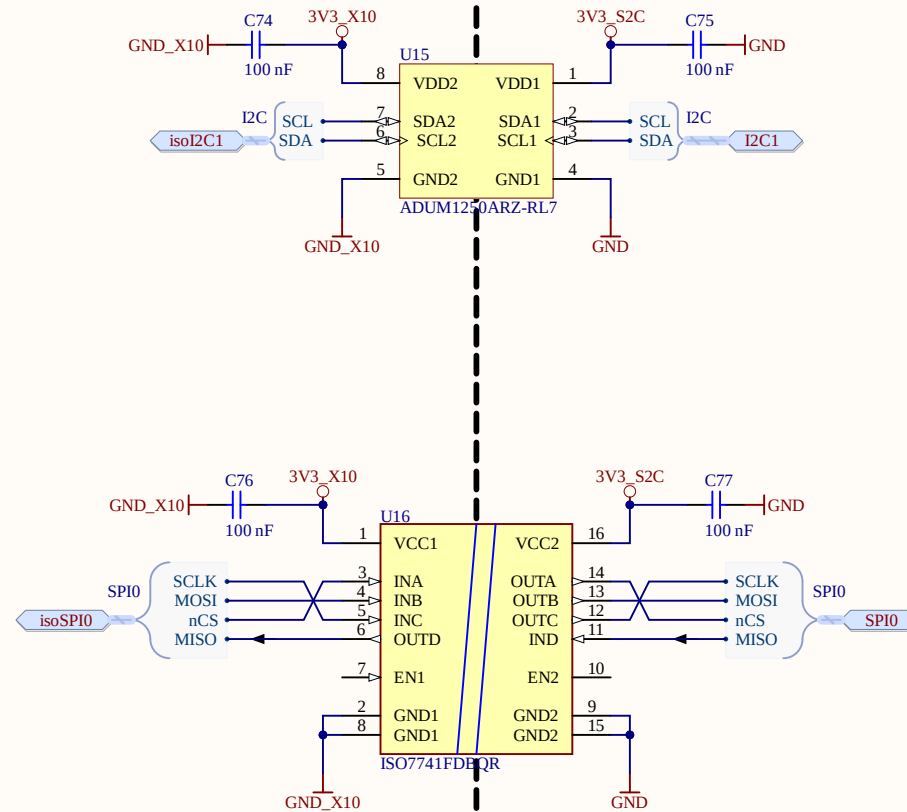
Project: UZ_per_cb_upgrade.PrfPcb

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Date: 31/07/2025

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A

B

C

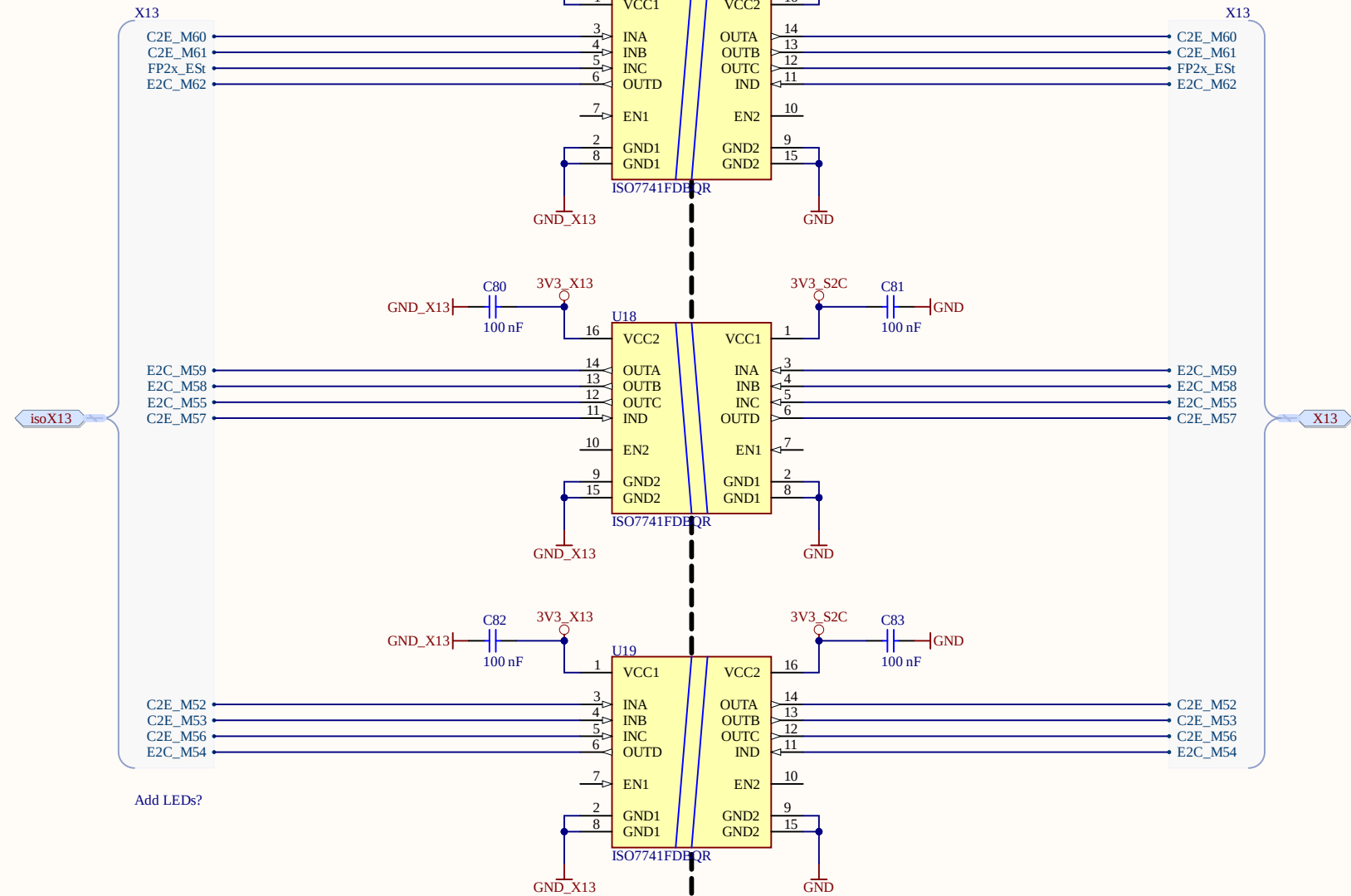
D

A

B

C

D



Title X13-Isolation.SchDoc

Revision: 03

Design Engineer: E. Aufderheide, M. Geier

Project: UZ_per_cb_upgrade.PrjPcb

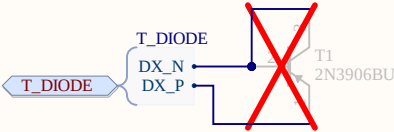
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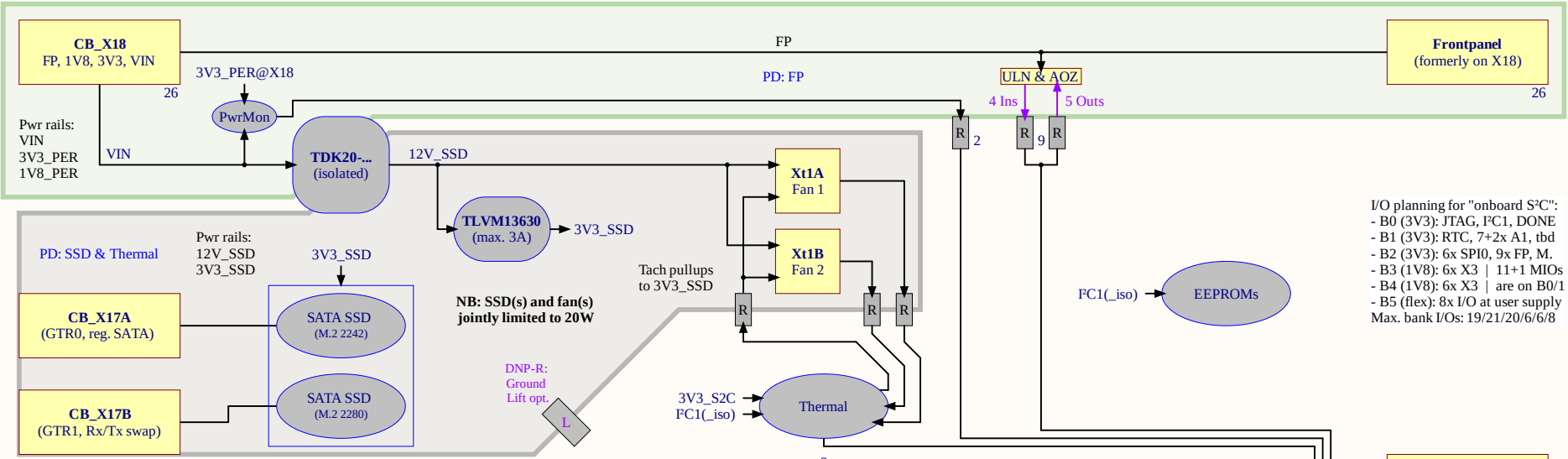
Sheet 24 of 29



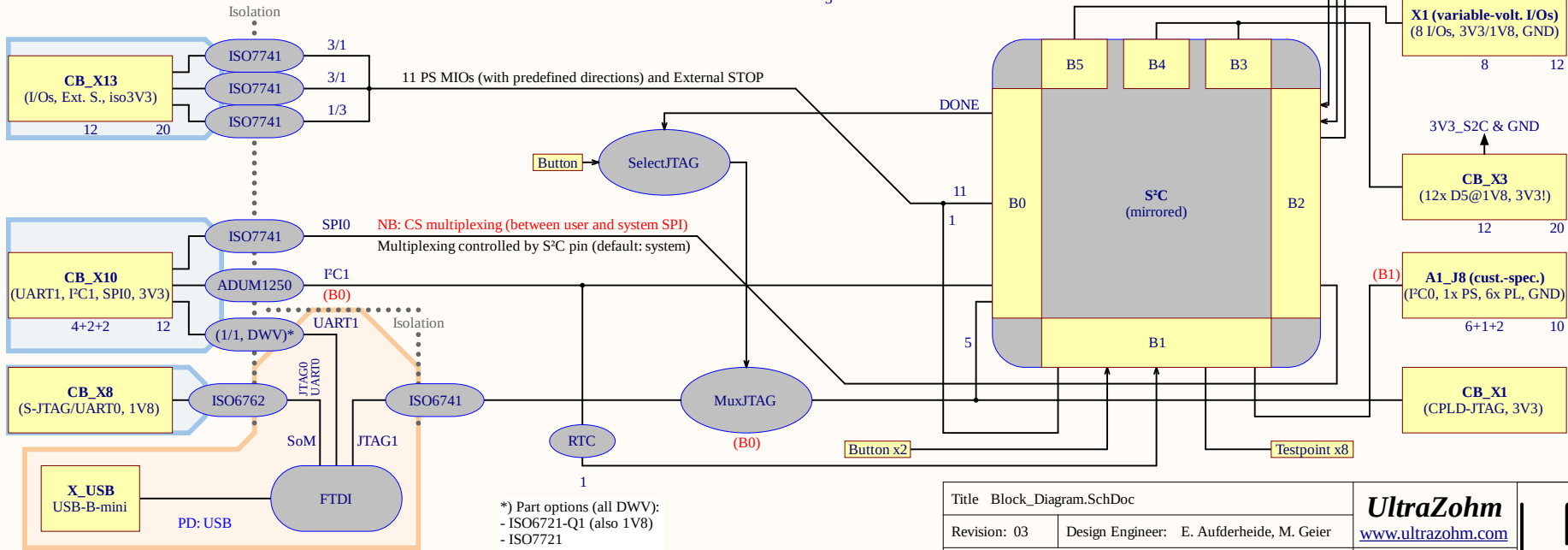


I²C, SSD and S²C Extension for Rev04-UZC-based UltraZohm systems

Partial retrofit of features that are available as standard in Rev05-UZC-based systems such as Linux/network support (EEPROMs), storage (SATA SSD), isolated USB-JTAG/UART, thermal management and a Hw-programmable Controller (S²C) for monitoring, I/O, ...



Pin|MIO | MIO|Pin
P12|M52 | M54|P02
P13|M53 | M55|P03
P15|M56 | M58|P05
P16|M57 | M59|P06
P18|M60 | M62|P08
P19|M61 | !ES!|P09
6x In | 5xO 1xI



*) Part options (all DWV):
- ISO6721-Q1 (also 1V8)
- ISO7721
- ISO7721-Q1

Title Block_Diagram.SchDoc

Revision: 03

Design Engineer: E. Aufderheide, M. Geier

Project: UZ_per_cb_upgrade.PrjPcb

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