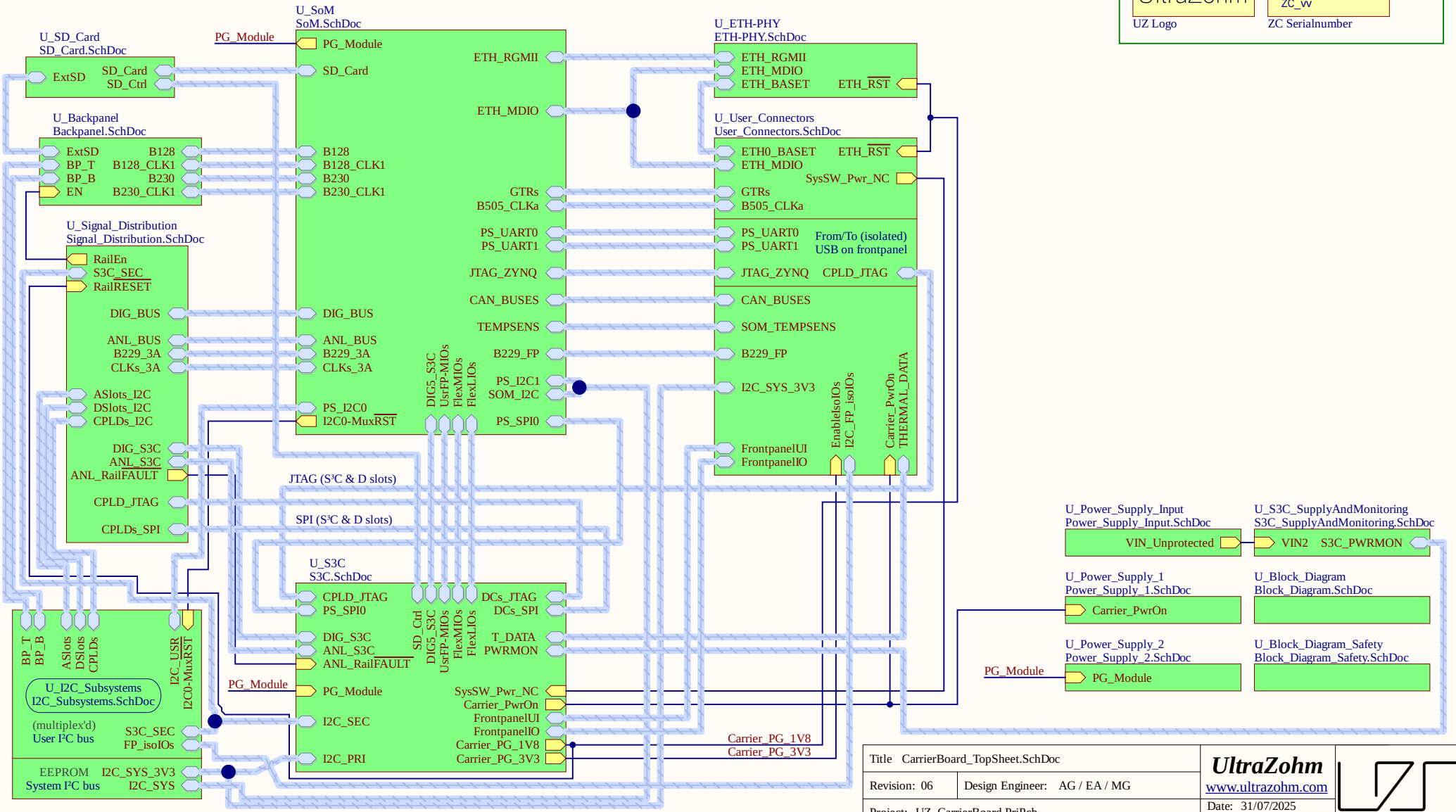
UltraZohm Carrier Board

For more information visit: www.ultrazohm.com

design information, revision number, ...

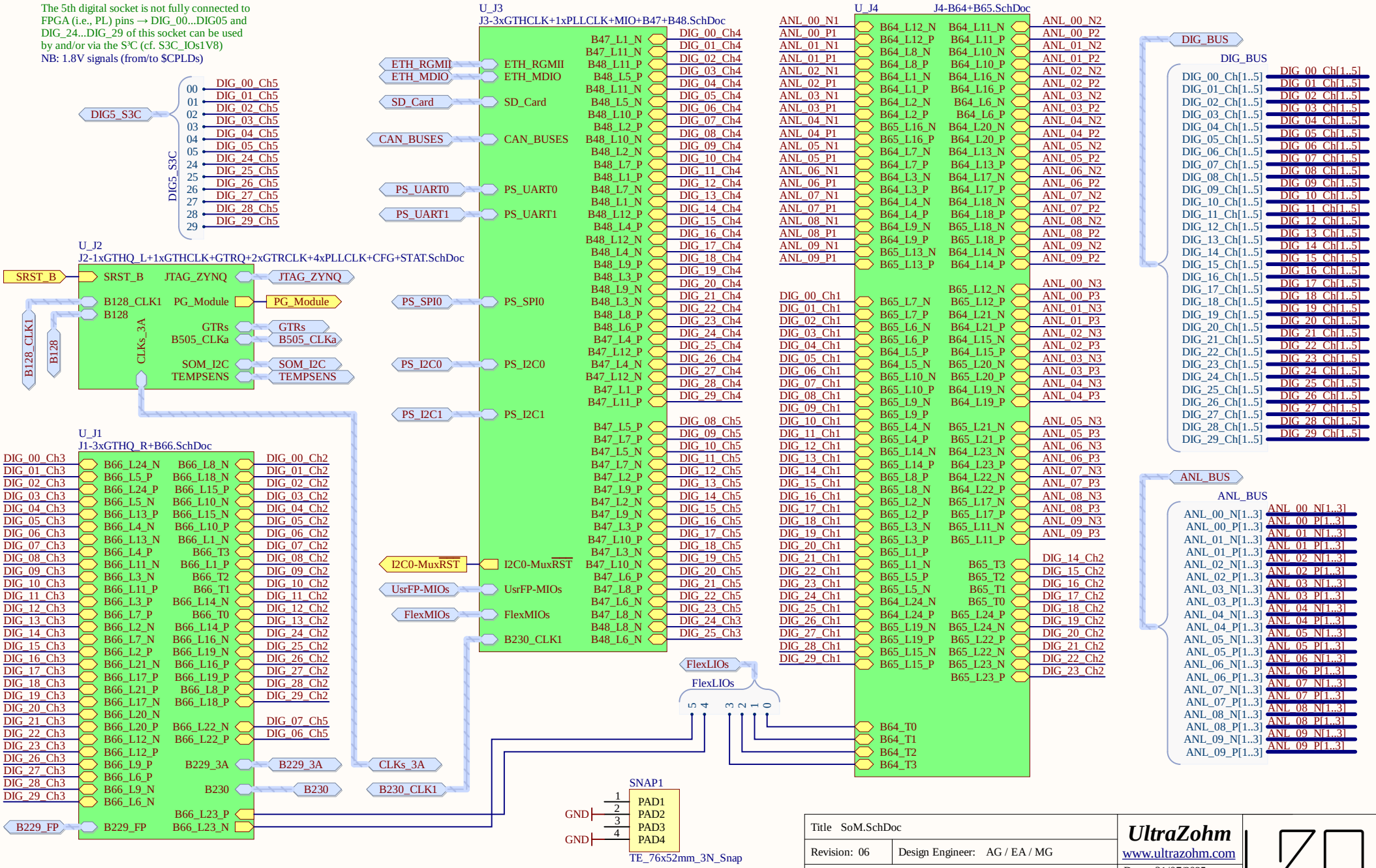
LOGO1 — UZ Logo

Serial1 — ZC_GGG, ZC_PPP, ProjectRevision, ZC_vv — ZC Serialnumber

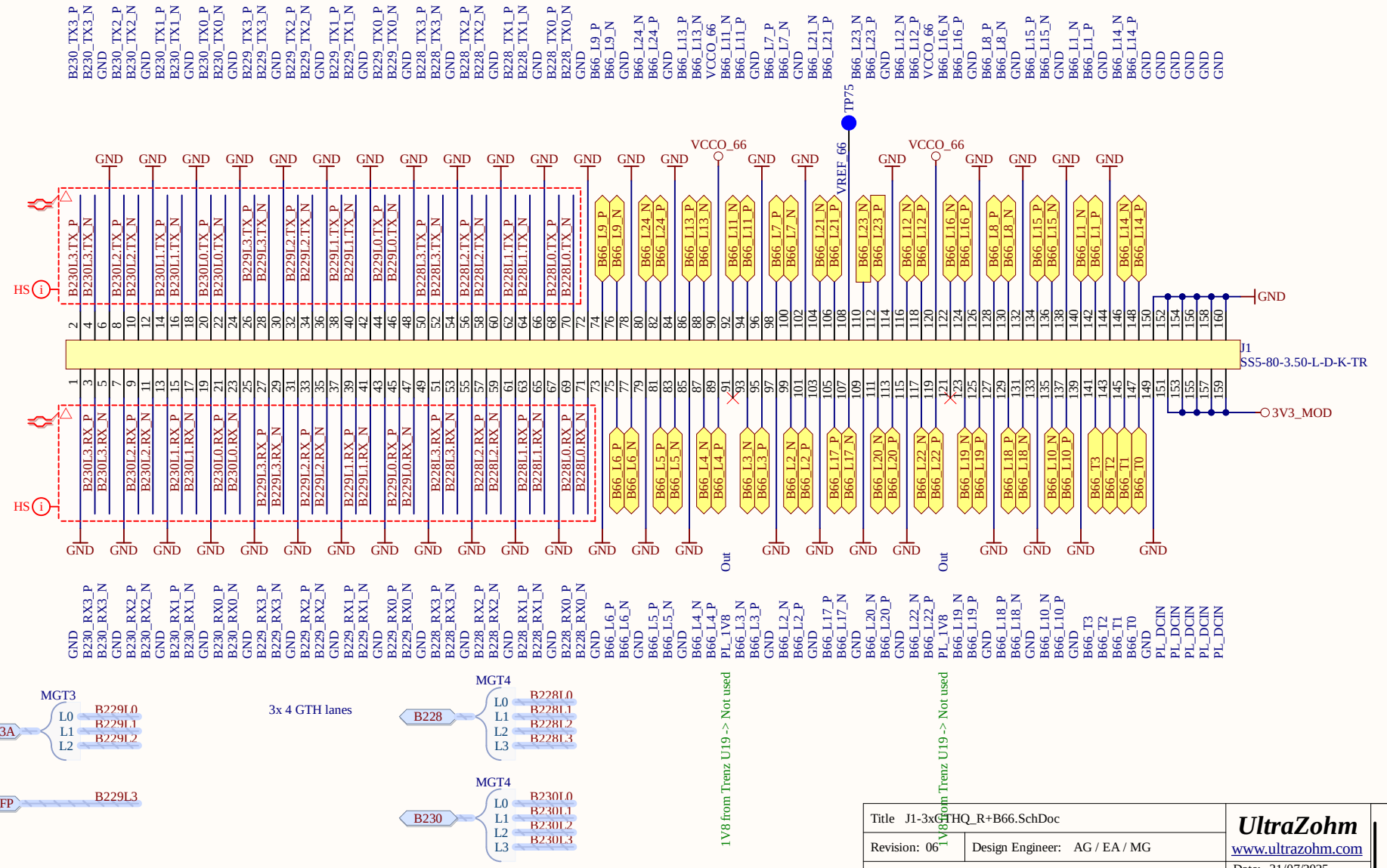


Title CarrierBoard_TopSheet.SchDoc		UltraZohm
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025
		Sheet 1 of 62

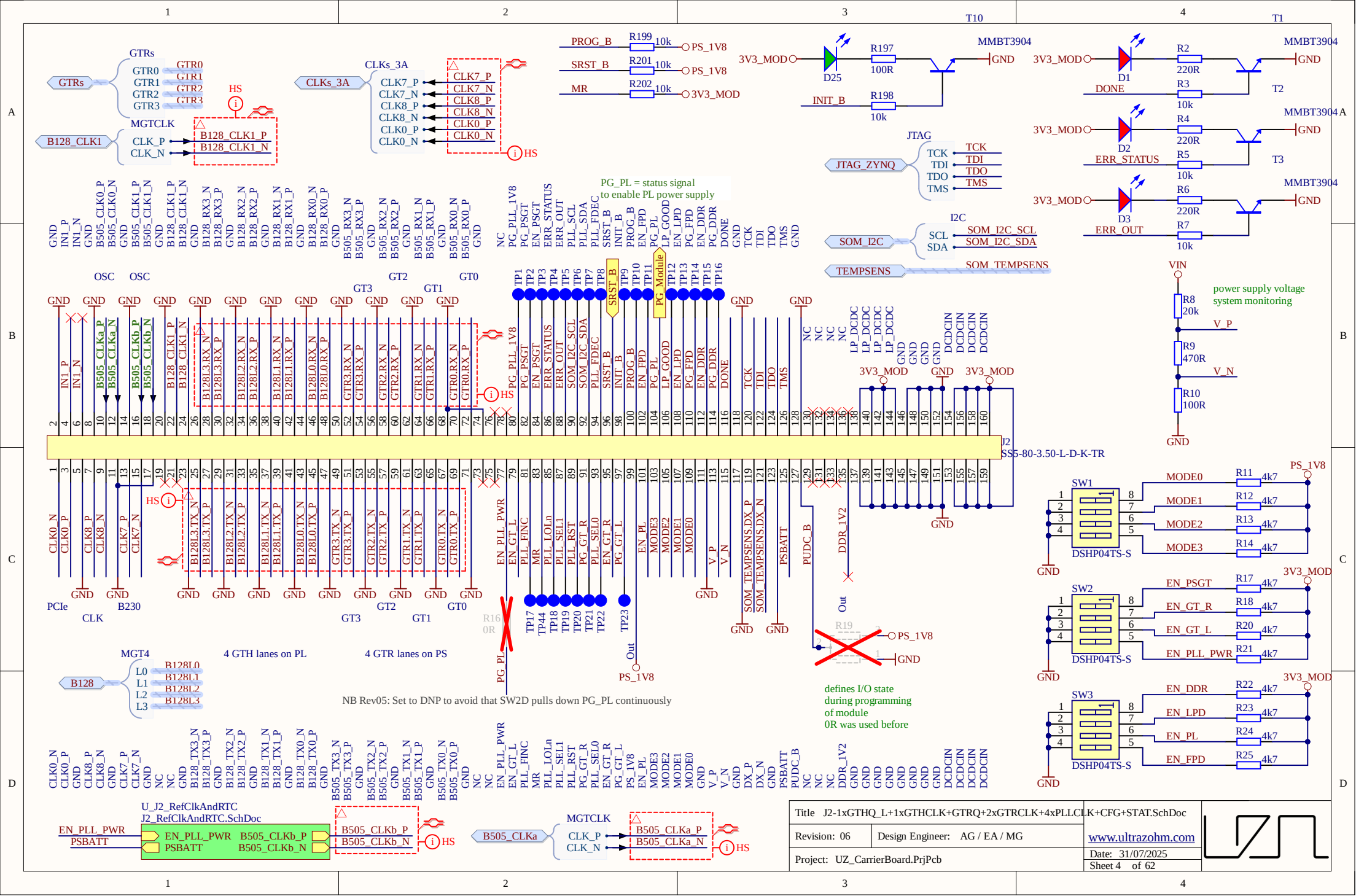
The 5th digital socket is not fully connected to FPGA (i.e., PL) pins → DIG_00...DIG05 and DIG_24...DIG_29 of this socket can be used by and/or via the S³C (cf. S3C_IOs1V8)
NB: 1.8V signals (from/to $CPLDs)



Title SoM.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 2 of 62	



Title J1-3xGTHQ_R+B66.SchDoc		**UltraZohm** www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	Date: 31/07/2025
Project: UZ_CarrierBoard.PrjPcb		Sheet 3 of 62


GTRs
GTR0
GTR1
GTR2
GTR3
MGTCLK
CLK_P
CLK_N
B128_CLK1
B128_CLK1_P
B128_CLK1_N
HS
CLKs_3A
CLK7_P
CLK7_N
CLK8_P
CLK8_N
CLK0_P
CLK0_N
PROG_B
SRST_B
MR
R199 10k
R201 10k
R202 10k
PS_1V8
3V3_MOD
D25
R197 100R
R198 10k
INIT_B
MMBT3904
GND
T10
T1
T2
T3
D1
D2
D3
R2 220R
R3 10k
R4 220R
R5 10k
R6 220R
R7 10k
DONE
ERR_STATUS
ERR_OUT
JTAG
JTAG_ZYNQ
TCK
TDI
TDO
TMS
I2C
SOM_I2C
SCL
SDA
SOM_I2C_SCL
SOM_I2C_SDA
TEMPSENS
SOM_TEMPSENS
PG_PL = status signal
to enable PL power supply
OSC
GT3
GT2
GT1
GT0
J2
SS5-80-3.50-L-D-K-TR
VIN
R8 20k
R9 470R
R10 100R
V_P
V_N
power supply voltage
system monitoring
PCIe
CLK
B230
MGT4
B128
L0
L1
L2
L3
4 GTH lanes on PL
4 GTR lanes on PS
R16 0R
R19
Out
DDR_1V2
PUDC_B
PSBATT
SW1
SW2
SW3
DSHP04TS-S
MODE0
MODE1
MODE2
MODE3
EN_PSGT
EN_GT_R
EN_GT_L
EN_PLL_PWR
EN_DDR
EN_LPD
EN_PL
EN_FPD
R11 4k7
R12 4k7
R13 4k7
R14 4k7
R17 4k7
R18 4k7
R20 4k7
R21 4k7
R22 4k7
R23 4k7
R24 4k7
R25 4k7
defines I/O state
during programming
of module
0R was used before
NB Rev05: Set to DNP to avoid that SW2D pulls down PG_PL continuously
U_J2_RefClkAndRTC
J2_RefClkAndRTC.SchDoc
B505_CLKa
B505_CLKa_P
B505_CLKa_N
B505_CLKb_P
B505_CLKb_N
Title J2-1xGTHQ_L+1xGTHCLK+GTRQ+2xGTRCLK+4xPLLCLK+CFG+STAT.SchDoc
Revision: 06
Design Engineer: AG / EA / MG
Project: UZ_CarrierBoard.PrjPcb
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Date: 31/07/2025
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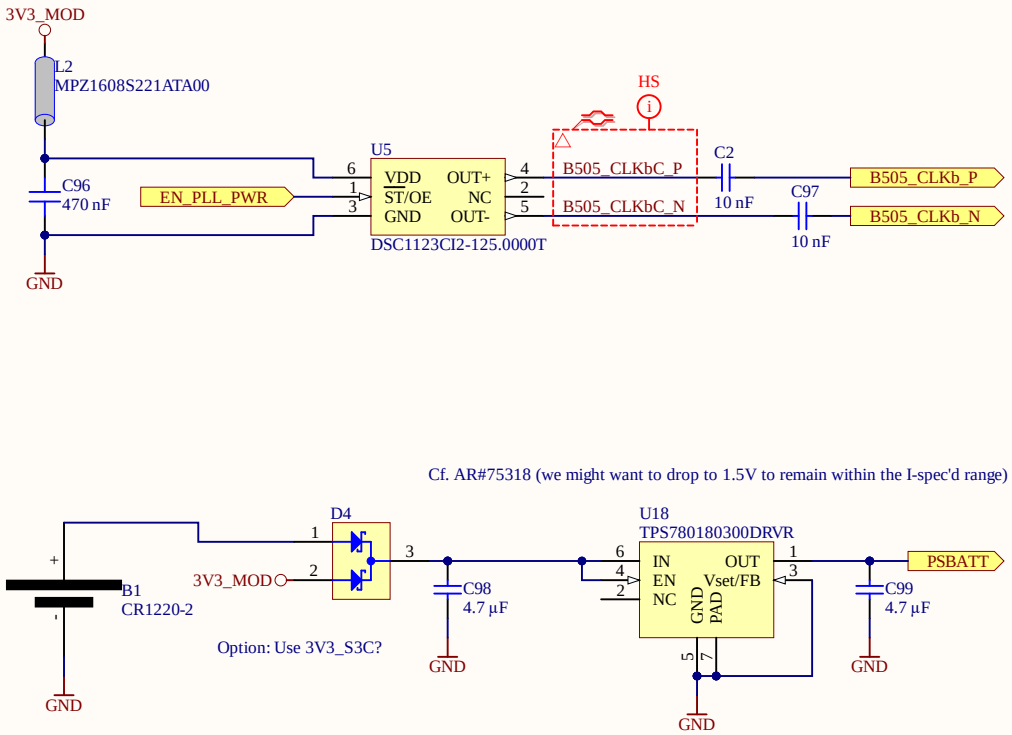
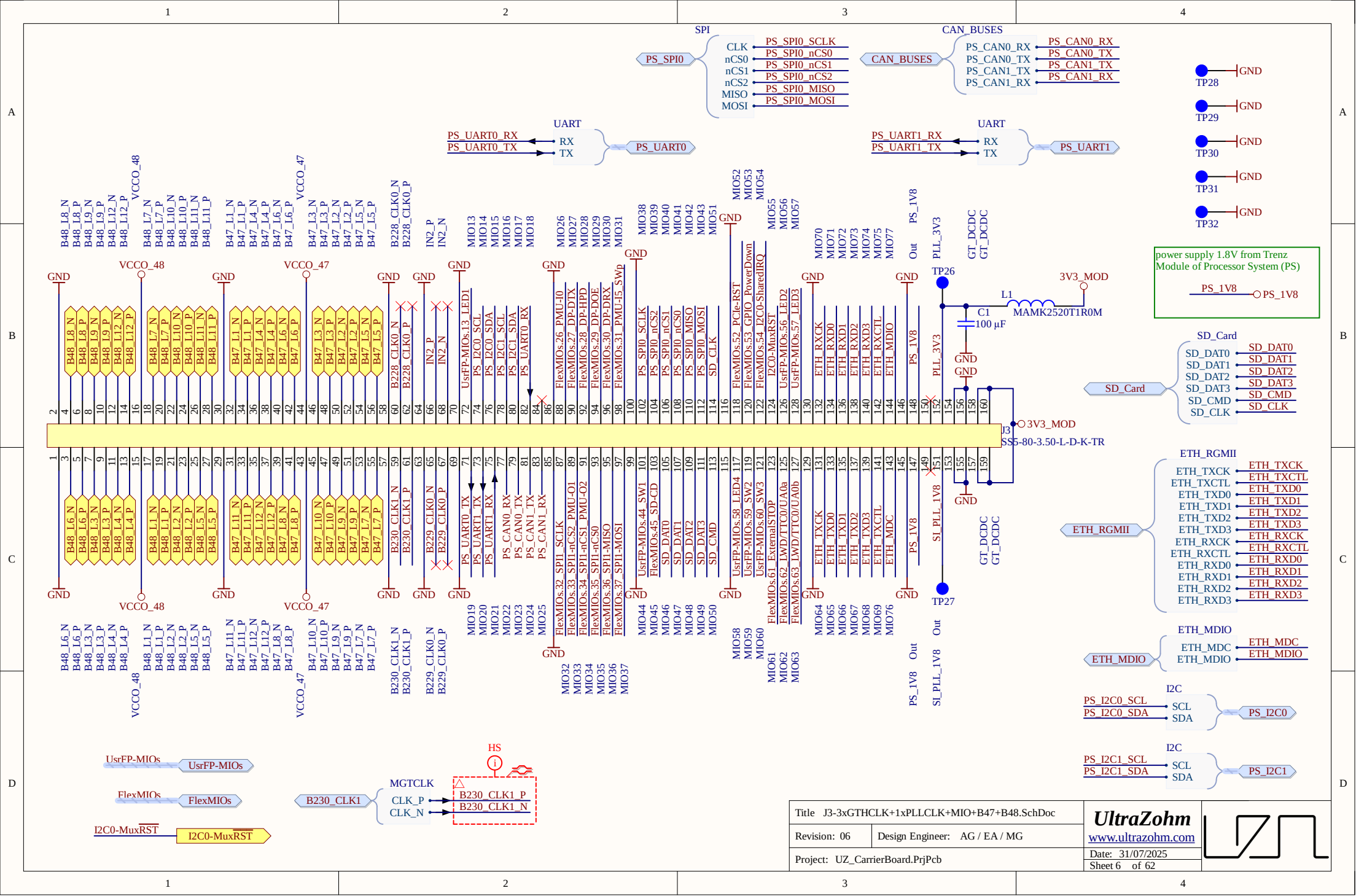


Title J2_RefClkAndRTC.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 06	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 5 of 62	



Title	J3-3xGTHCLK+1xPLLCLK+MIO+B47+B48.SchDoc
Revision: 06	Design Engineer: AG / EA / MG
Project: UZ_CarrierBoard.PrjPcb	

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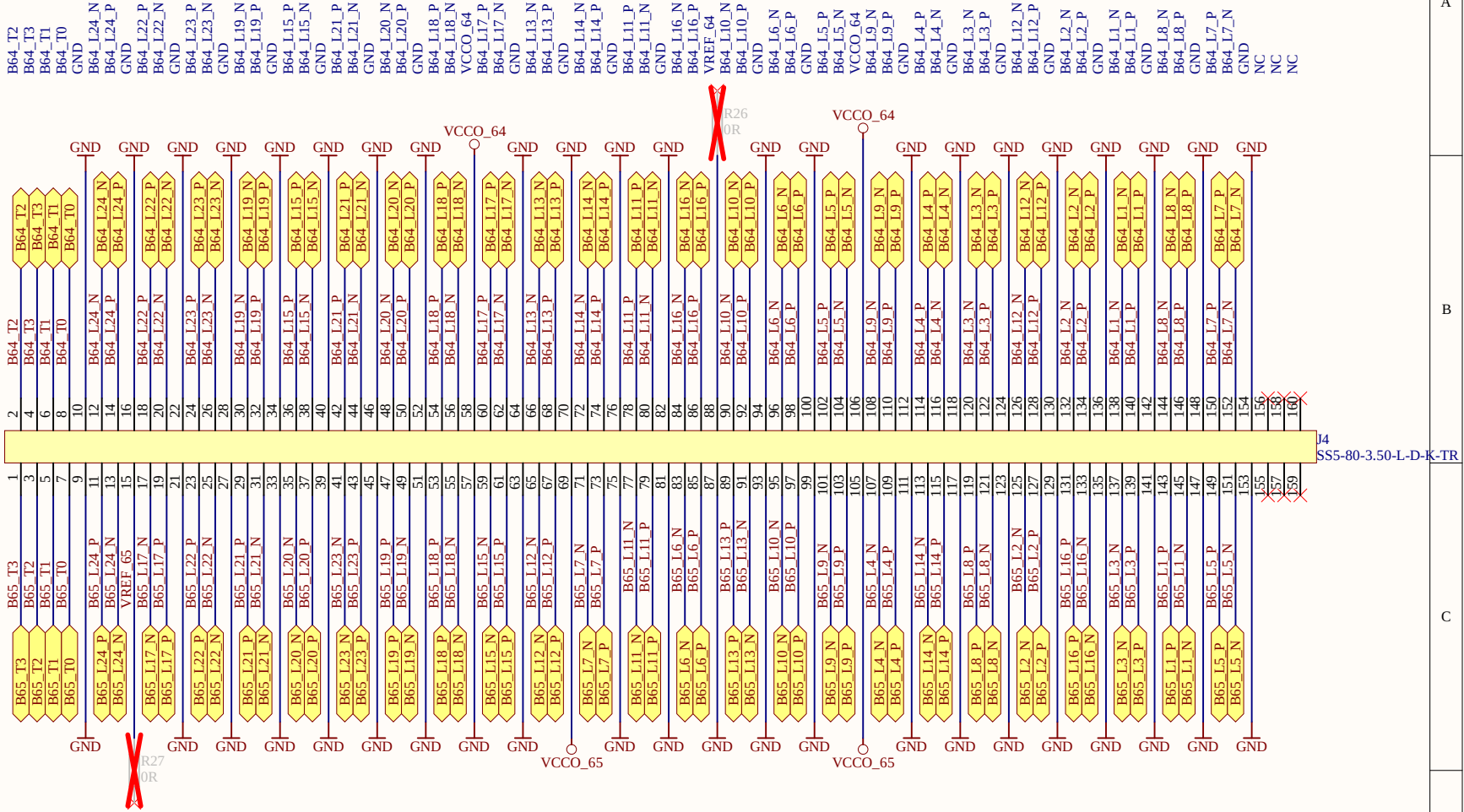
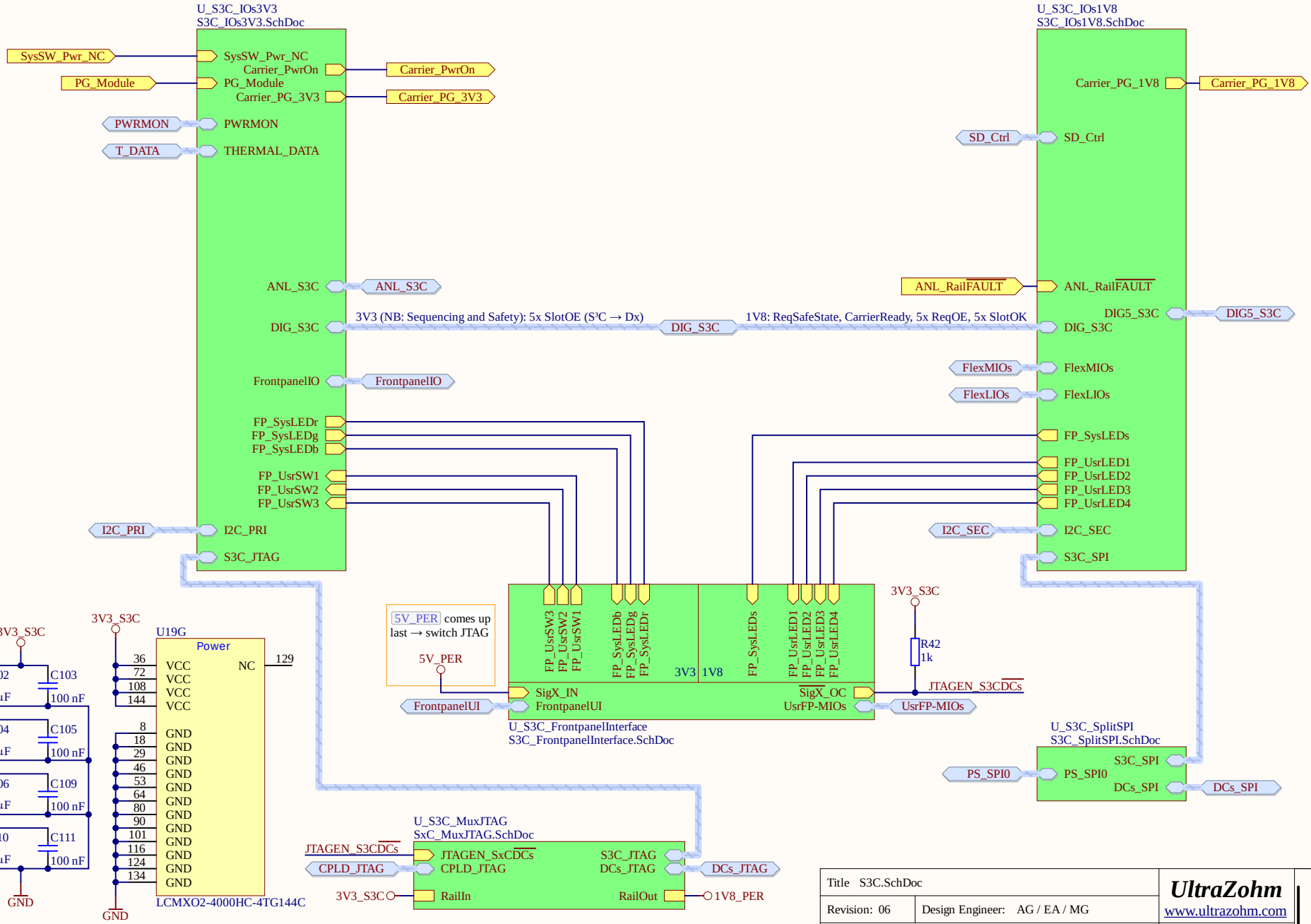


Title J4-B64+B65.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 7 of 62


U_S3C_IOs3V3
S3C_IOs3V3.SchDoc
SysSW_Pwr_NC
PG_Module
PWRMON
T_DATA
Carrier_PwrOn
Carrier_PG_3V3
ANL_S3C
DIG_S3C
FrontpanelIO
FP_SysLEDr
FP_SysLEDg
FP_SysLEDb
FP_UsrSW1
FP_UsrSW2
FP_UsrSW3
I2C_PRI
S3C_JTAG
3V3 (NB: Sequencing and Safety): 5x SlotOE (S³C → Dx)
U_S3C_IOs1V8
S3C_IOs1V8.SchDoc
Carrier_PG_1V8
SD_Ctrl
ANL_RailFAULT
DIG5_S3C
FlexMIOs
FlexLIOs
FP_SysLEDs
FP_UsrLED1
FP_UsrLED2
FP_UsrLED3
FP_UsrLED4
I2C_SEC
S3C_SPI
1V8: ReqSafeState, CarrierReady, 5x ReqOE, 5x SlotOK
5V_PER comes up last → switch JTAG
5V_PER
3V3
1V8
SigX_IN
SigX_OC
FrontpanelUI
UsrFP-MIOs
U_S3C_FrontpanelInterface
S3C_FrontpanelInterface.SchDoc
3V3_S3C
R42
1k
JTAGEN_S3CDCs
U_S3C_SplitSPI
S3C_SplitSPI.SchDoc
PS_SPI0
DCs_SPI
U19G
Power
VCC
GND
NC
LCMXO2-4000HC-4TG144C
C102
C103
C104
C105
C106
C109
C110
C111
10 µF
100 nF
U_S3C_MuxJTAG
SxC_MuxJTAG.SchDoc
JTAGEN_SxCDCs
CPLD_JTAG
RailIn
RailOut
1V8_PER
Title S3C.SchDoc
Revision: 06
Design Engineer: AG / EA / MG
Project: UZ_CarrierBoard.PrjPcb
UltraZohm
www.ultrazohm.com
Date: 31/07/2025
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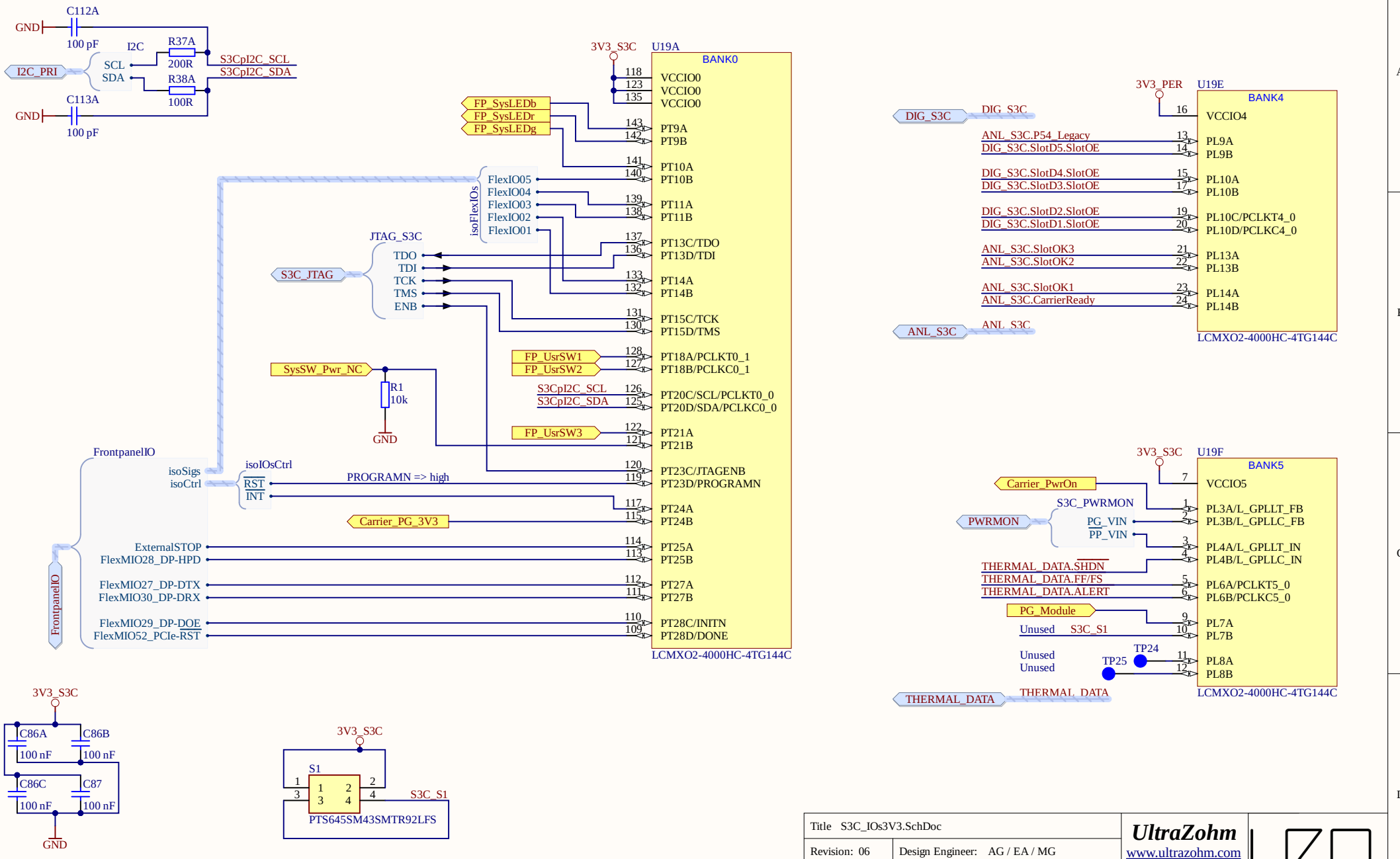
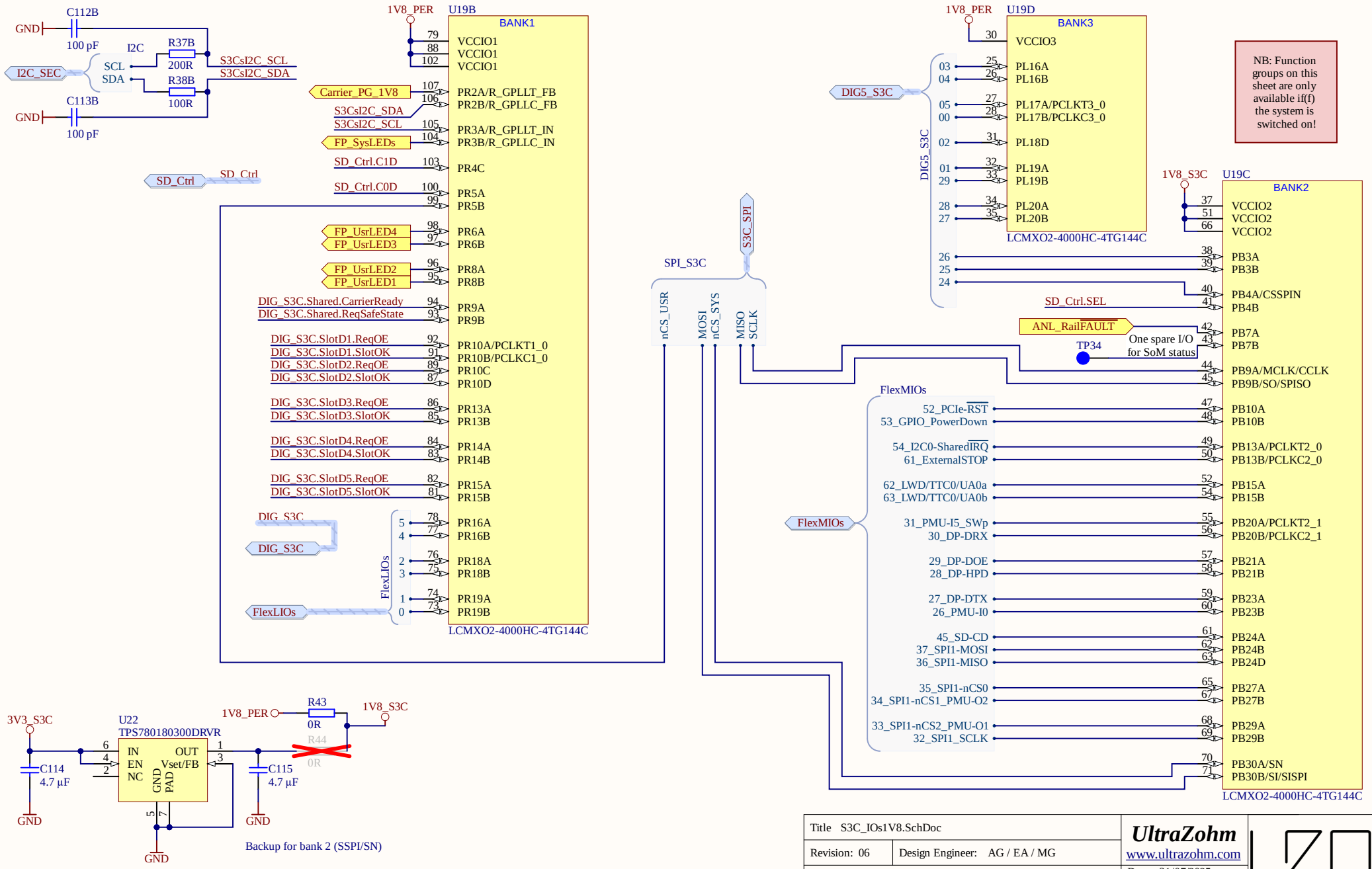


Title S3C_IOs3V3.SchDoc		**UltraZohm**	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 9 of 62	


C112B
GND
100 pF
I2C
R37B
200R
S3CsI2C_SCL
I2C_SEC
SCL
SDA
R38B
100R
S3CsI2C_SDA
C113B
GND
100 pF
1V8_PER
U19B
BANK1
79 VCCIO1
88 VCCIO1
102 VCCIO1
Carrier_PG_1V8
107 PR2A/R_GPLLT_FB
106 PR2B/R_GPLLC_FB
S3CsI2C_SDA
S3CsI2C_SCL
105 PR3A/R_GPLLT_IN
104 PR3B/R_GPLLC_IN
FP_SysLEDs
SD_Ctrl.C1D
103 PR4C
SD_Ctrl
SD_Ctrl
SD_Ctrl.C0D
100 PR5A
99 PR5B
FP_UsrLED4
98 PR6A
FP_UsrLED3
97 PR6B
FP_UsrLED2
96 PR8A
FP_UsrLED1
95 PR8B
DIG_S3C.Shared.CarrierReady
94 PR9A
DIG_S3C.Shared.ReqSafeState
93 PR9B
DIG_S3C.SlotD1.ReqOE
92 PR10A/PCLKT1_0
DIG_S3C.SlotD1.SlotOK
91 PR10B/PCLKC1_0
DIG_S3C.SlotD2.ReqOE
89 PR10C
DIG_S3C.SlotD2.SlotOK
87 PR10D
DIG_S3C.SlotD3.ReqOE
86 PR13A
DIG_S3C.SlotD3.SlotOK
85 PR13B
DIG_S3C.SlotD4.ReqOE
84 PR14A
DIG_S3C.SlotD4.SlotOK
83 PR14B
DIG_S3C.SlotD5.ReqOE
82 PR15A
DIG_S3C.SlotD5.SlotOK
81 PR15B
DIG_S3C
DIG_S3C
5 78 PR16A
4 77 PR16B
2 76 PR18A
3 75 PR18B
1 74 PR19A
0 73 PR19B
FlexLIOs
FlexLIOs
LCMXO2-4000HC-4TG144C
3V3_S3C
U22
TPS780180300DRVR
IN
EN
NC
OUT
Vset/FB
GND PAD
C114
4.7 µF
GND
1V8_PER
R43
0R
1V8_S3C
R44
0R
C115
4.7 µF
GND
GND
Backup for bank 2 (SSPI/SN)
1V8_PER
U19D
BANK3
30 VCCIO3
DIG5_S3C
03 25 PL16A
04 26 PL16B
05 27 PL17A/PCLKT3_0
00 28 PL17B/PCLKC3_0
02 31 PL18D
01 32 PL19A
29 33 PL19B
28 34 PL20A
27 35 PL20B
DIG5_S3C
LCMXO2-4000HC-4TG144C
NB: Function groups on this sheet are only available if(f) the system is switched on!
1V8_S3C
U19C
BANK2
37 VCCIO2
51 VCCIO2
66 VCCIO2
26 38 PB3A
25 39 PB3B
24 40 PB4A/CSSPIN
SD_Ctrl.SEL
41 PB4B
ANL_RailFAULT
42 PB7A
One spare I/O for SoM status
TP34
43 PB7B
44 PB9A/MCLK/CCLK
45 PB9B/SO/SPISO
S3C_SPI
SPI_S3C
nCS_USR
MOSI
nCS_SYS
MISO
SCLK
FlexMIOs
52_PCIe-RST
47 PB10A
53_GPIO_PowerDown
48 PB10B
54_I2C0-SharedIRQ
49 PB13A/PCLKT2_0
61_ExternalSTOP
50 PB13B/PCLKC2_0
62_LWD/TTC0/UA0a
52 PB15A
63_LWD/TTC0/UA0b
54 PB15B
FlexMIOs
31_PMU-I5_SWp
55 PB20A/PCLKT2_1
30_DP-DRX
56 PB20B/PCLKC2_1
29_DP-DOE
57 PB21A
28_DP-HPD
58 PB21B
27_DP-DTX
59 PB23A
26_PMU-I0
60 PB23B
45_SD-CD
61 PB24A
37_SPI1-MOSI
62 PB24B
36_SPI1-MISO
63 PB24D
35_SPI1-nCS0
65 PB27A
34_SPI1-nCS1_PMU-O2
67 PB27B
33_SPI1-nCS2_PMU-O1
68 PB29A
32_SPI1_SCLK
69 PB29B
70 PB30A/SN
71 PB30B/SI/SISPI
LCMXO2-4000HC-4TG144C
Title S3C_IOs1V8.SchDoc
Revision: 06
Design Engineer: AG / EA / MG
Project: UZ_CarrierBoard.PrjPcb
UltraZohm
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Date: 31/07/2025
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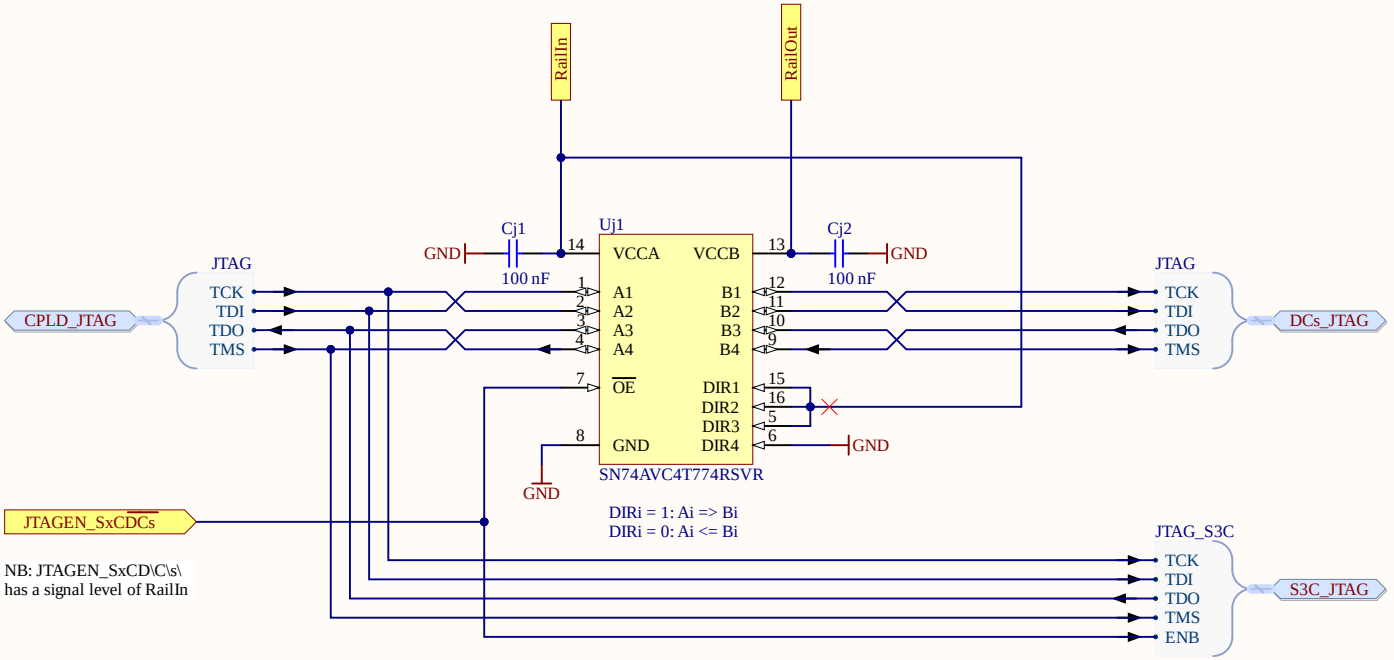
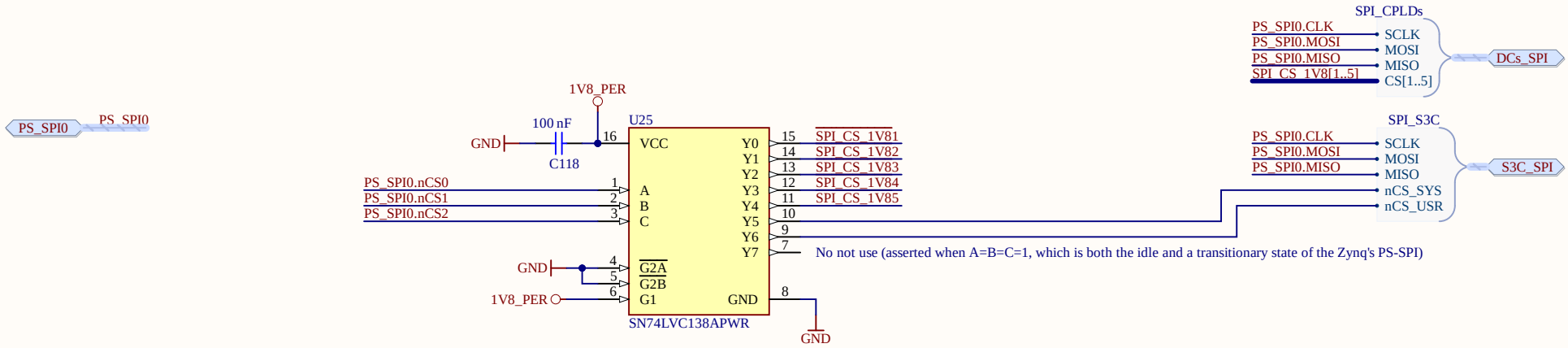
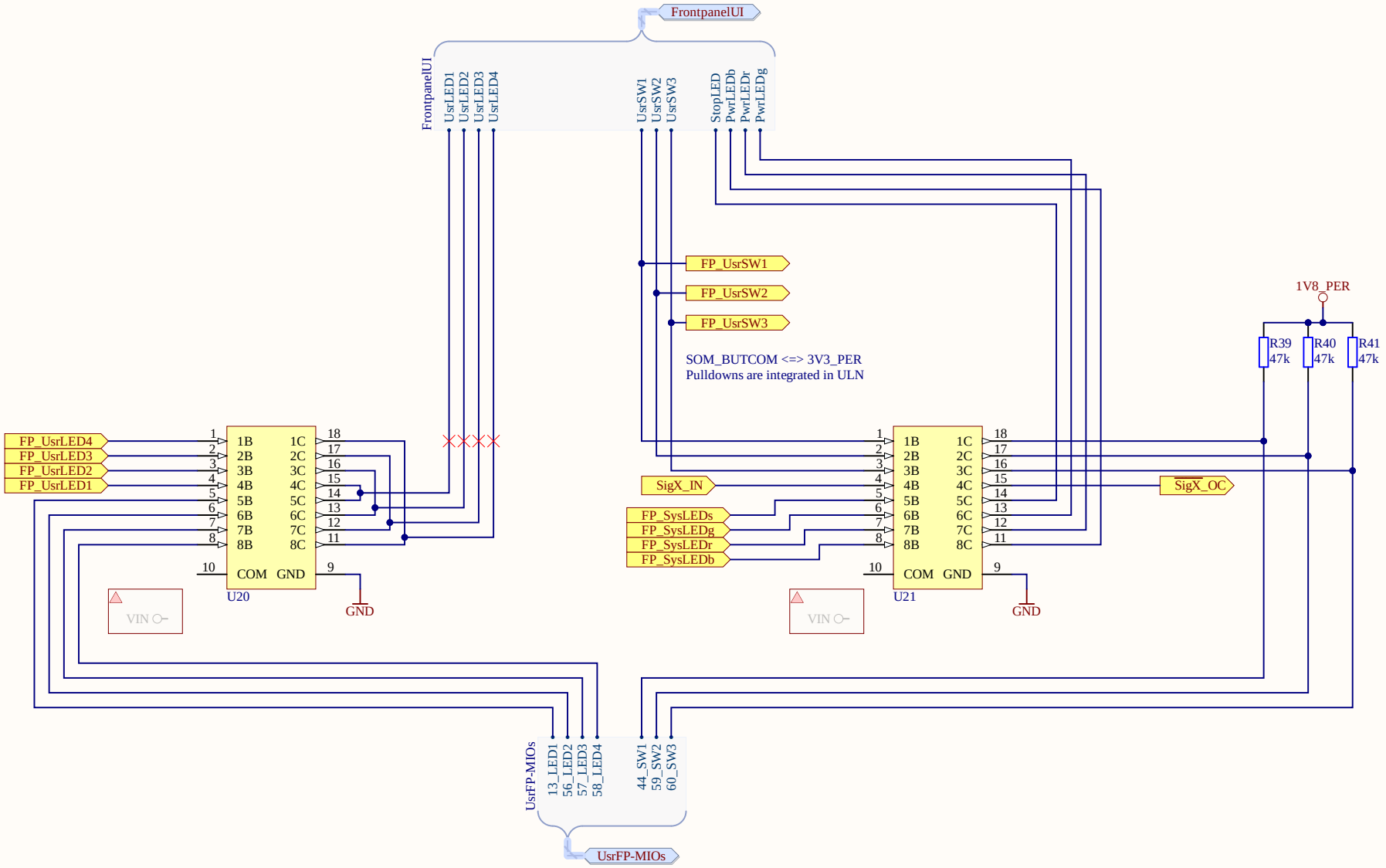


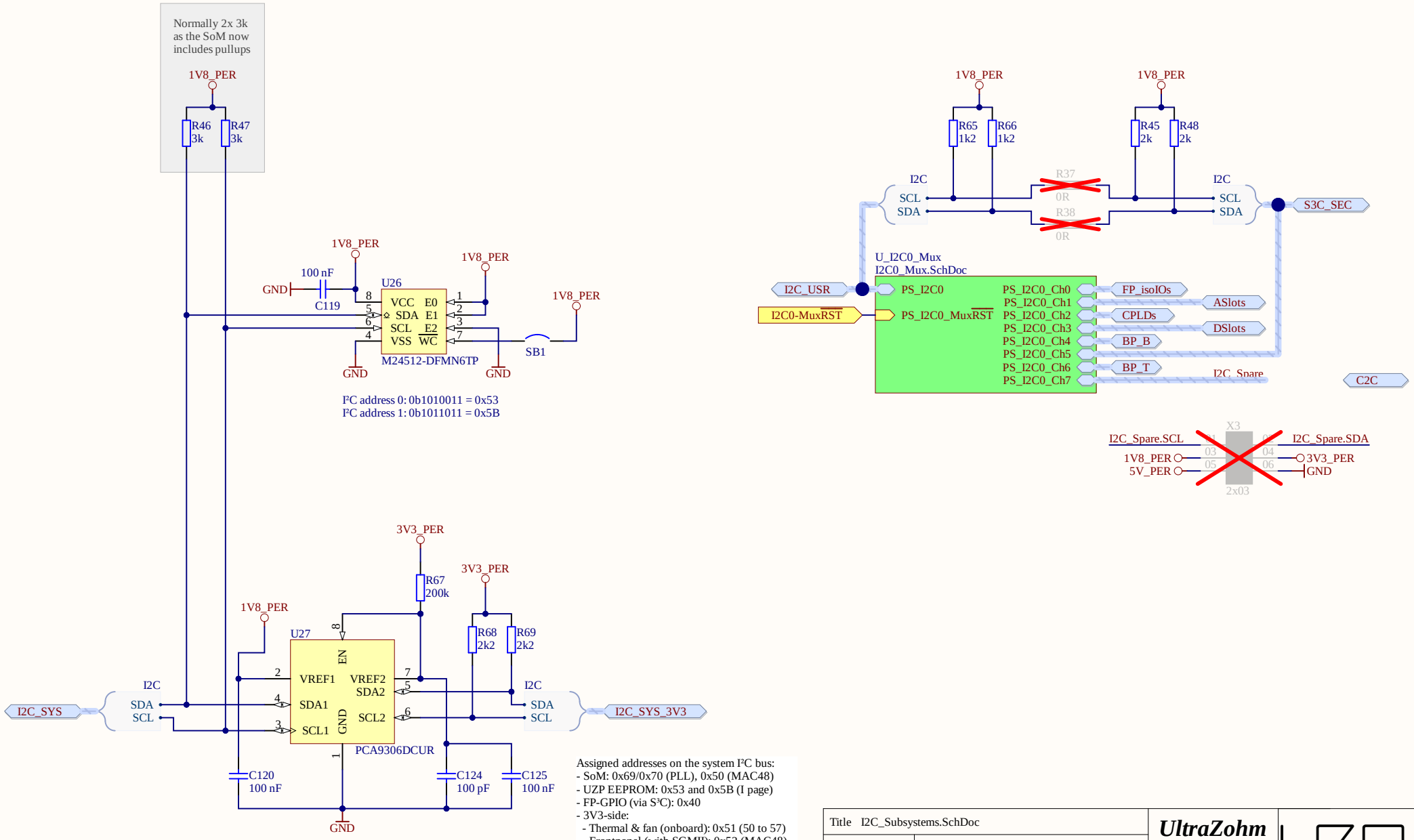
Title SxC_MuxJTAG.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 11 of 62	



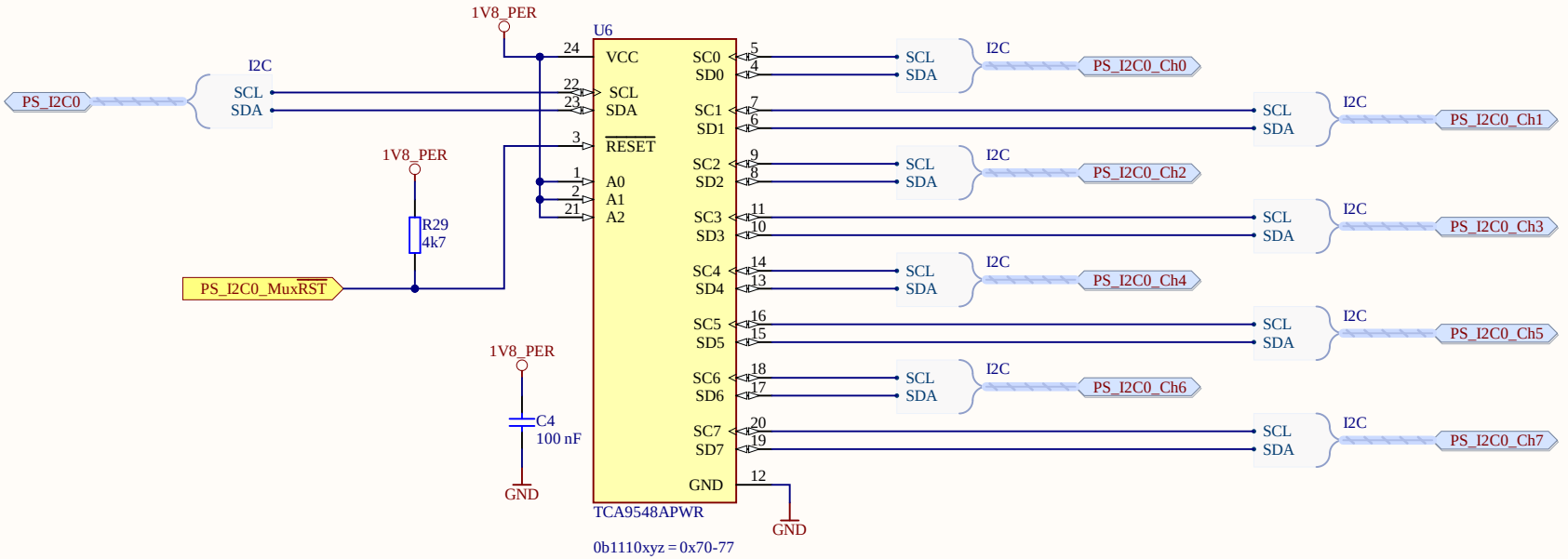
Title S3C_SplitSPI.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 06	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 12 of 62	



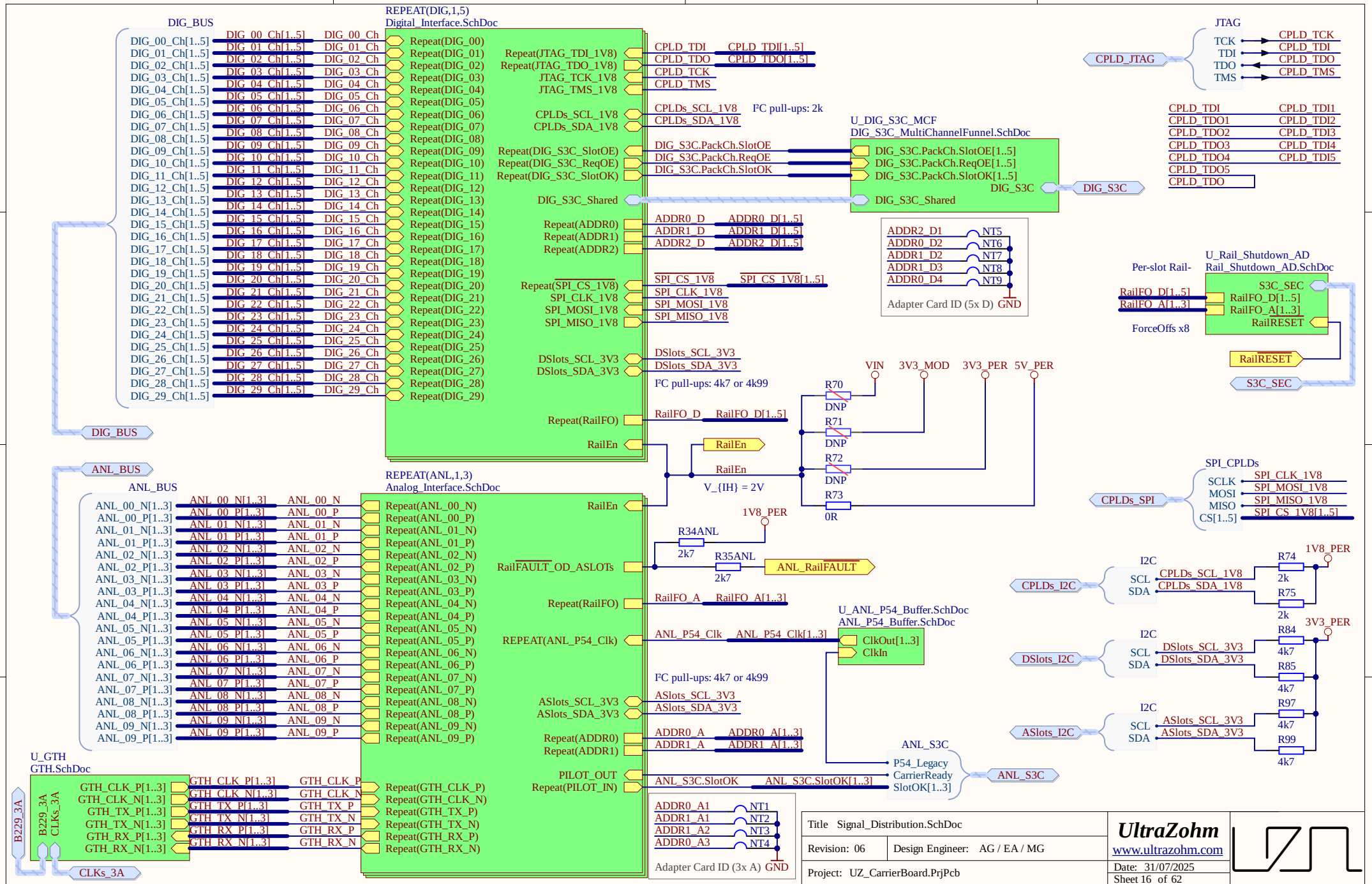
Title S3C_FrontpanelInterface.SchDoc		**UltraZohm** www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	Date: 31/07/2025
Project: UZ_CarrierBoard.PrjPcb		Sheet 13 of 62



Title I2C_Subsystems.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 14 of 62



Title I2C0_Mux.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 15 of 62	


DIG_BUS
REPEAT(DIG,1,5)
Digital_Interface.SchDoc
JTAG
CPLD_JTAG
TCK
TDI
TDO
TMS
CPLD_TCK
CPLD_TDI
CPLD_TDO
CPLD_TMS
CPLD_TDI1
CPLD_TDI2
CPLD_TDI3
CPLD_TDI4
CPLD_TDI5
CPLD_TDO1
CPLD_TDO2
CPLD_TDO3
CPLD_TDO4
CPLD_TDO5
I²C pull-ups: 2k
U_DIG_S3C_MCF
DIG_S3C_MultiChannelFunnel.SchDoc
DIG_S3C.PackCh.SlotOE[1..5]
DIG_S3C.PackCh.ReqOE[1..5]
DIG_S3C.PackCh.SlotOK[1..5]
DIG_S3C
DIG_S3C_Shared
ADDR2_D1
ADDR0_D2
ADDR1_D2
ADDR1_D3
ADDR0_D4
NT5
NT6
NT7
NT8
NT9
GND
Adapter Card ID (5x D)
U_Rail_Shutdown_AD
Rail_Shutdown_AD.SchDoc
Per-slot Rail-
RailFO_D[1..5]
RailFO_A[1..3]
ForceOffs x8
S3C_SEC
RailRESET
I²C pull-ups: 4k7 or 4k99
VIN
3V3_MOD
3V3_PER
5V_PER
R70
R71
R72
R73
DNP
0R
RailEn
V_{IH} = 2V
ANL_BUS
REPEAT(ANL,1,3)
Analog_Interface.SchDoc
1V8_PER
R34ANL
R35ANL
2k7
RailFAULT_OD_ASLOTs
ANL_RailFAULT
SPI_CPLDs
SCLK
MOSI
MISO
CS[1..5]
SPI_CLK_1V8
SPI_MOSI_1V8
SPI_MISO_1V8
SPI_CS_1V8[1..5]
CPLDs_SPI
I²C pull-ups: 4k7 or 4k99
U_ANL_P54_Buffer.SchDoc
ANL_P54_Buffer.SchDoc
ClkOut[1..3]
ClkIn
ANL_P54_Clk
ANL_P54_Clk[1..3]
ANL_S3C
P54_Legacy
CarrierReady
SlotOK[1..3]
ANL_S3C.SlotOK
ANL_S3C.SlotOK[1..3]
I2C
SCL
SDA
CPLDs_I2C
DSlots_I2C
ASlots_I2C
R74
R75
R84
R85
R97
R99
2k
4k7
3V3_PER
U_GTH
GTH.SchDoc
B229_3A
CLKs_3A
GTH_CLK_P[1..3]
GTH_CLK_N[1..3]
GTH_TX_P[1..3]
GTH_TX_N[1..3]
GTH_RX_P[1..3]
GTH_RX_N[1..3]
ADDR0_A1
ADDR1_A1
ADDR1_A2
ADDR0_A3
NT1
NT2
NT3
NT4
Adapter Card ID (3x A)
Title Signal_Distribution.SchDoc
Revision: 06
Design Engineer: AG / EA / MG
Project: UZ_CarrierBoard.PrjPcb
UltraZohm
www.ultrazohm.com
Date: 31/07/2025
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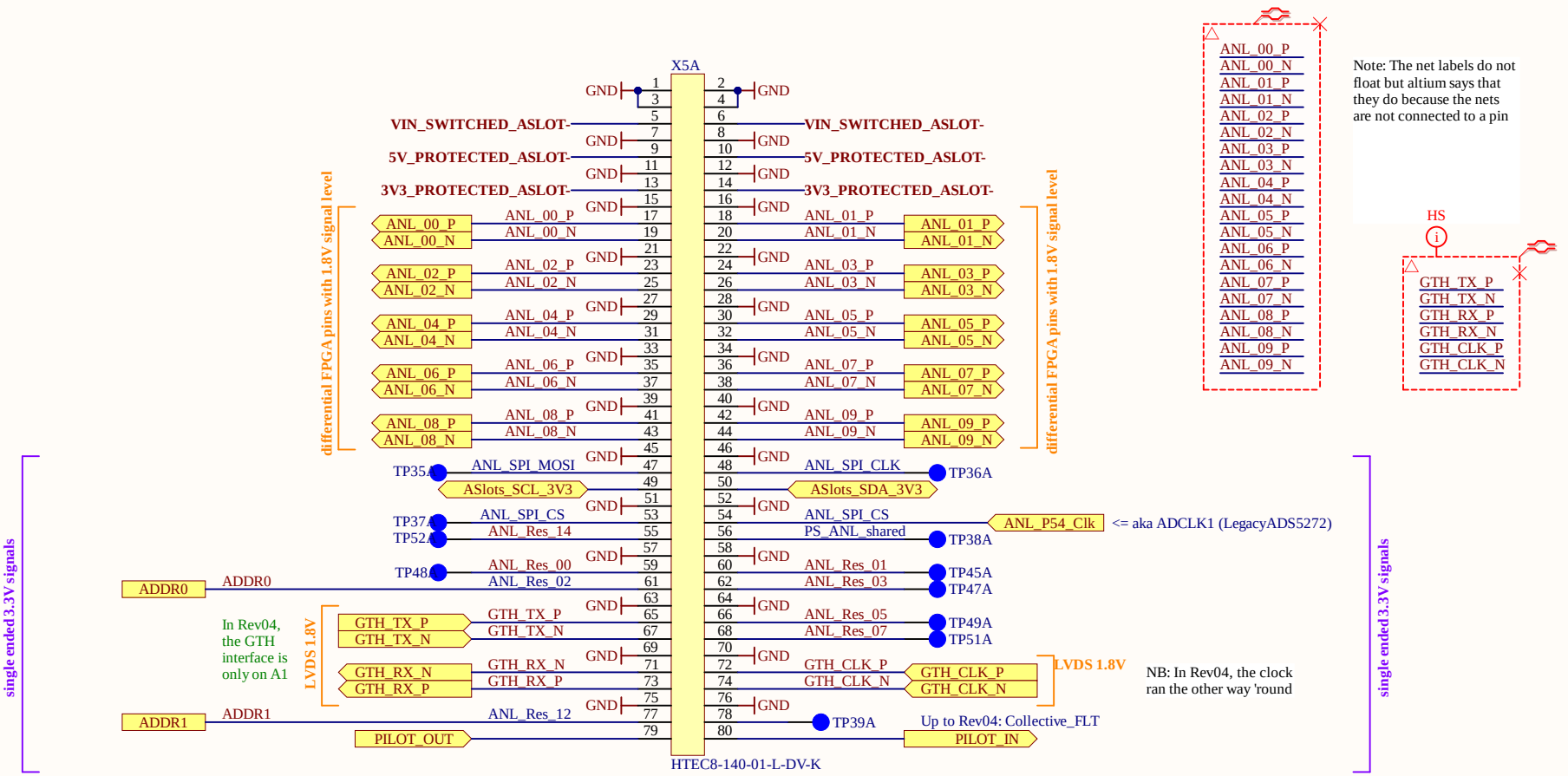
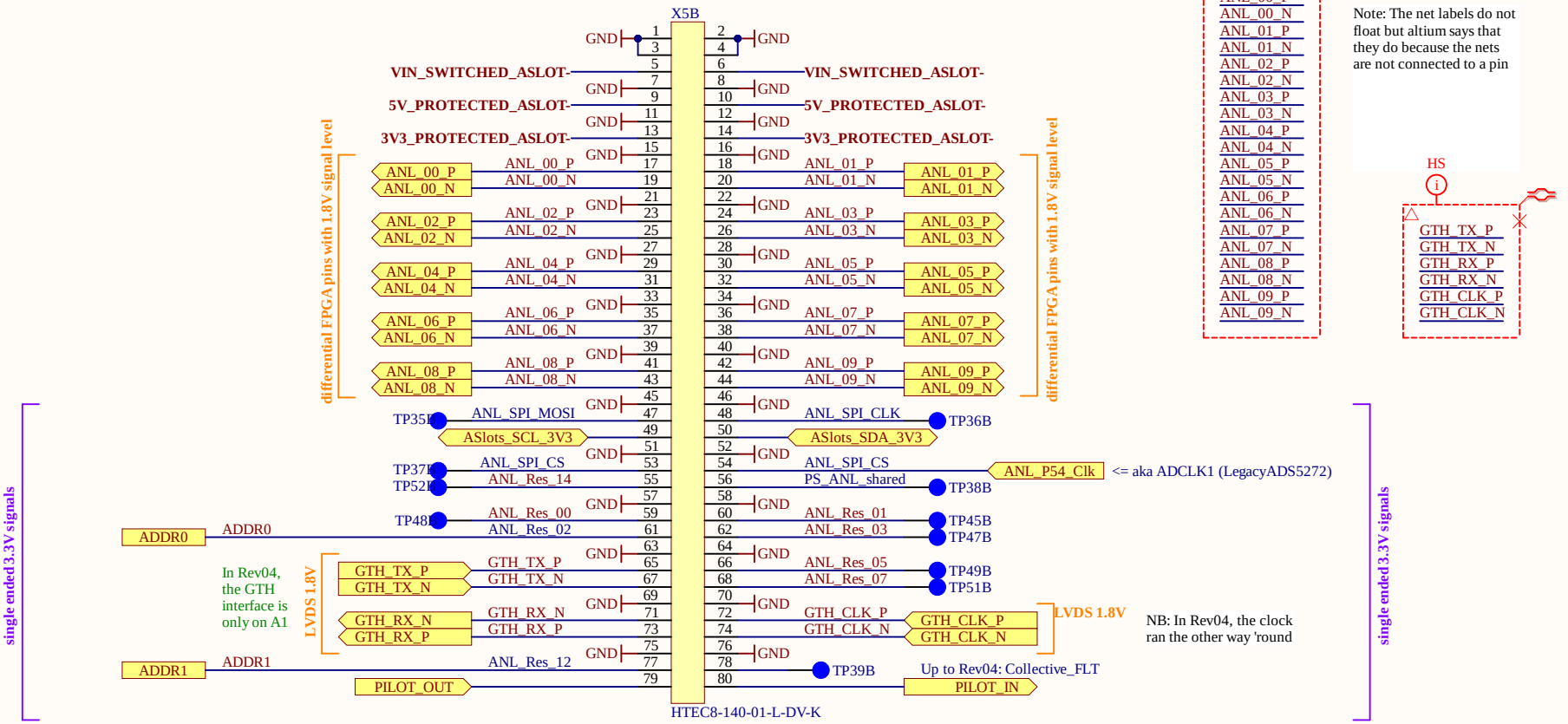
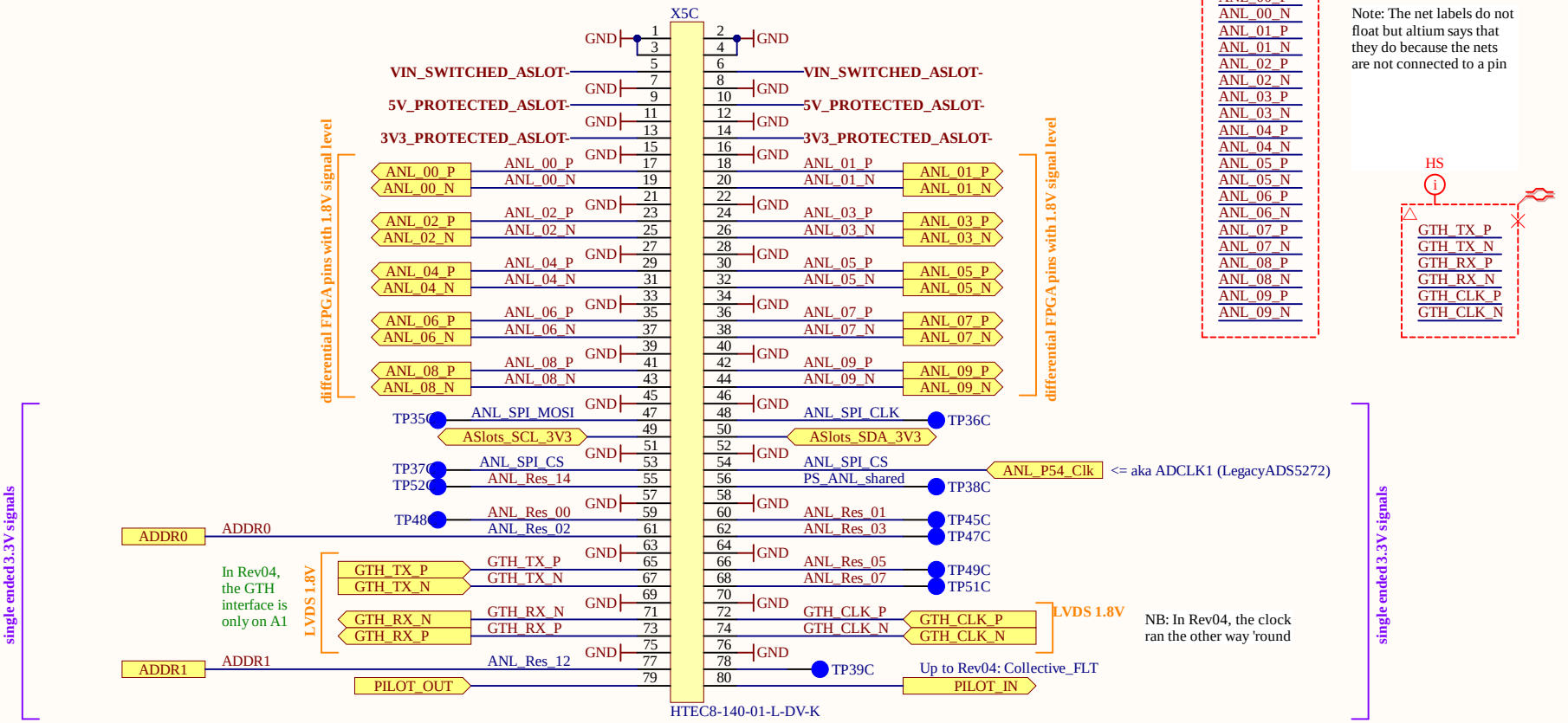
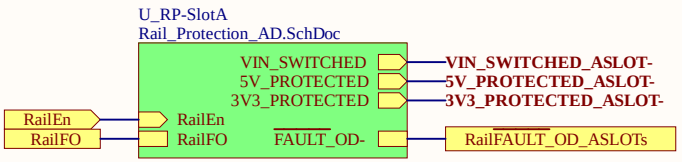


Title Analog_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 17.1of 62

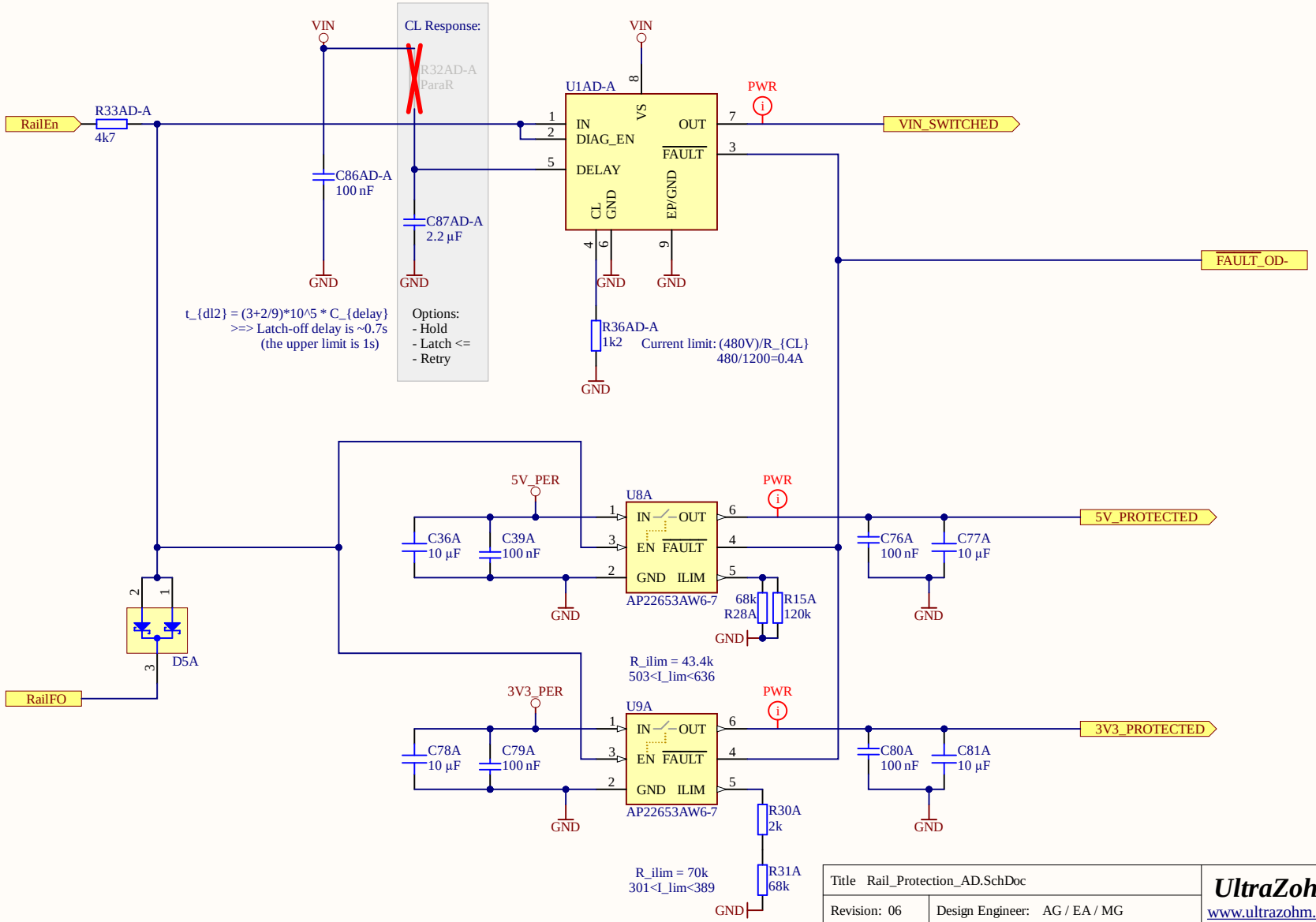


Title Analog_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 17.2 of 62





Title Analog_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 17.3of 62



Title Rail_Protection_AD.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
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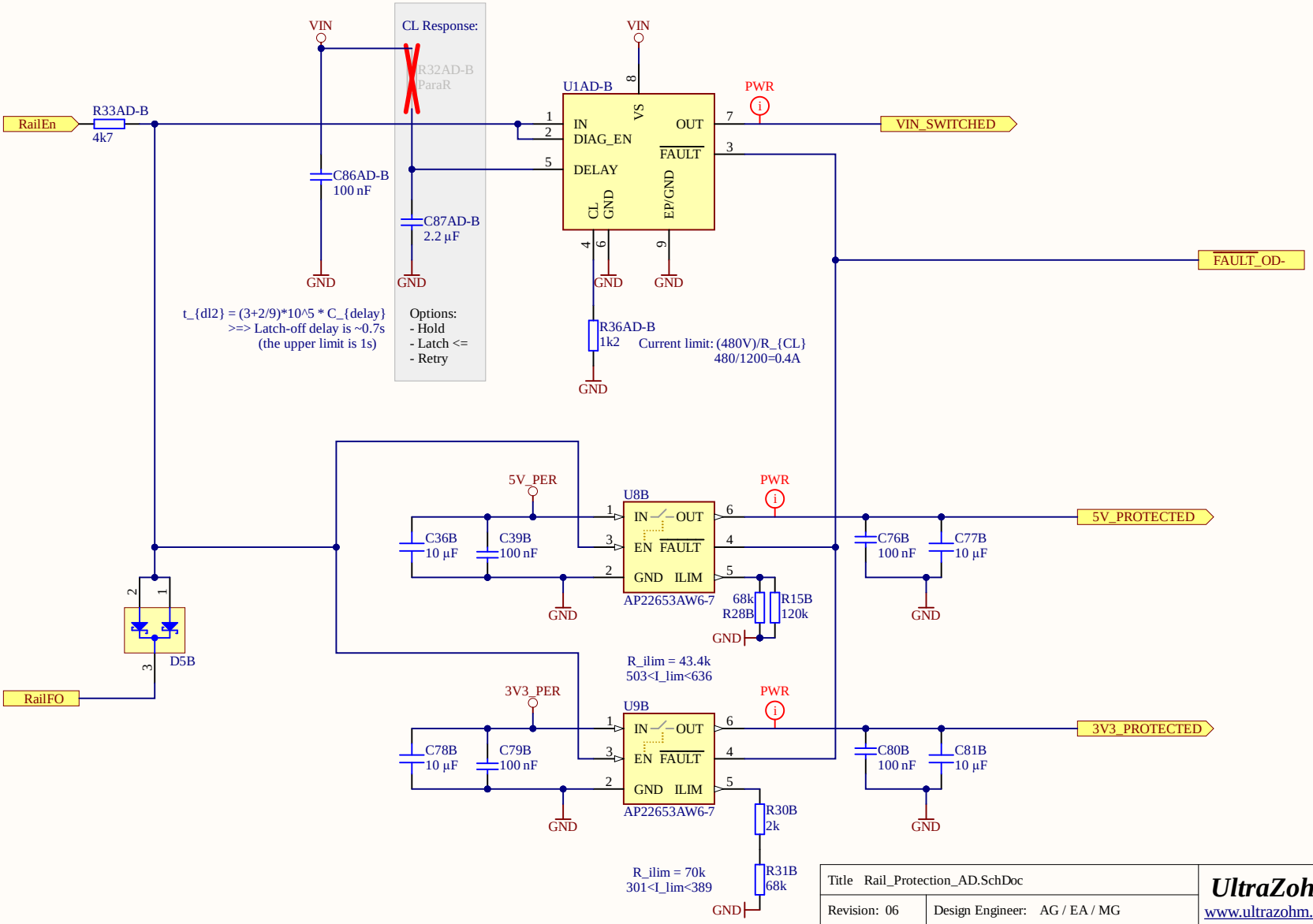

Title Rail_Protection_AD.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025
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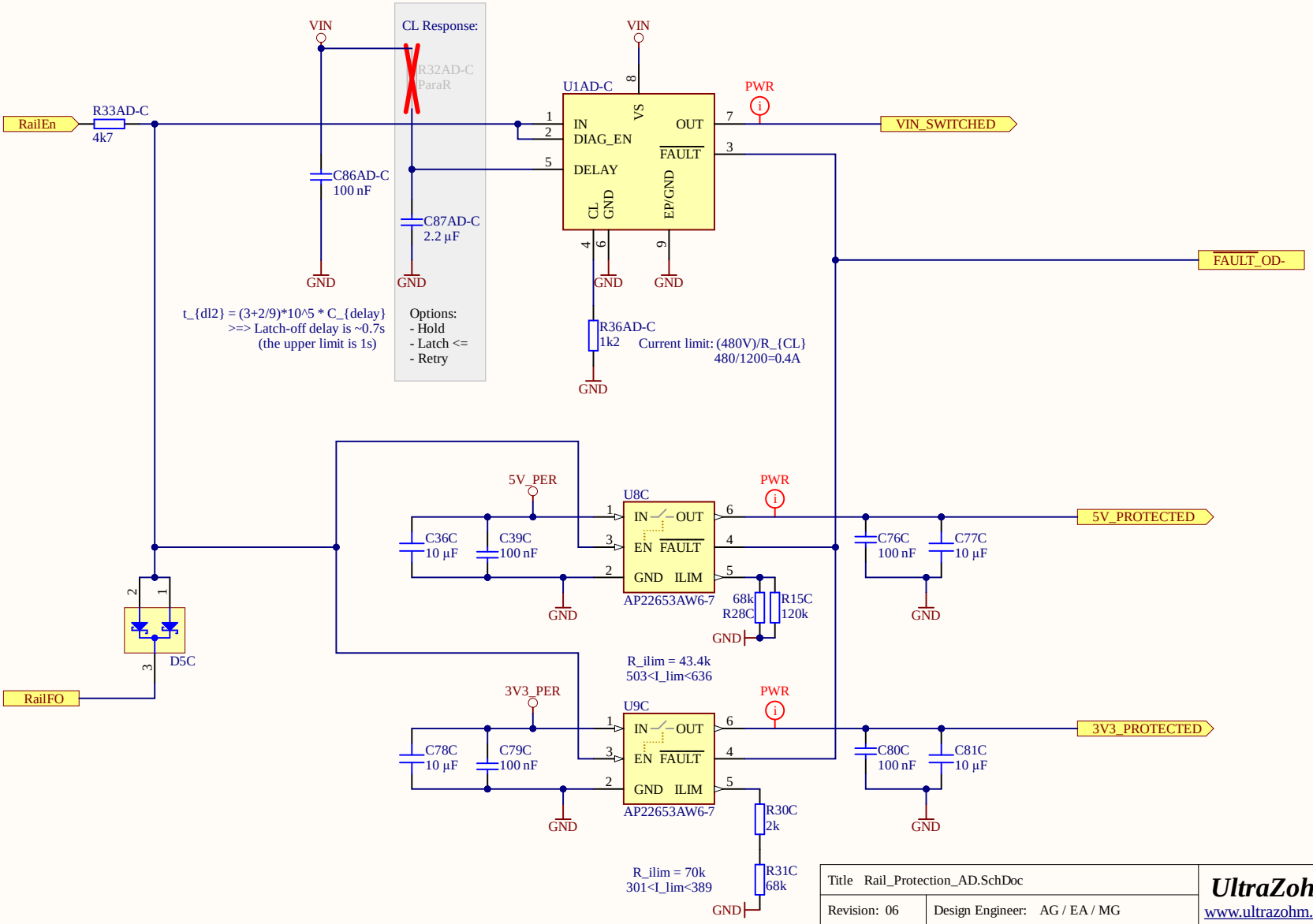

Title	Rail_Protection_AD.SchDoc	UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
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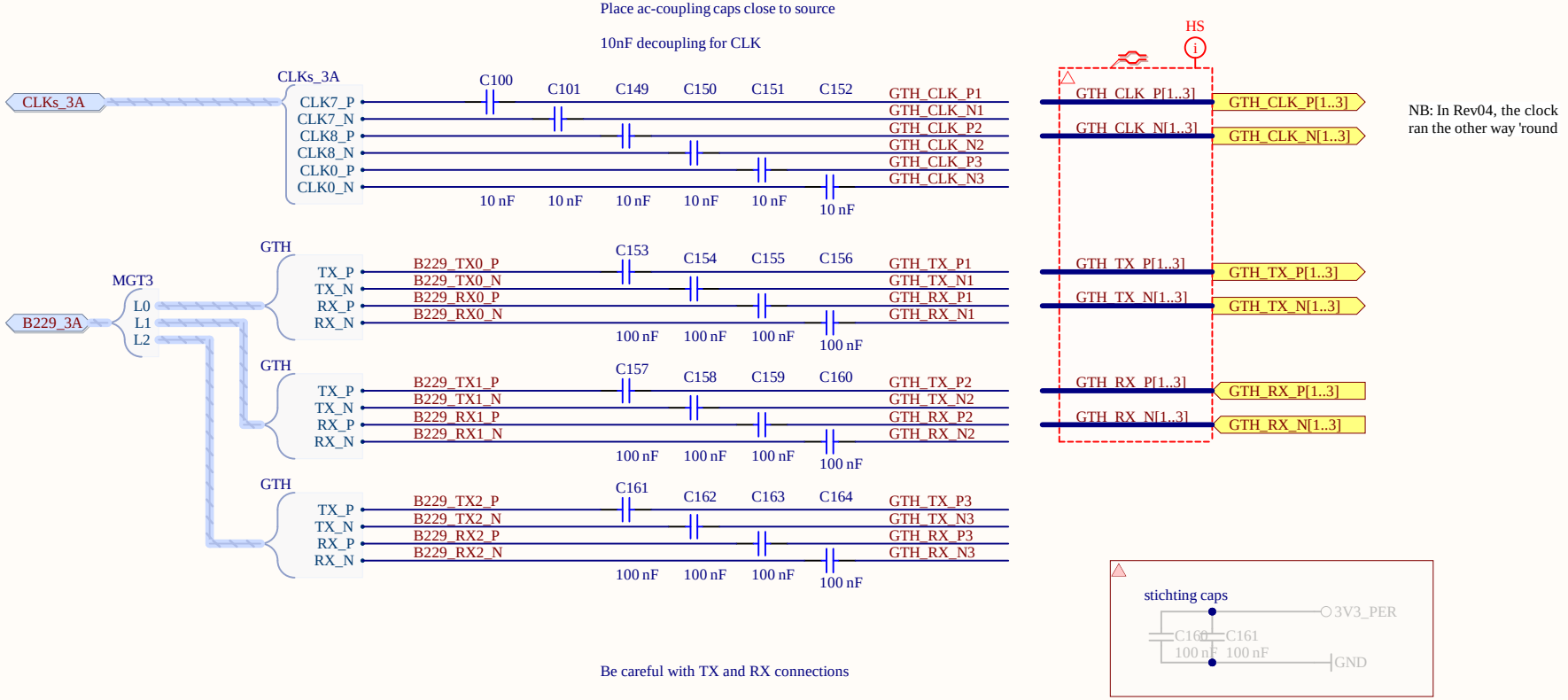
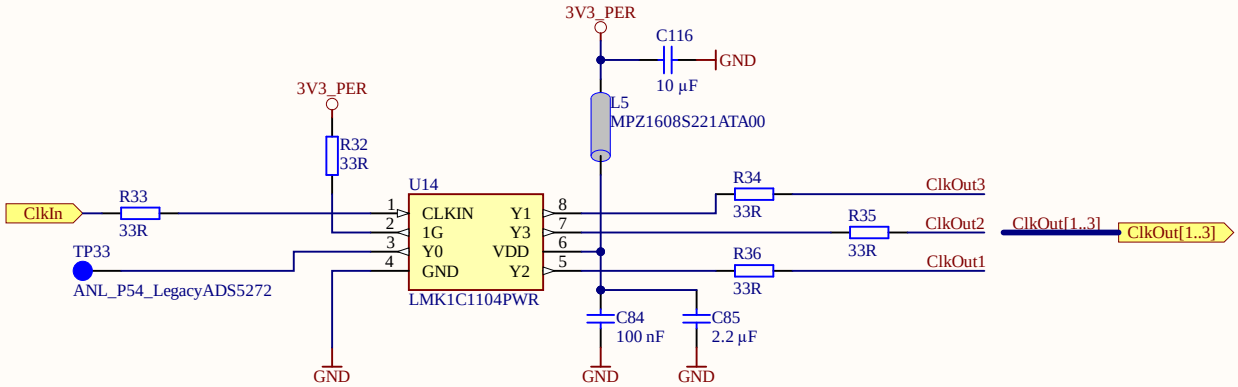


Title GTH.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 06	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 18 of 62	



Title ANL_P54_Buffer.SchDoc		**UltraZohm**	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
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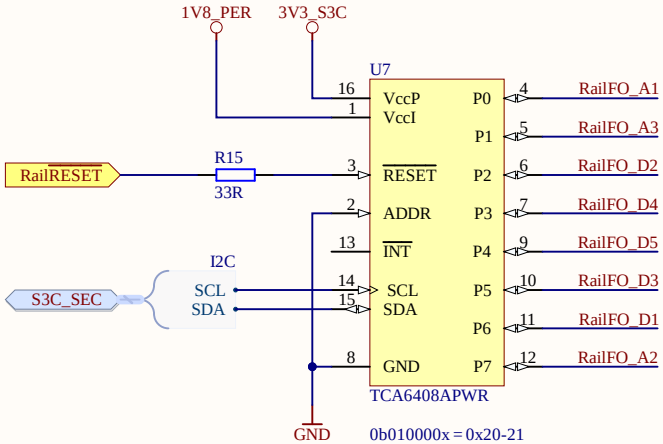

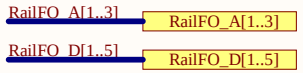

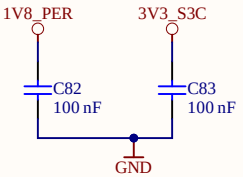

Title Rail_Shutdown_AD.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
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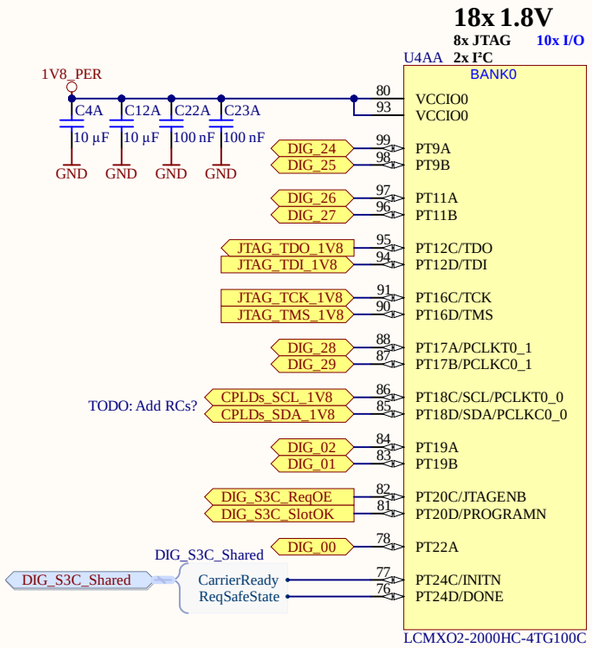

Title	Digital_Interface.SchDoc
Revision: 06	Design Engineer: AG / EA / MG
Project: UZ_CarrierBoard.PrjPcb	

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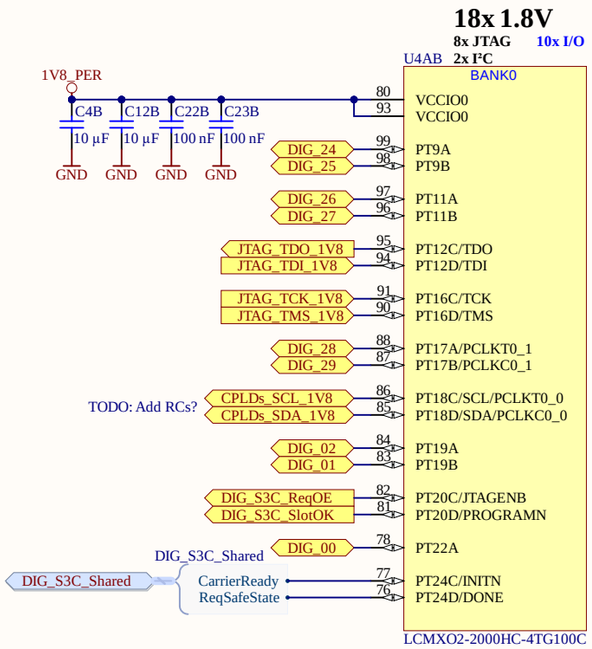

Title	Digital_Interface.SchDoc
Revision: 06	Design Engineer: AG / EA / MG
Project: UZ_CarrierBoard.PrjPcb	

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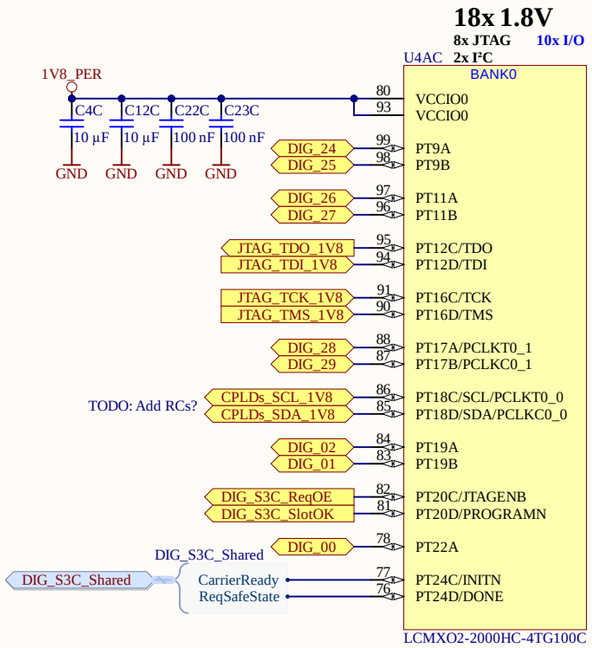

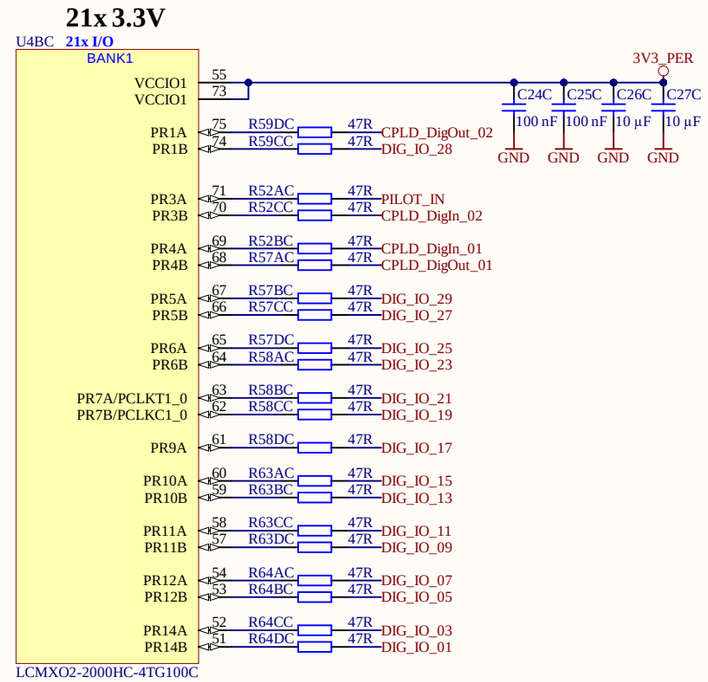

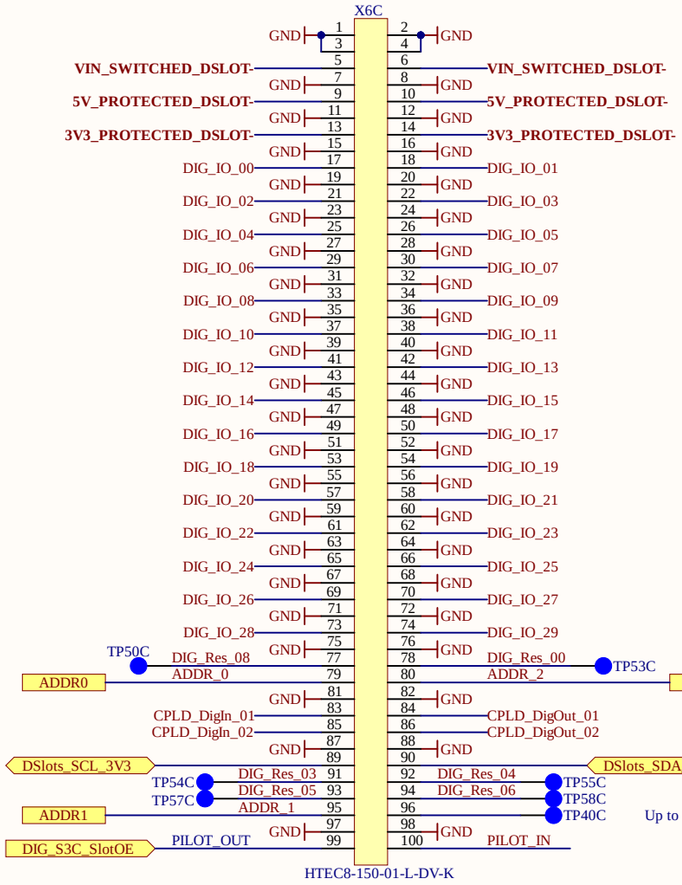

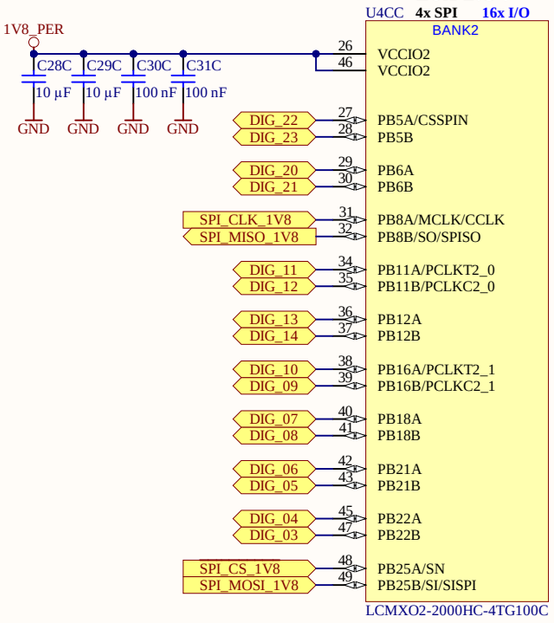

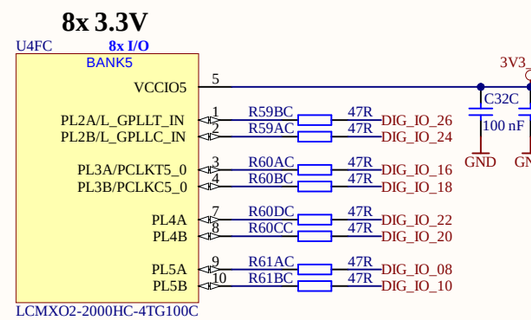

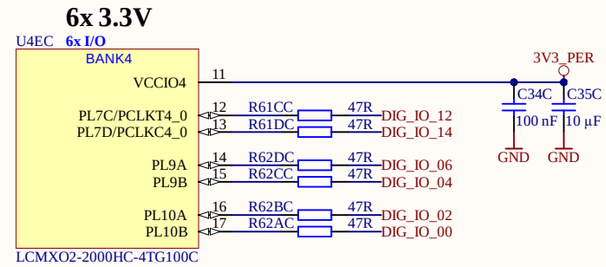

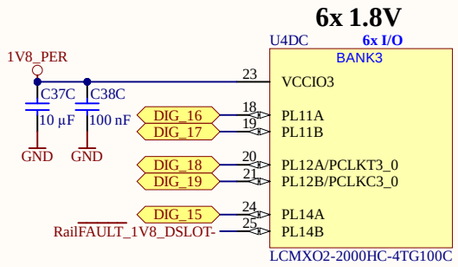

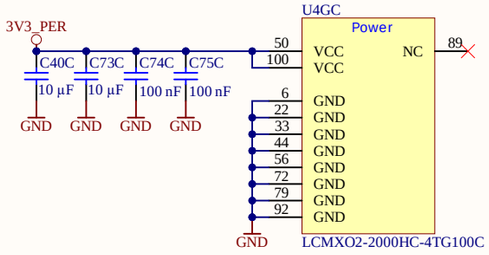

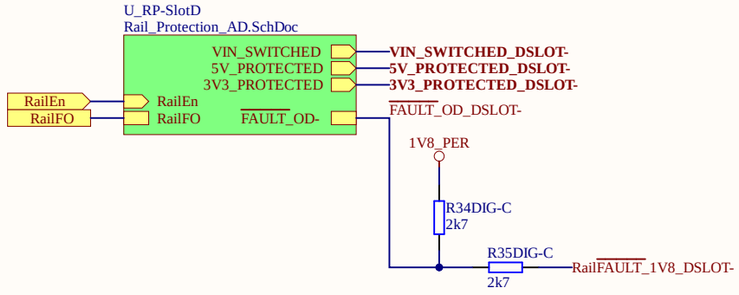

Title Digital_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	Date: 31/07/2025
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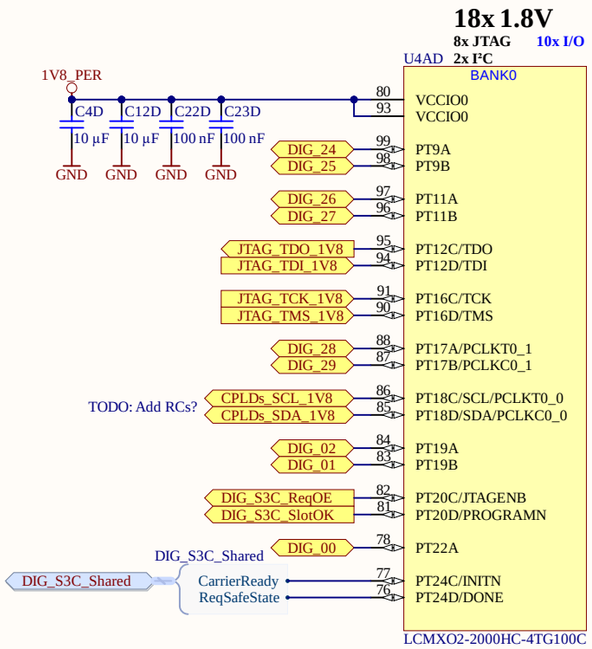
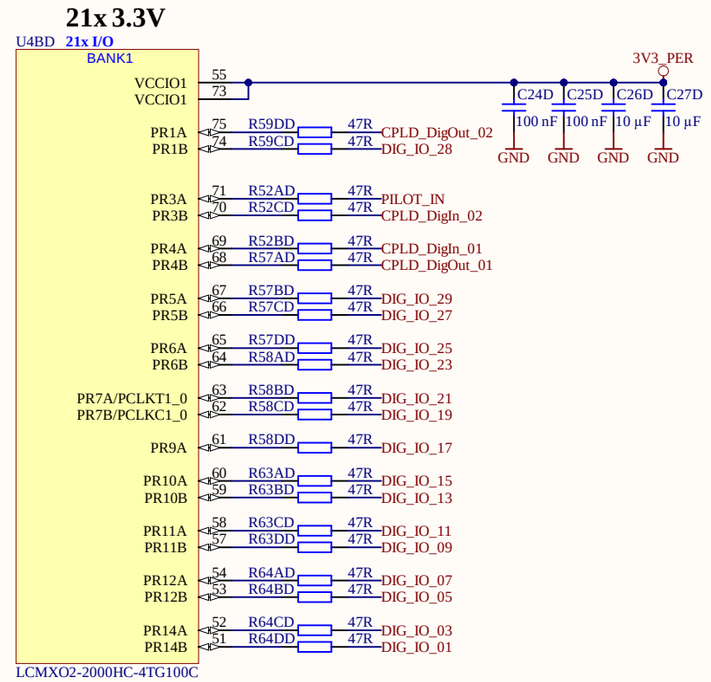
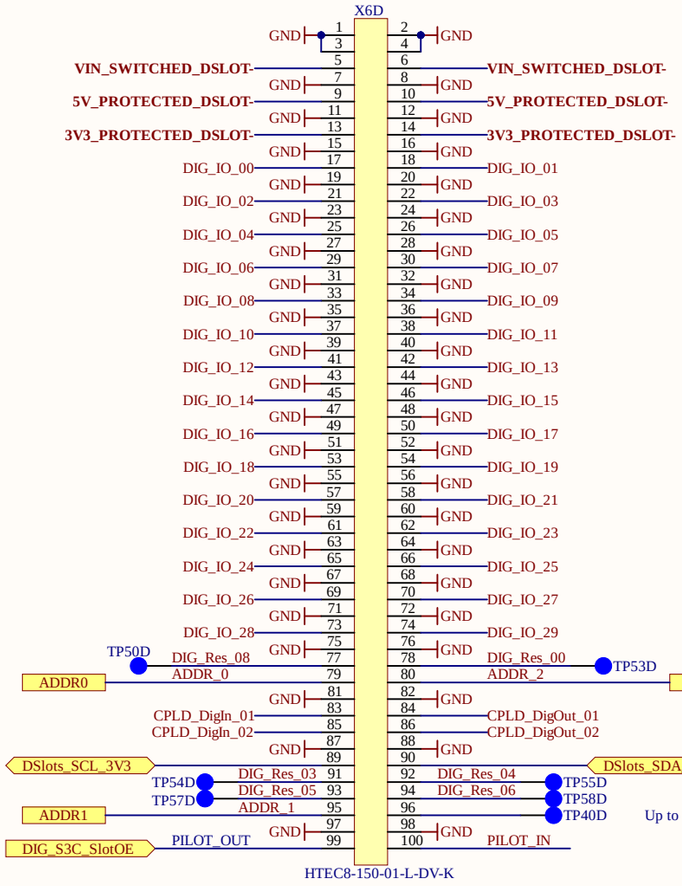
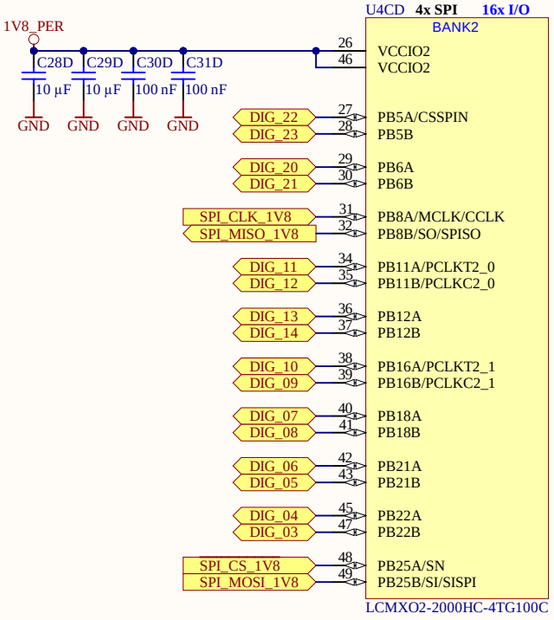
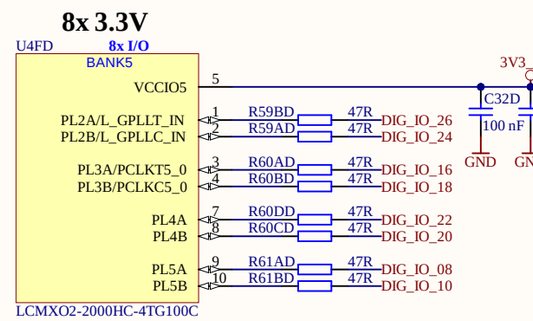
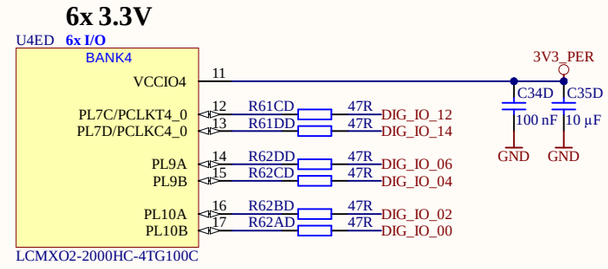


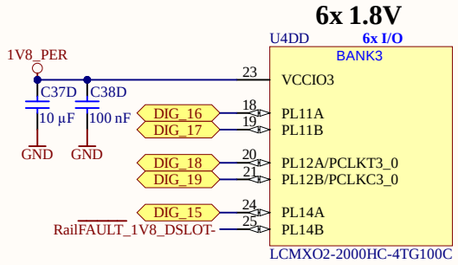


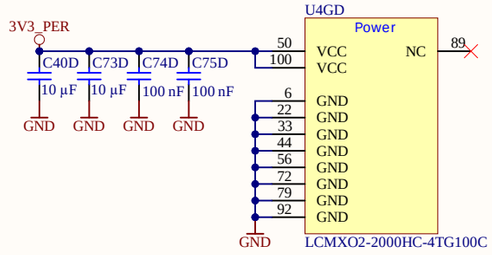


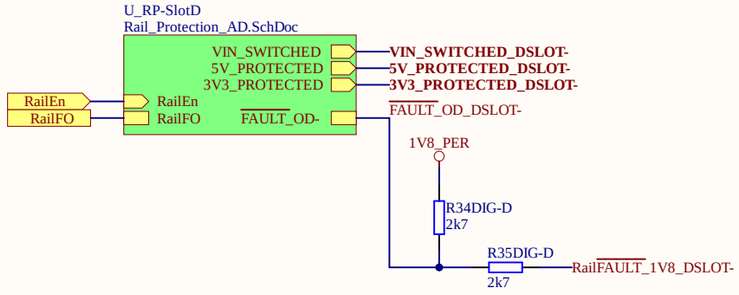




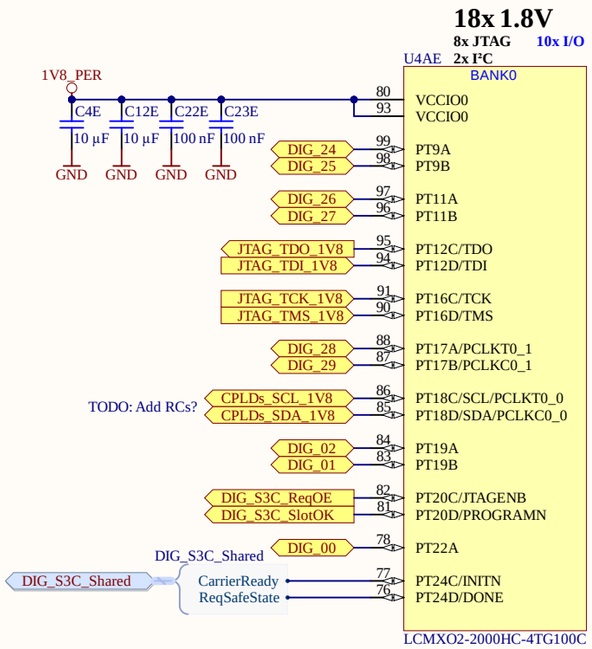


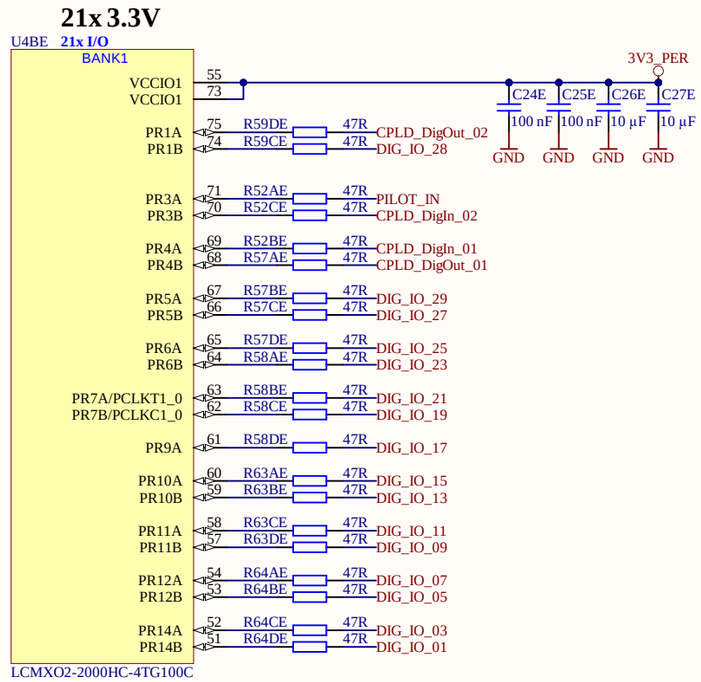


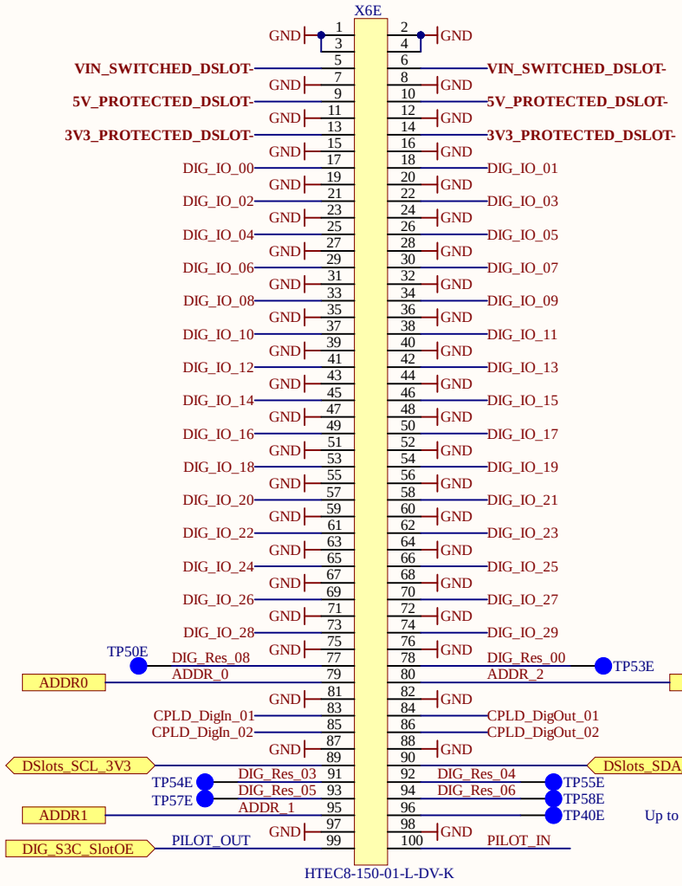


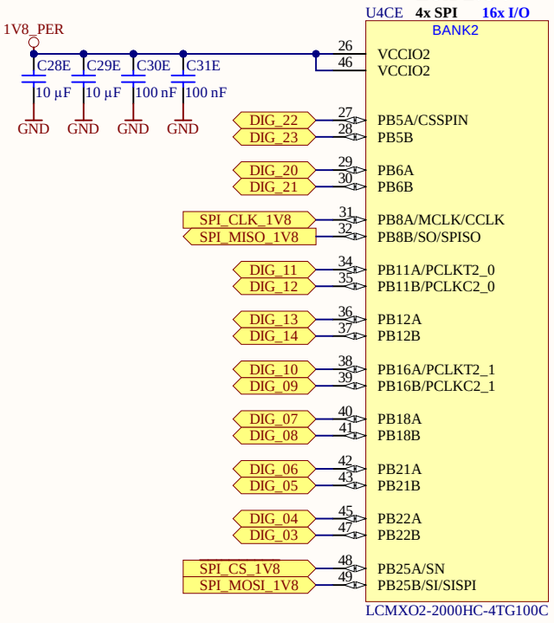


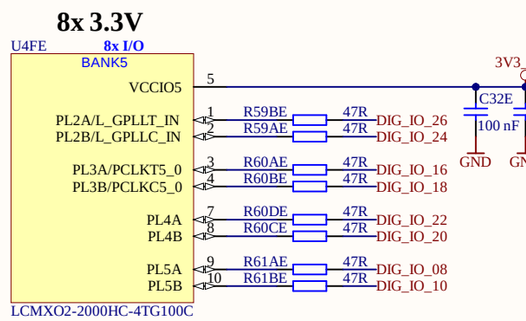
Title Digital_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	Date: 31/07/2025
Project: UZ_CarrierBoard.PrjPcb		Sheet 21.4of 62

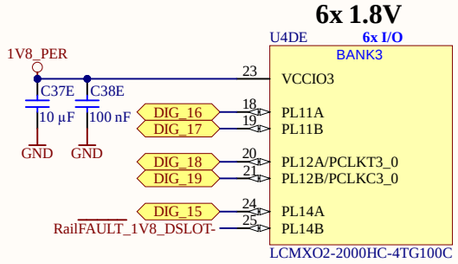


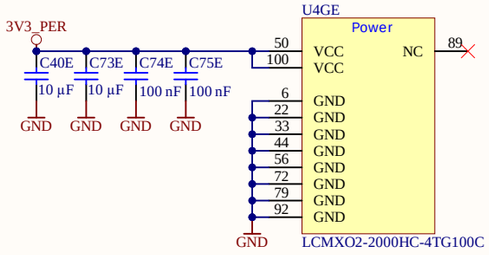


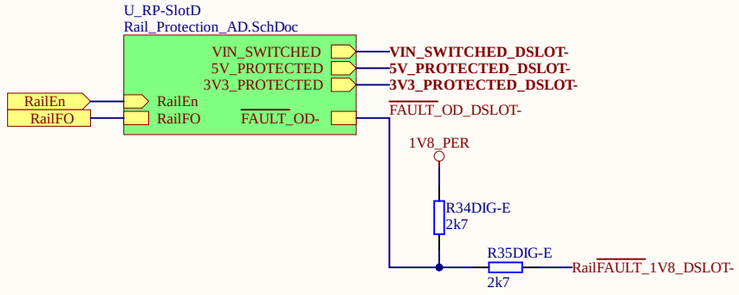




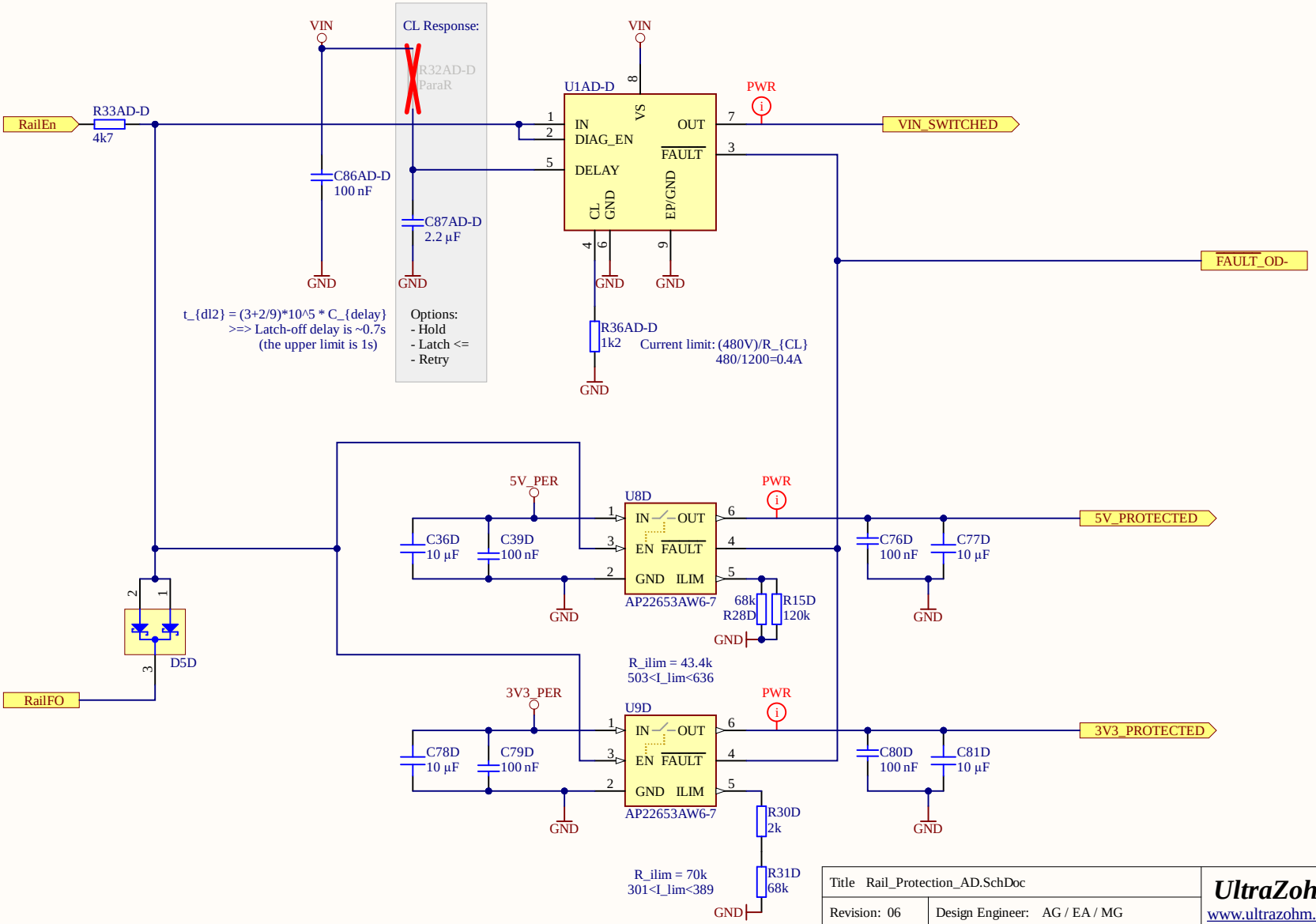




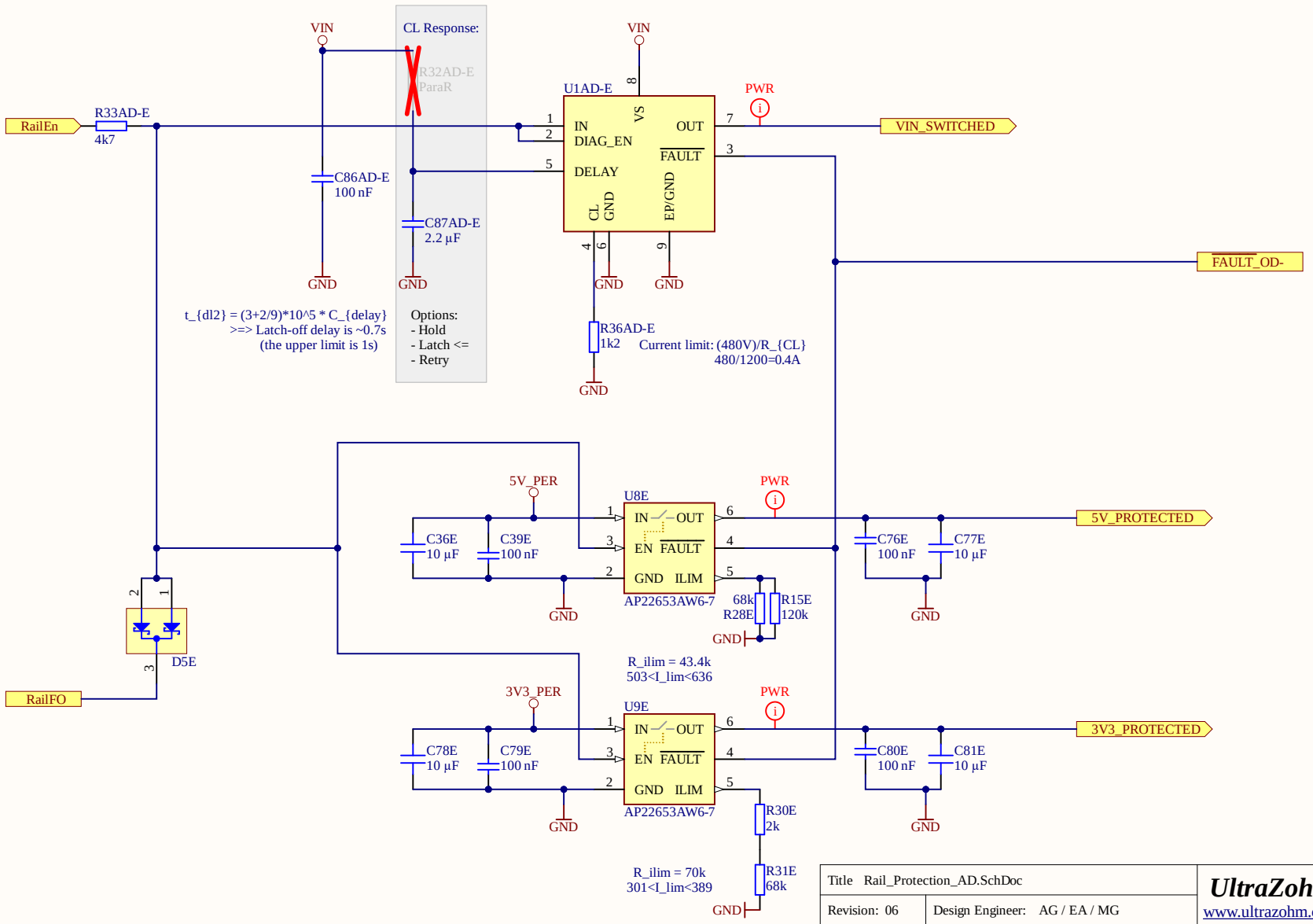




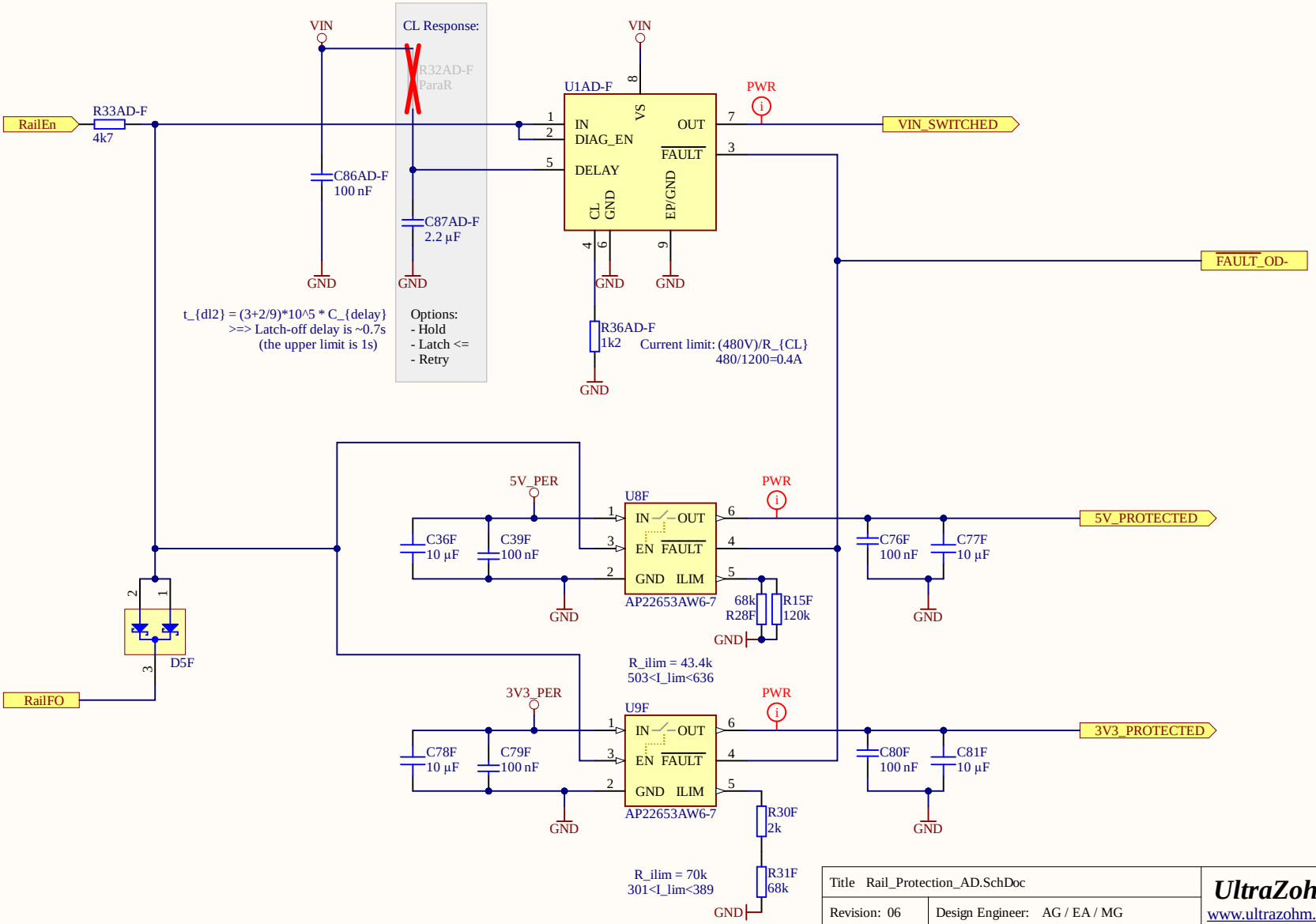
Title Digital_Interface.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	Date: 31/07/2025
Project: UZ_CarrierBoard.PrjPcb		Sheet 21.5of 62



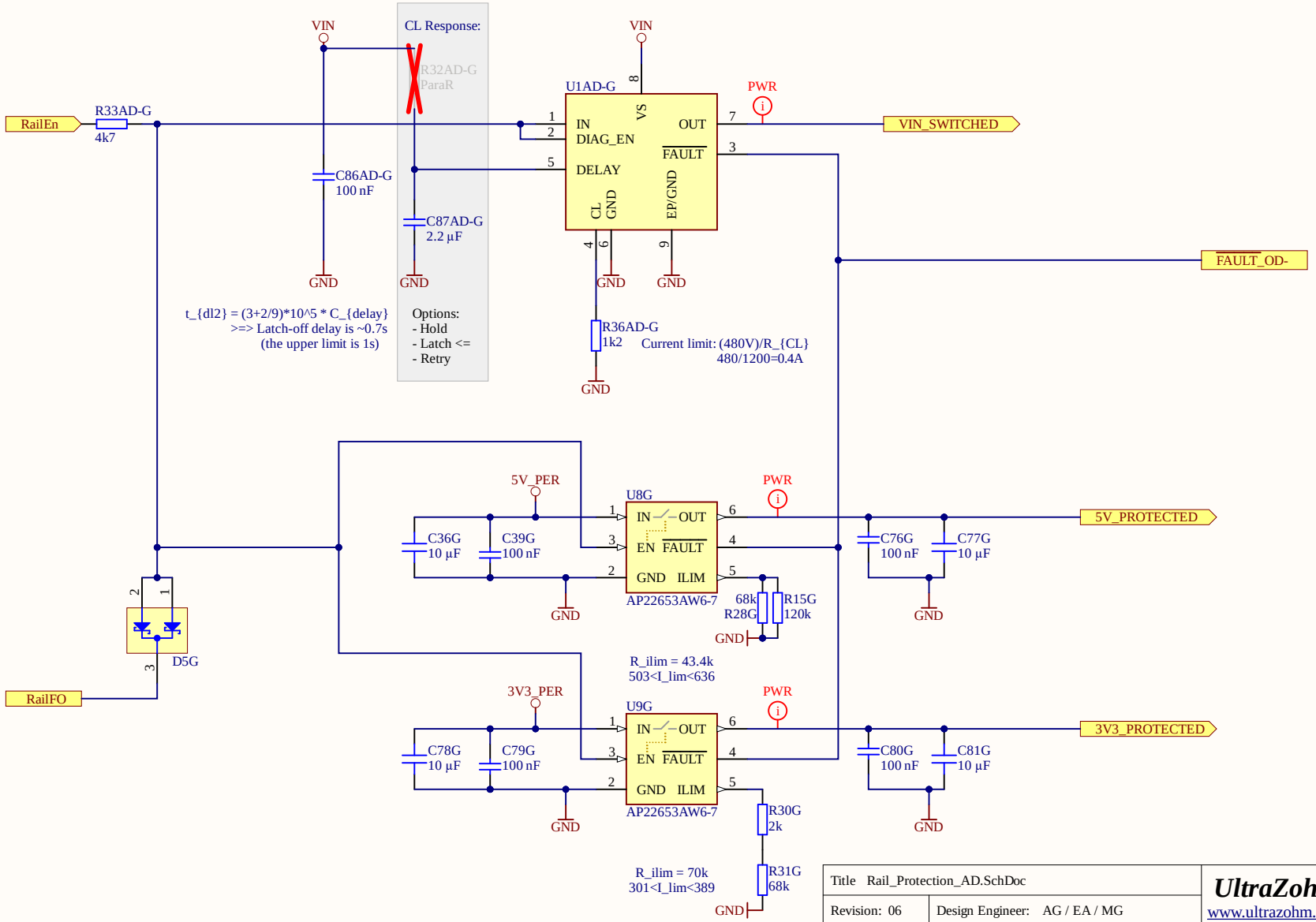
Title Rail_Protection_AD.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 21 of 62	



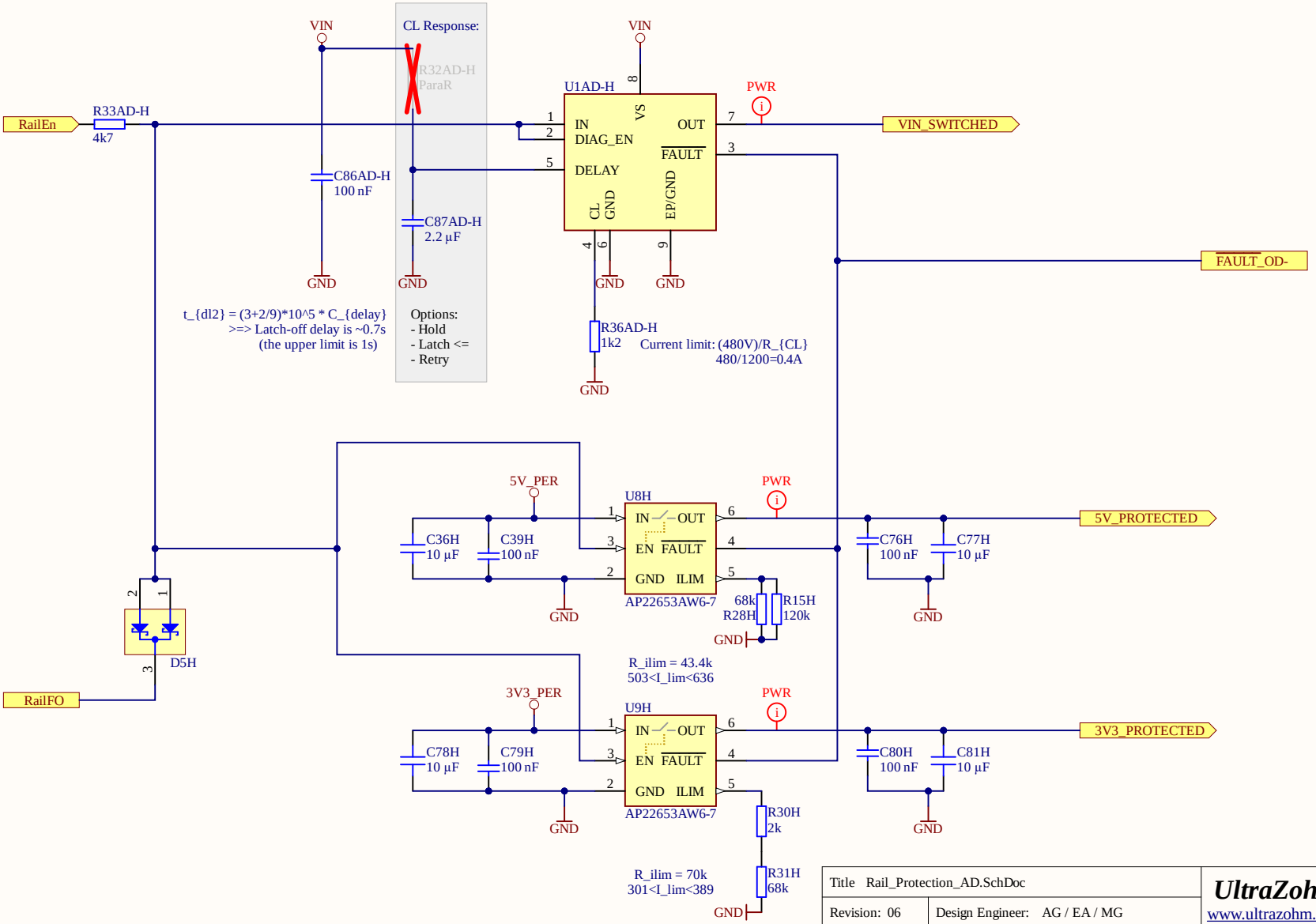
Title Rail_Protection_AD.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	Date: 31/07/2025
Project: UZ_CarrierBoard.PrjPcb		Sheet 21 of 62



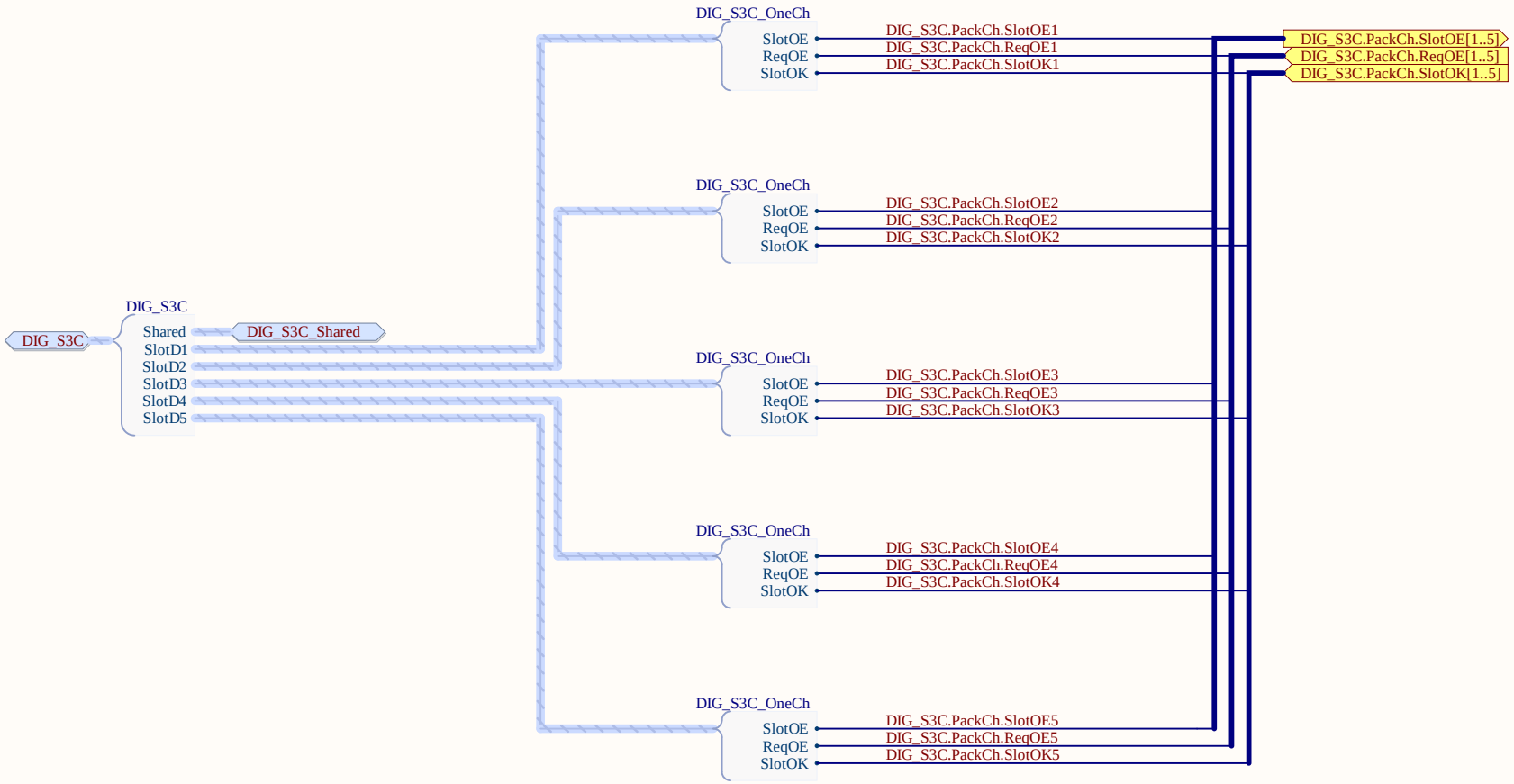
Title Rail_Protection_AD.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 21.3of 62	



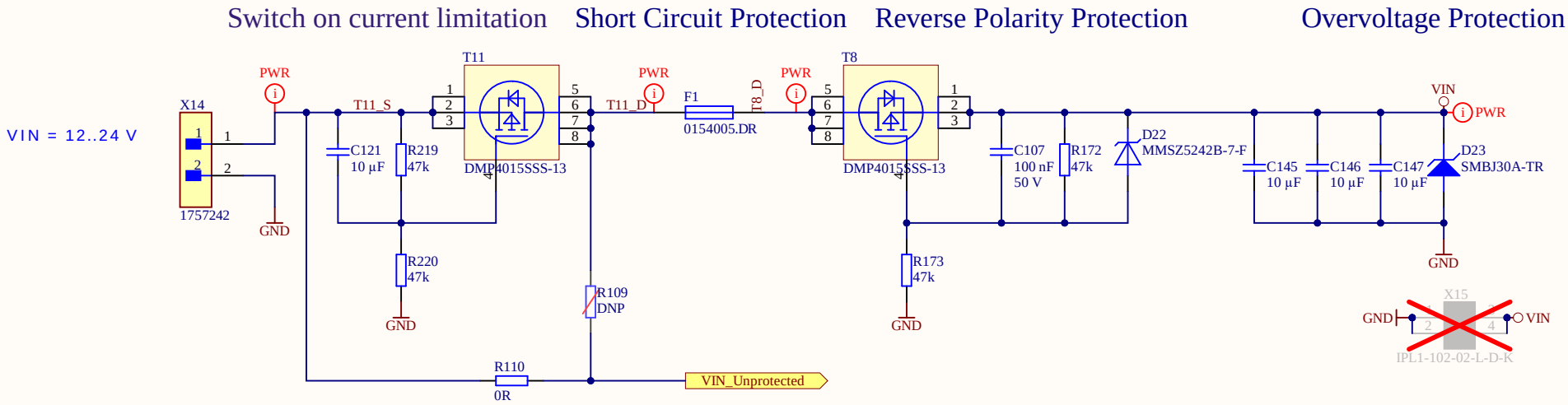
Title	Rail_Protection_AD.SchDoc	UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 21.4of 62	



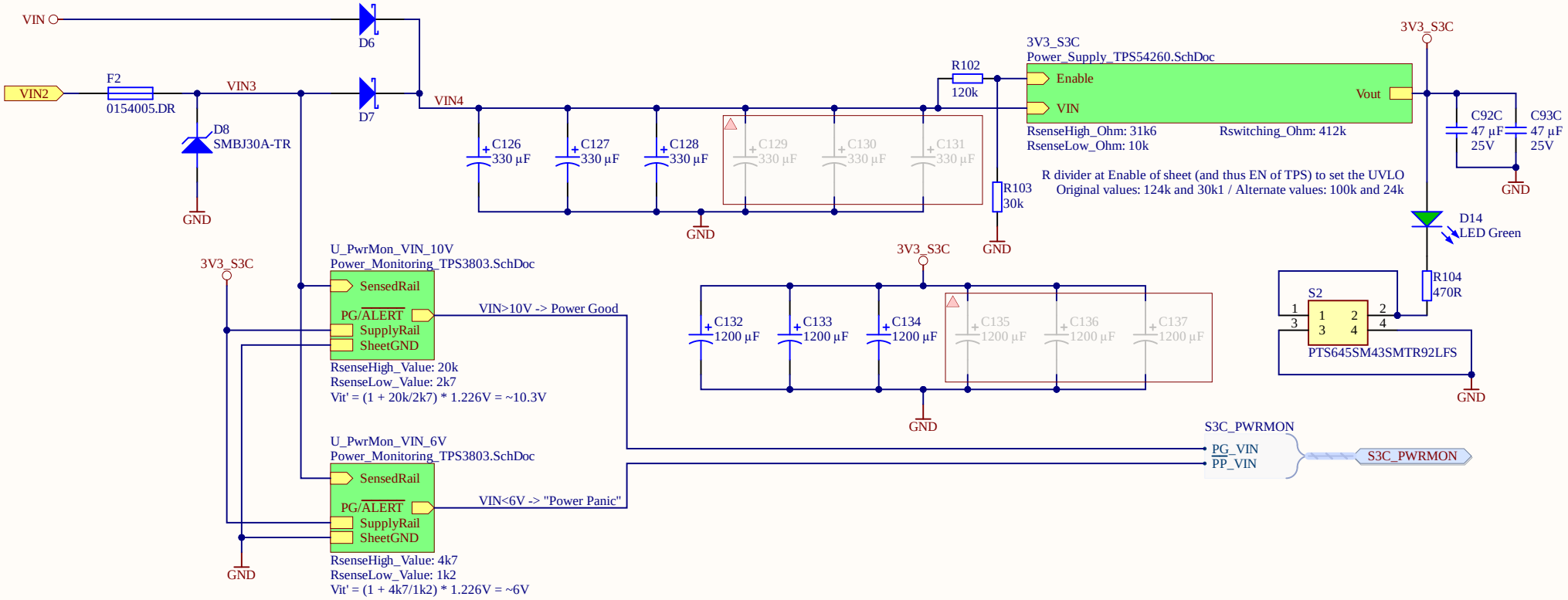
Title Rail_Protection_AD.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 21.5of 62	



Title DIG_S3C_MultiChannelFunnel.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 22 of 62	

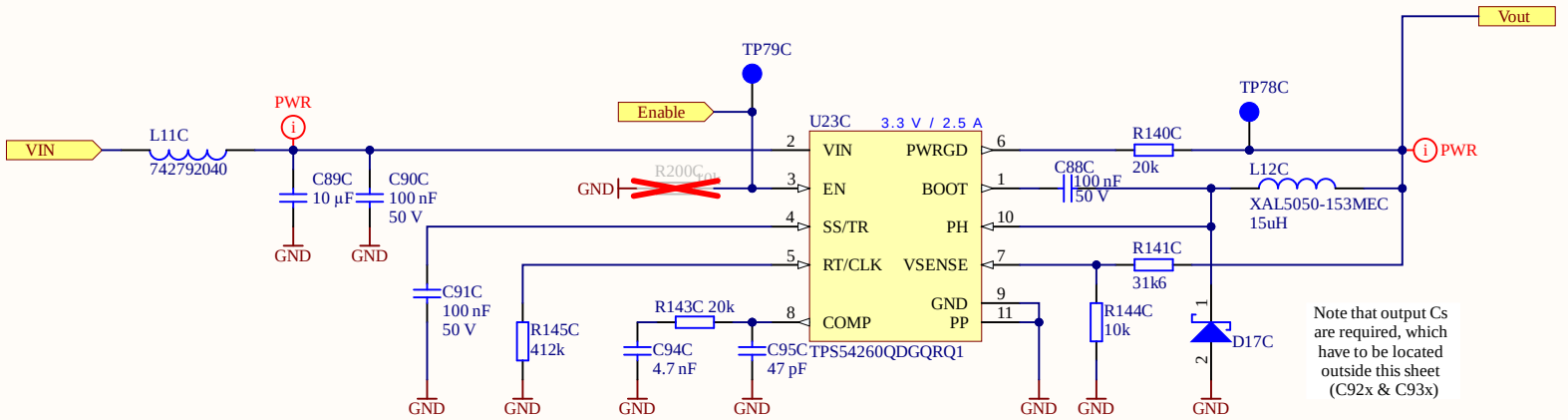


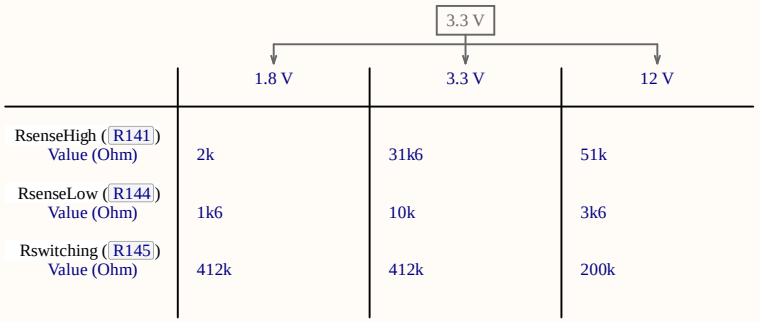
Title Power_Supply_Input.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 06	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 23 of 62	



Additional sources:
- Co-monitor VIN (by wire-OR-ing to S3C_PWRMON)
- LMZ/... (U10/U11/U12) : No integrated PG output
- TPS (U23 A to C): PWRGD (OD, up to 5.5V), valid from 1.5/3V input voltage
- SoM
  - PG_PL (aka PG_Module): OD, on-SoM pull-up to PL_DCIN (aka 3V3_MOD)
  - Some more PG_* signals
  - PLL_LOLn

Title S3C_SupplyAndMonitoring.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	Date: 31/07/2025
Project: UZ_CarrierBoard.PrjPcb		Sheet 24 of 62

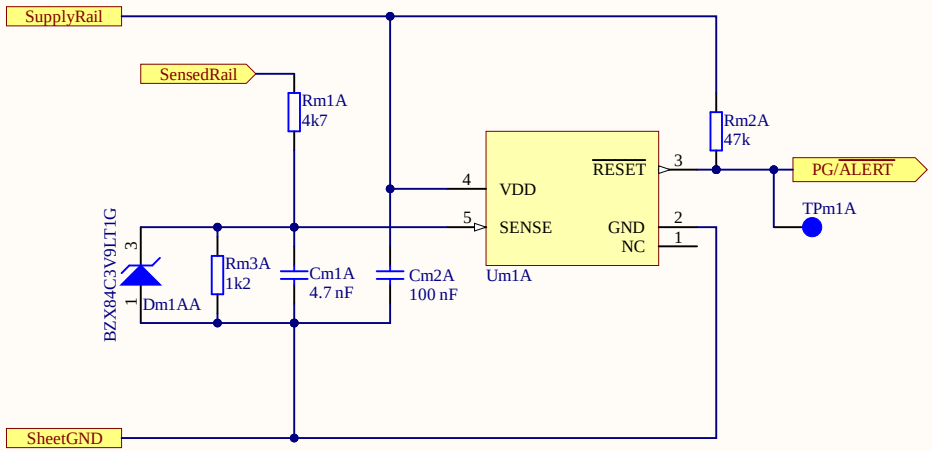




	1.8 V	3.3 V	12 V
RsenseHigh (R141) Value (Ohm)	2k	31k6	51k
RsenseLow (R144) Value (Ohm)	1k6	10k	3k6
Rswitching (R145) Value (Ohm)	412k	412k	200k

NB: No need to set MPN as parameter!

Title Power_Supply_TPS54260.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 25 of 62



Title Power_Monitoring_TPS3803.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
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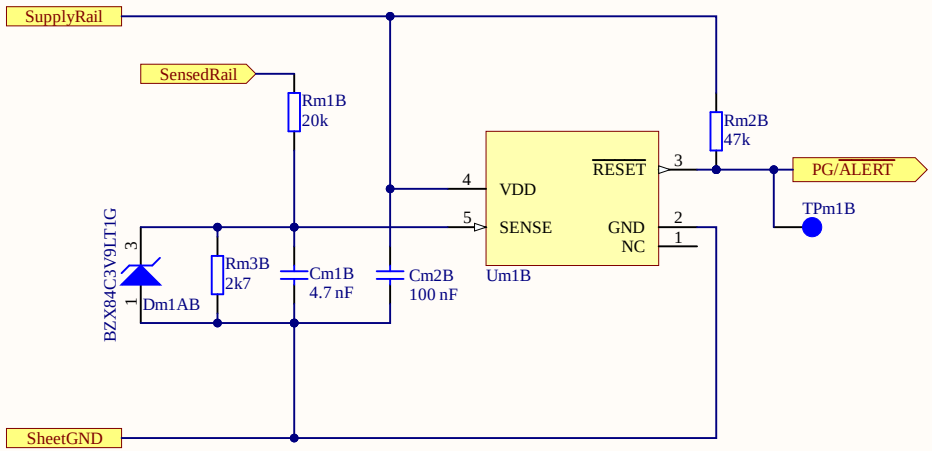

Title Power_Monitoring_TPS3803.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
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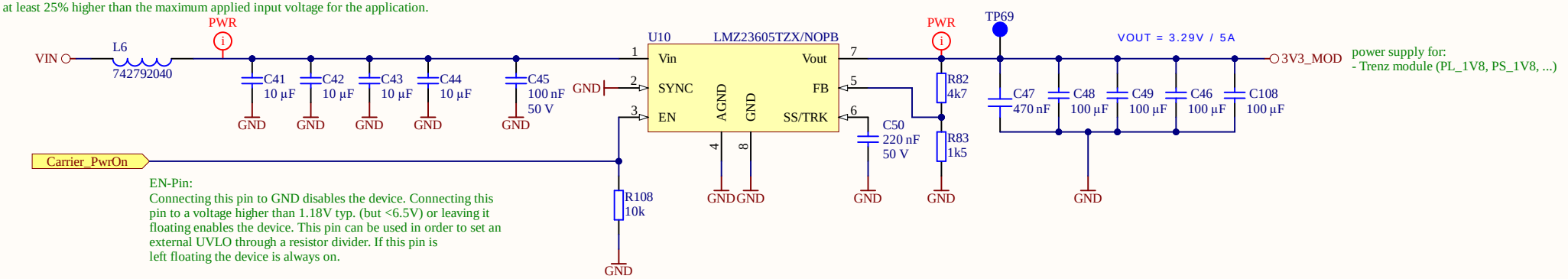
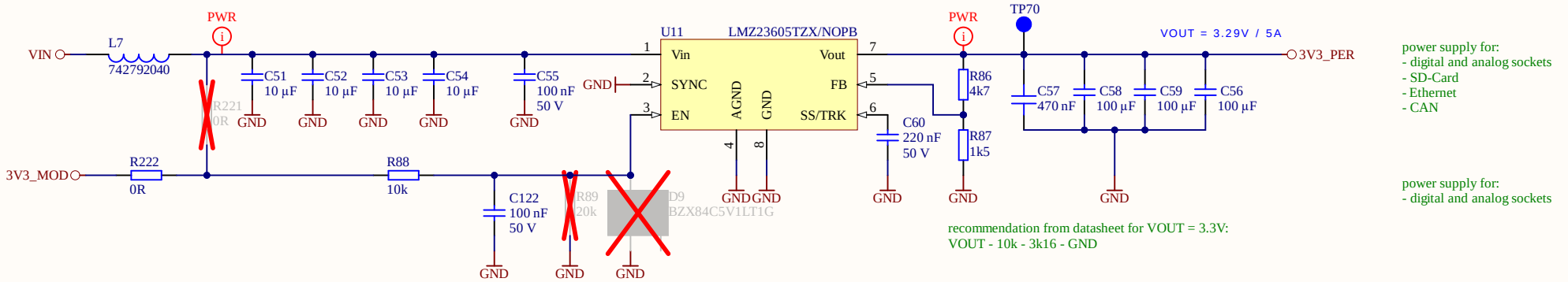
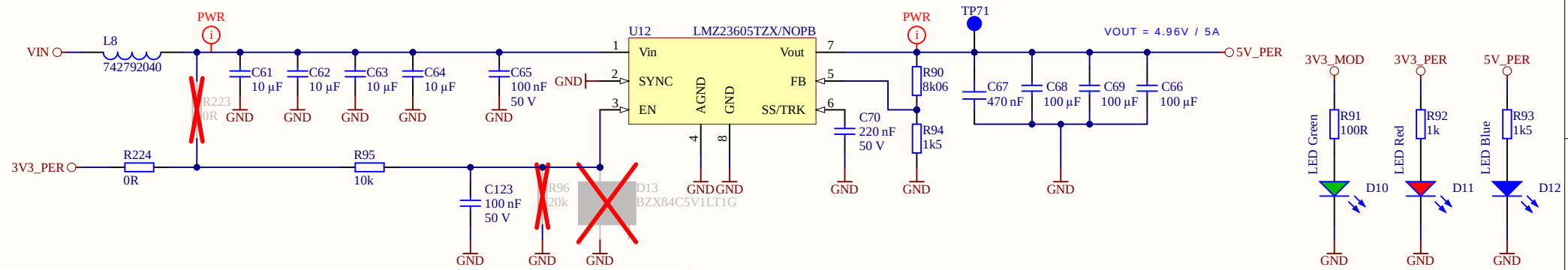
Notes: preferred to use 2x 22µF/50V capacitors at Vin, but this design uses 35V caps due to worse availability at distributors.
Datasheet: recommended minimum input capacitance is 22 µF (including derating) ceramic with voltage rating
at least 25% higher than the maximum applied input voltage for the application.

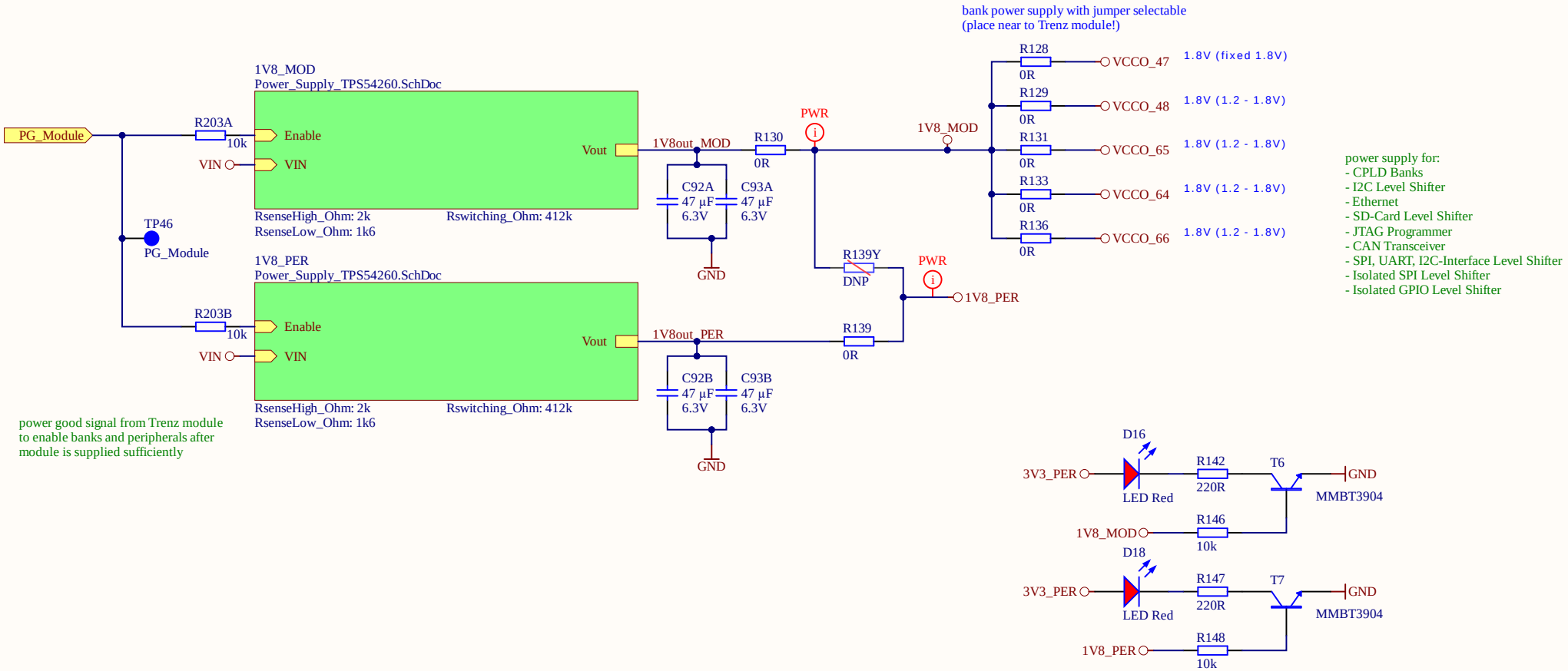




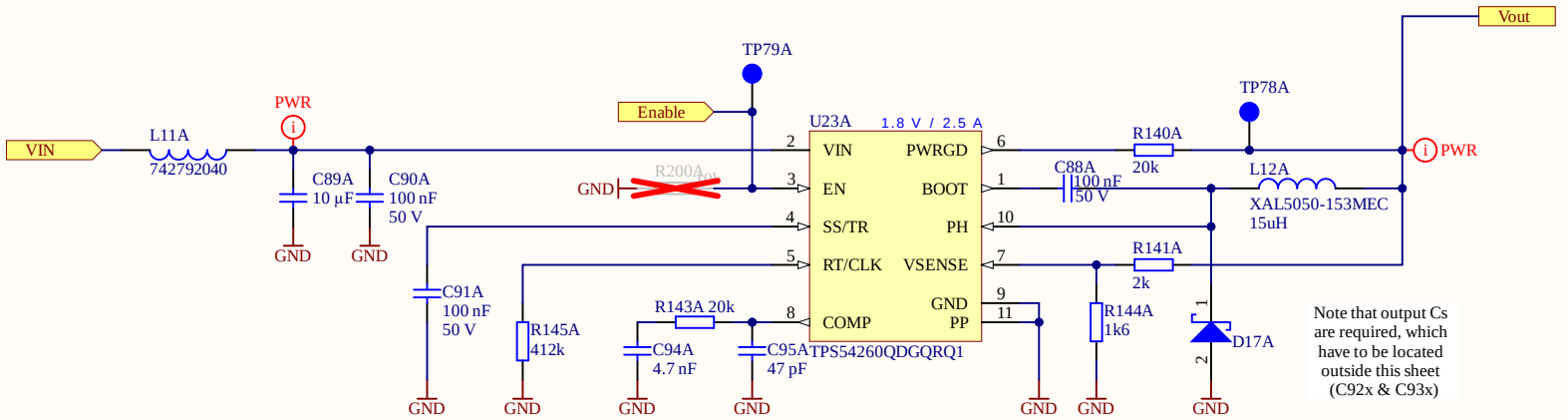


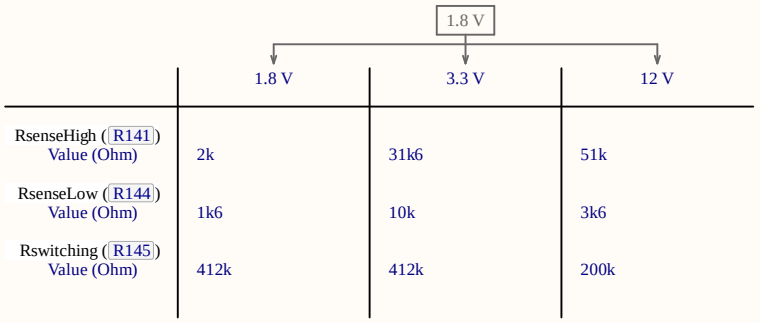
The delay time between the power supplies U10 U11 and U12 is determined by R88 C122 R95 and C123.
The delay time can be estimated as follows: t_on = -tau * ln(1-(U_en/U_max))
tau = R*C
U_en = 1,27V
U_max = output voltage of prior stage (e.g. 3V3)
Since the input current of the EN pin is about 21µA the real dealy time is a bit longer than the calculated value. With the values above there is a delay of about 5ms,

Title Power_Supply_1.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 27 of 62	



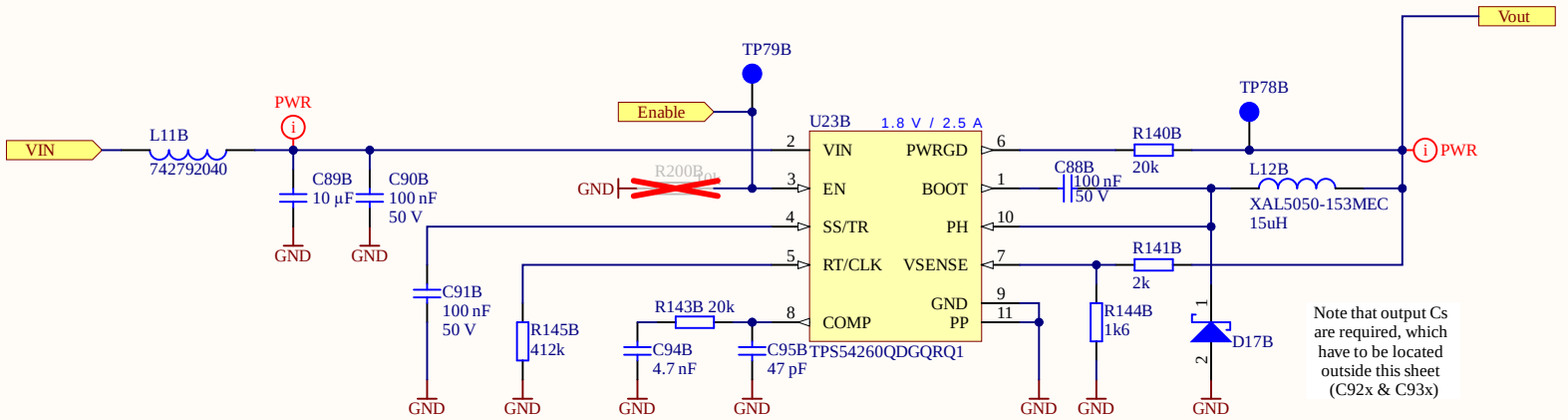
Title Power_Supply_2.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 28 of 62	

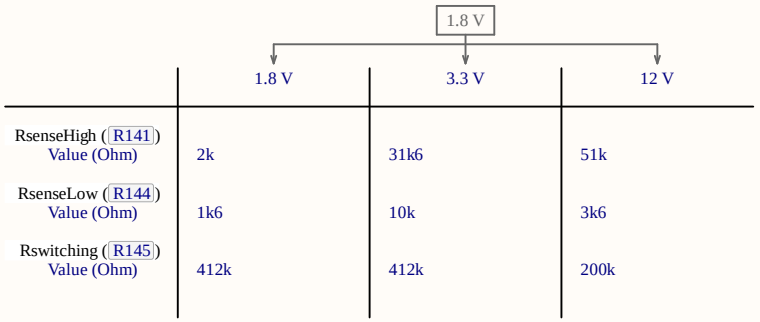




NB: No need to set MPN as parameter!

Title	Power_Supply_TPS54260.SchDoc	UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 28.1of 62	





NB: No need to set MPN as parameter!

Title	Power_Supply_TPS54260.SchDoc		
Revision: 06	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb			

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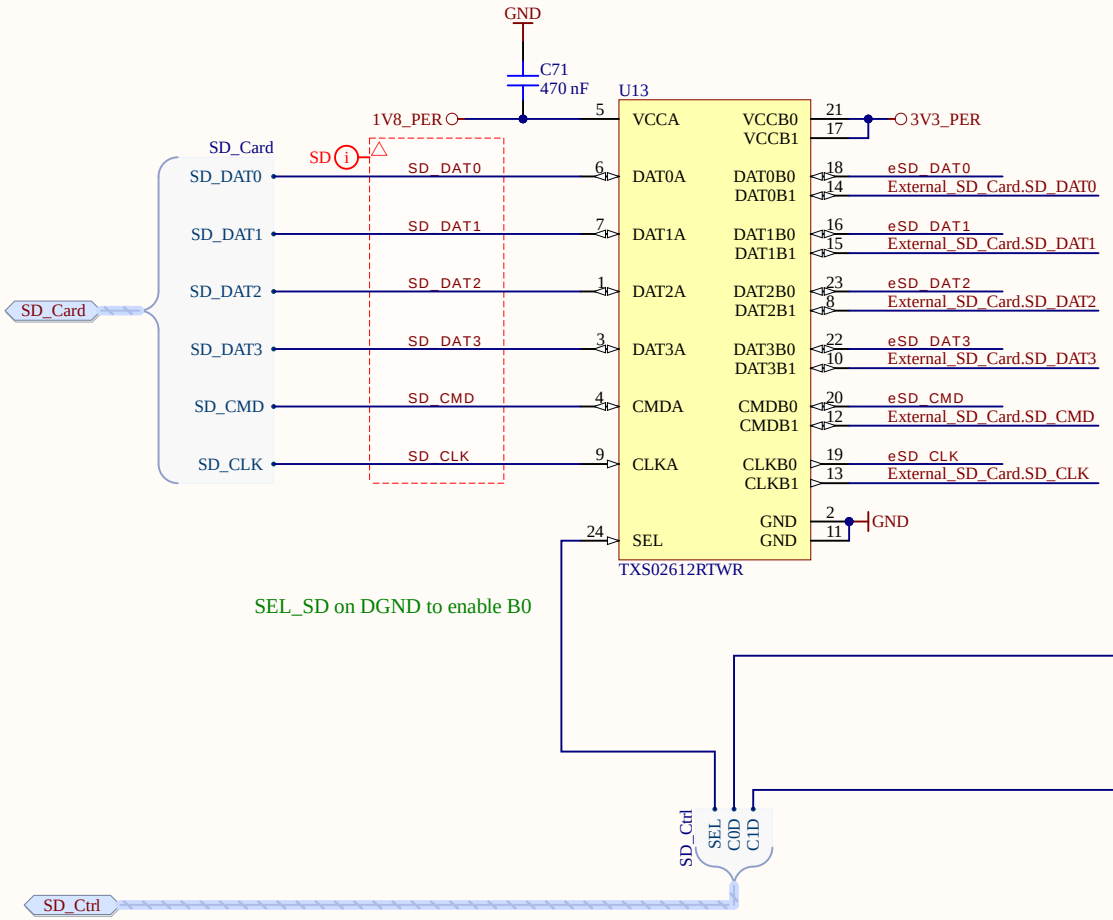
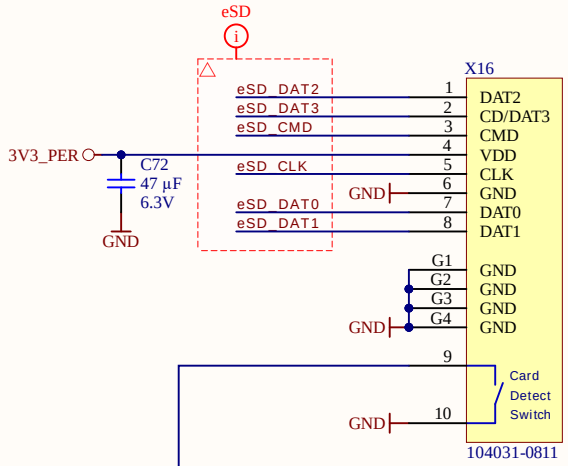
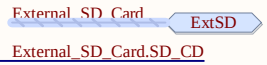
www.ultrazohm.com
Date: 31/07/2025
Sheet 28.2 of 62

Bidirectional Level Shifting 1.8V to 3.3V



SD Card Connector

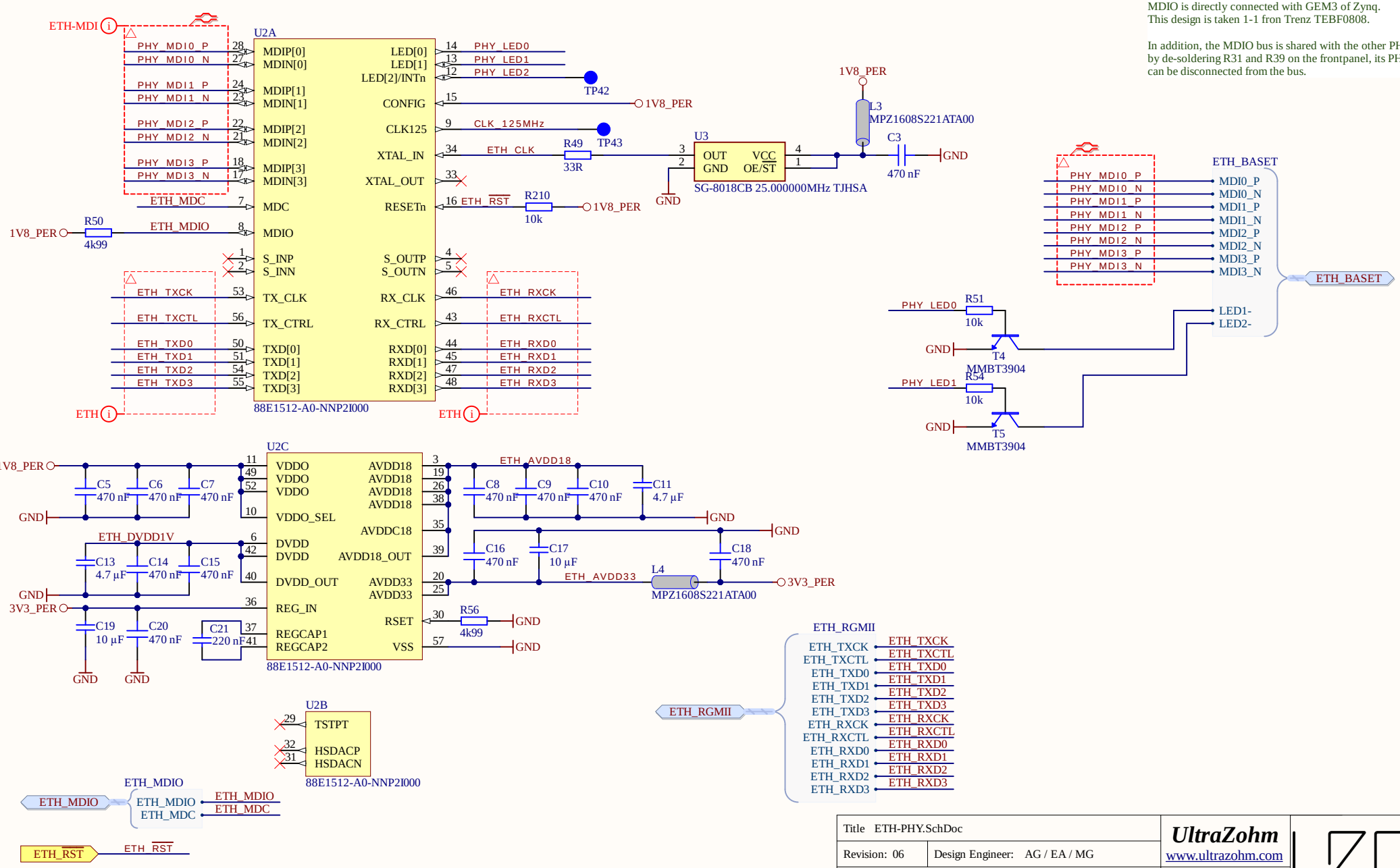


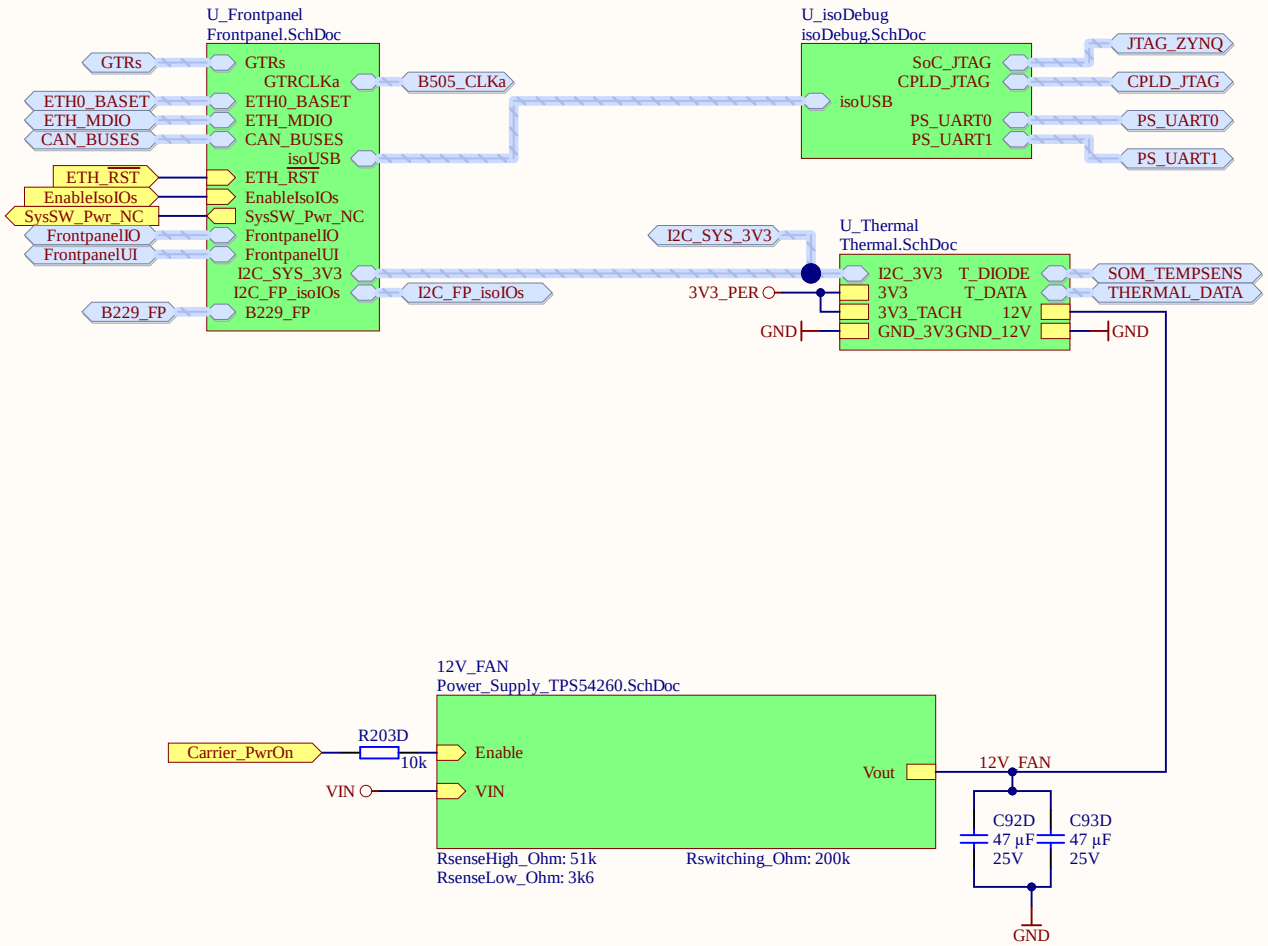


Title SD_Card.SchDoc		**UltraZohm**	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 29 of 62	

Config Pin 15 is high, so PHY address = 1
PHY is connected to GEM3 of Zynq via RGMII
MDIO is directly connected with GEM3 of Zynq.
This design is taken 1-1 fron Trenz TEBF0808.

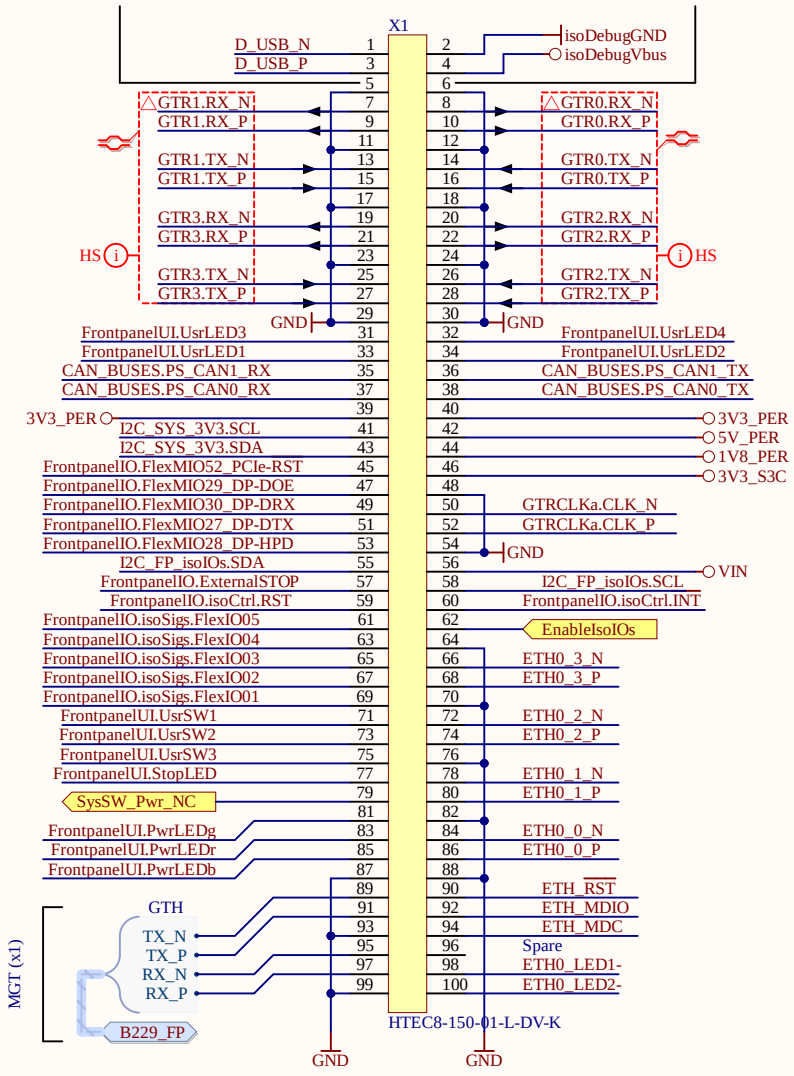
In addition, the MDIO bus is shared with the other PHY; by de-soldering R31 and R39 on the frontpanel, its PHY can be disconnected from the bus.





Title User_Connectors.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 31 of 62	

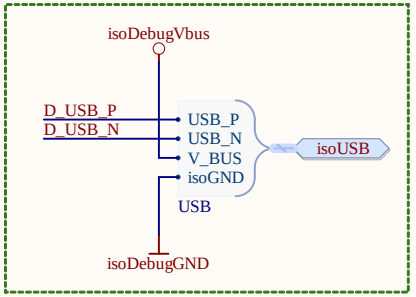
NB: VIN is always active - i.e., even if the system is (soft-)switched off

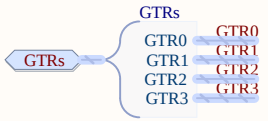


S3C_BUTCOM <=> 3V3_S3C

I2C_SYS_3V3 I2C_SYS_3V3

FrontpanelUI FrontpanelUI





GTRCLKa GTRCLKa

ETH_RST ETH_RST

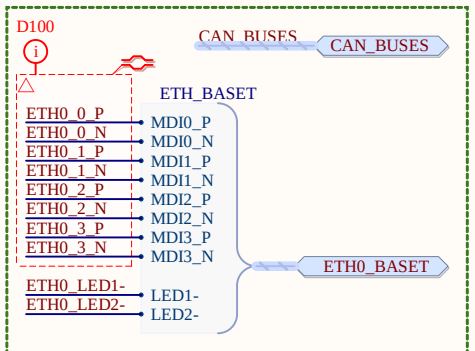
I2C_FP_isoIOs I2C_FP_isoIOs

FrontpanelIO FrontpanelIO

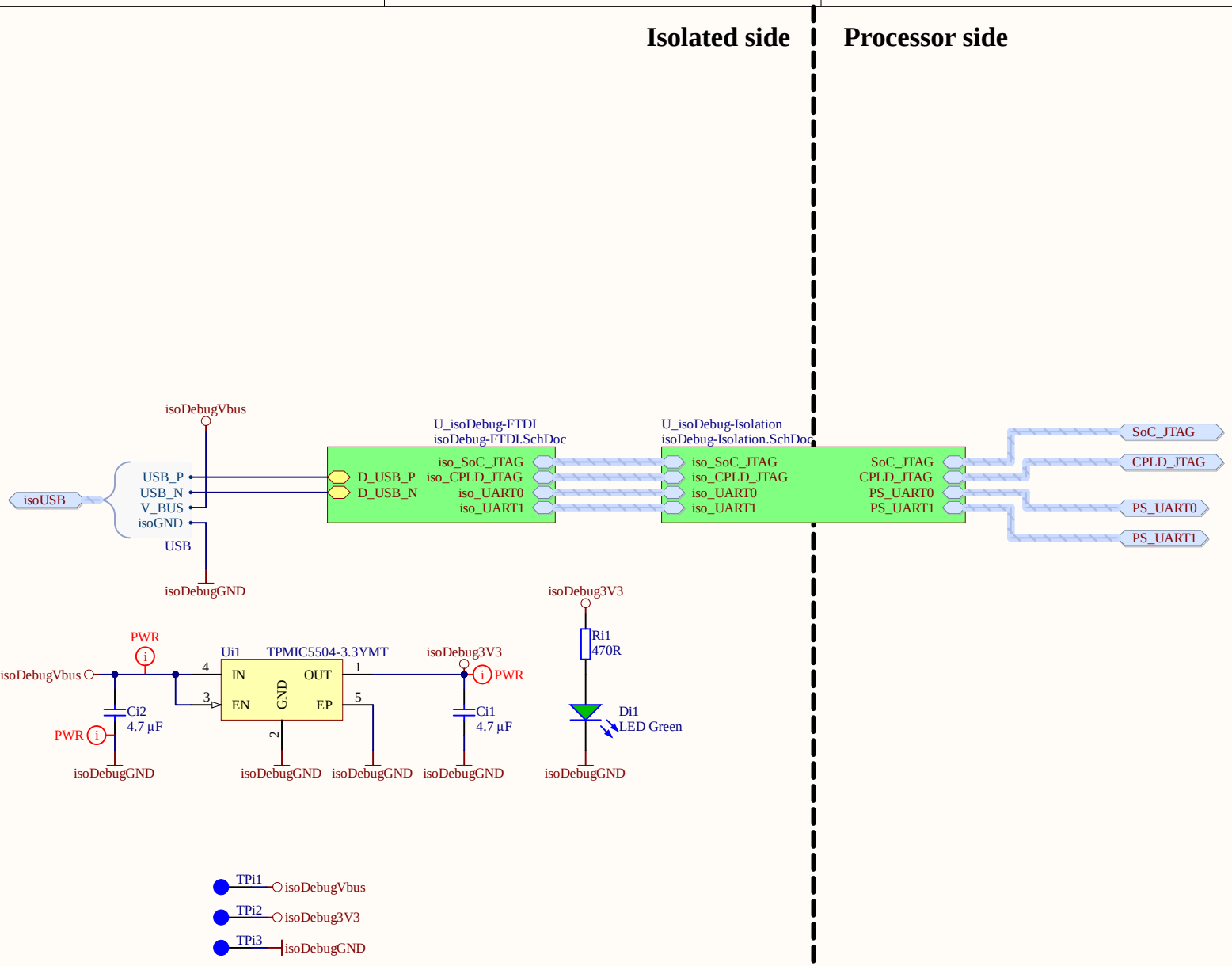
Also includes the following FlexMIOs from/to the S³C:

- PCIe: FrontpanelIO.FlexMIO52_PCIe-R\S\T\
- DP
  - FrontpanelIO.FlexMIO27_DP-DTX
  - FrontpanelIO.FlexMIO28_DP-HPD
  - FrontpanelIO.FlexMIO29_DP-DOE
  - FrontpanelIO.FlexMIO30_DP-DRX

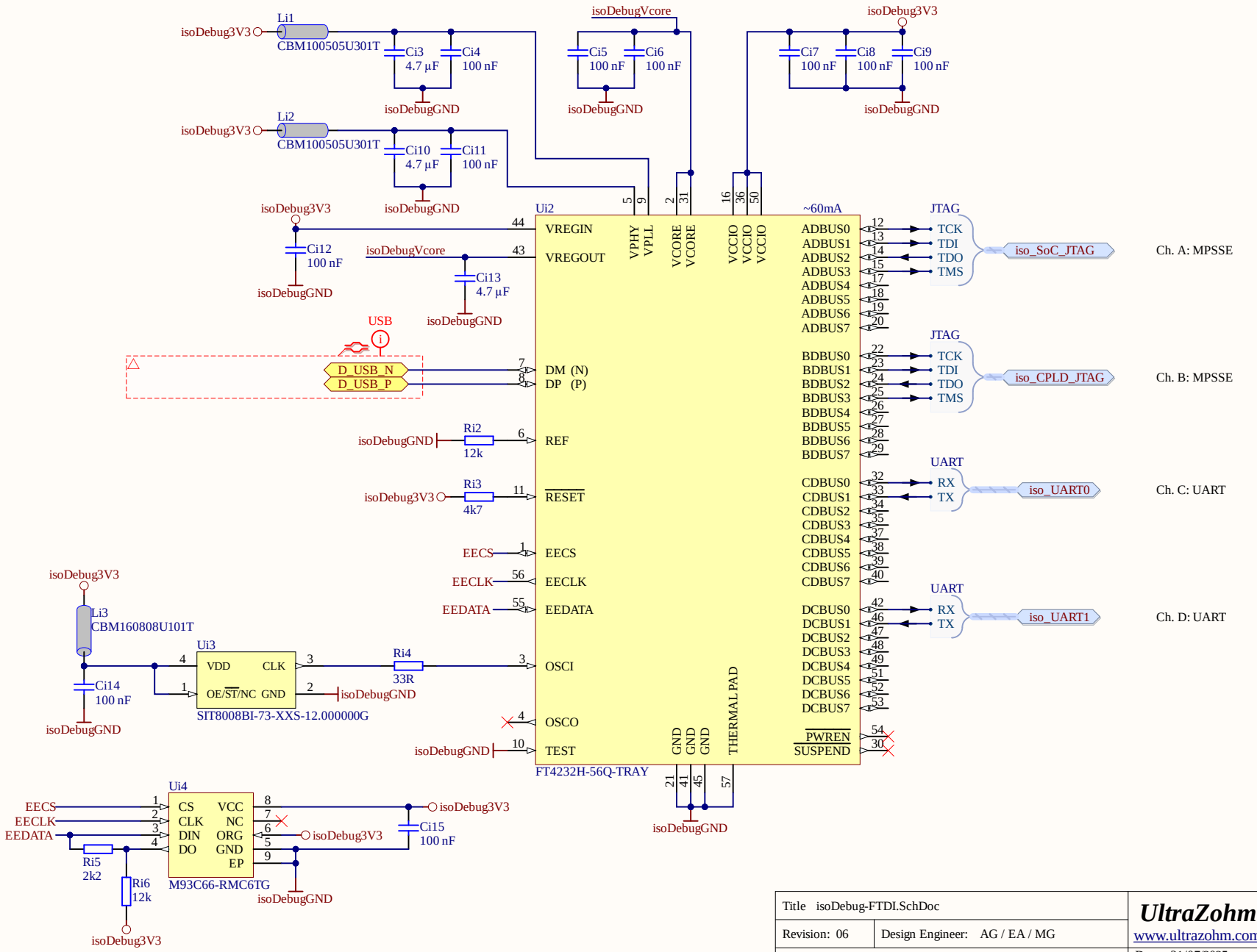
Unused FlexMIOs can be used as (S³C/PS/PL-)GPIOs.



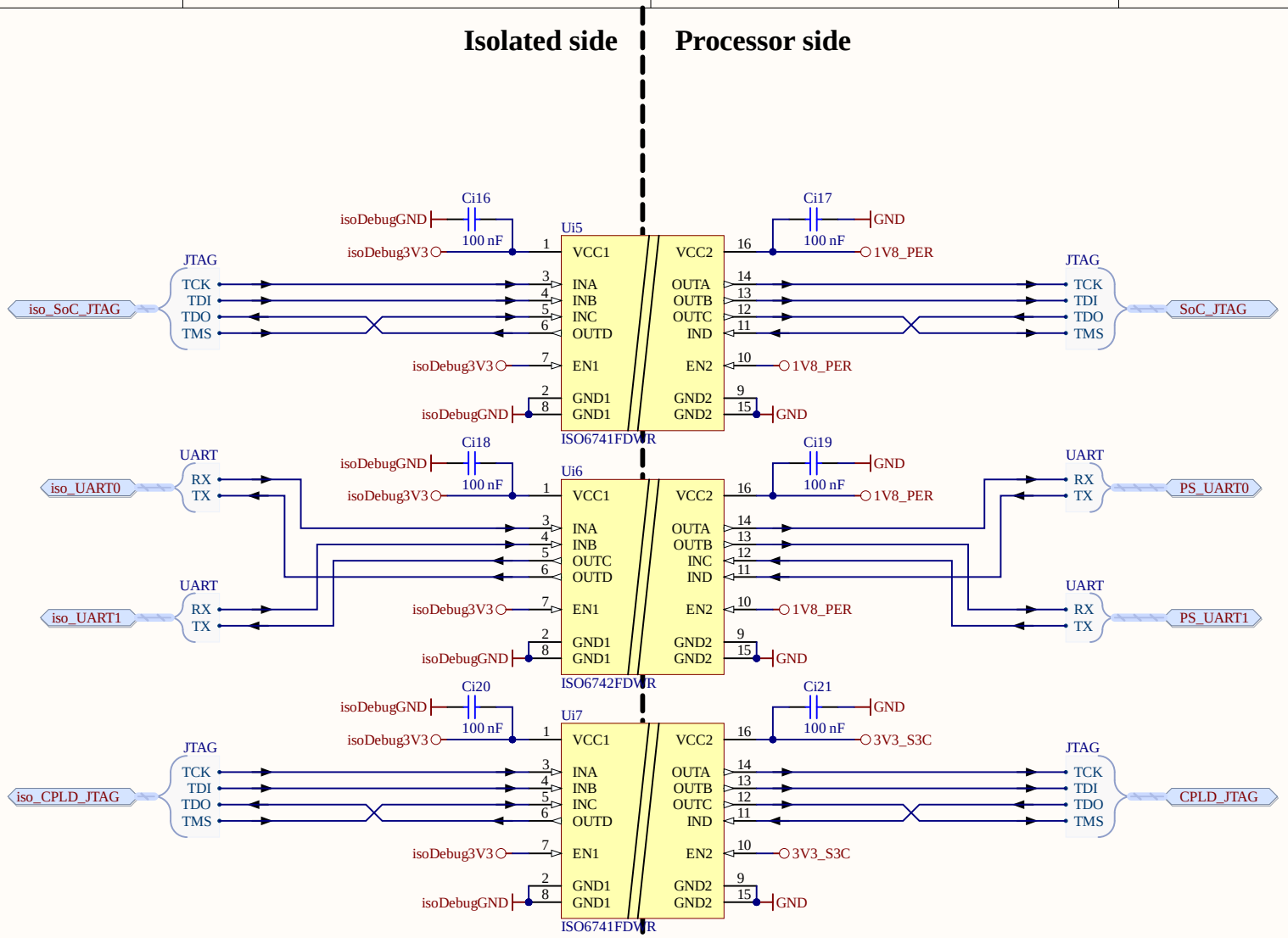
Title Frontpanel.SchDoc		**UltraZohm** www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 32 of 62



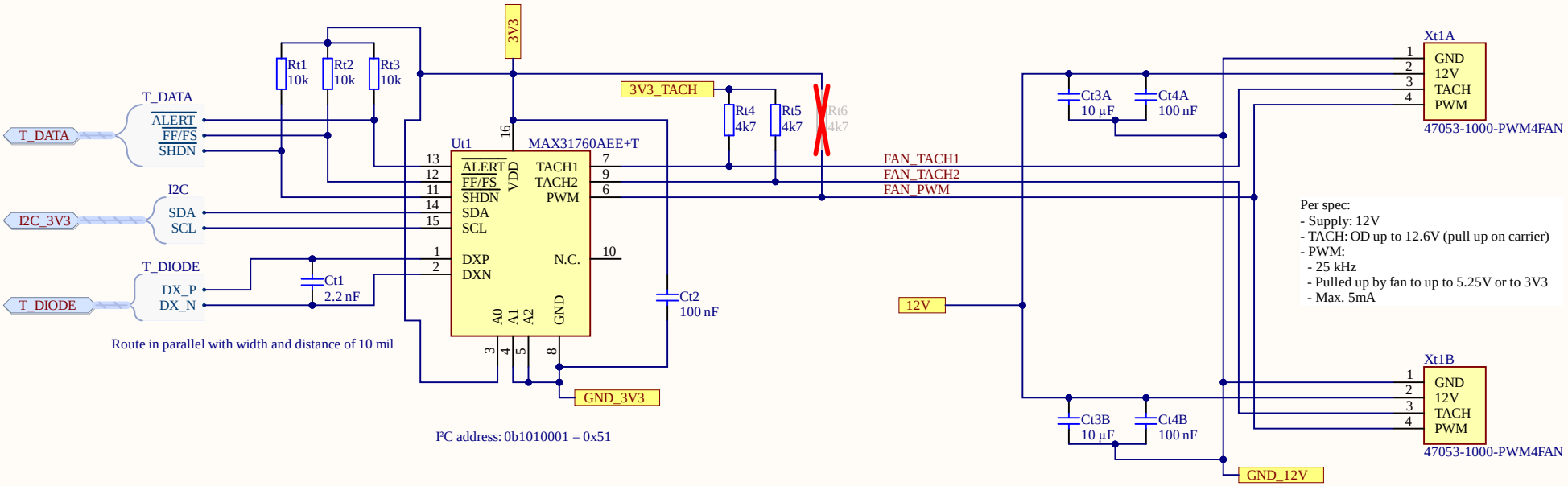
Title isoDebug.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 33 of 62	



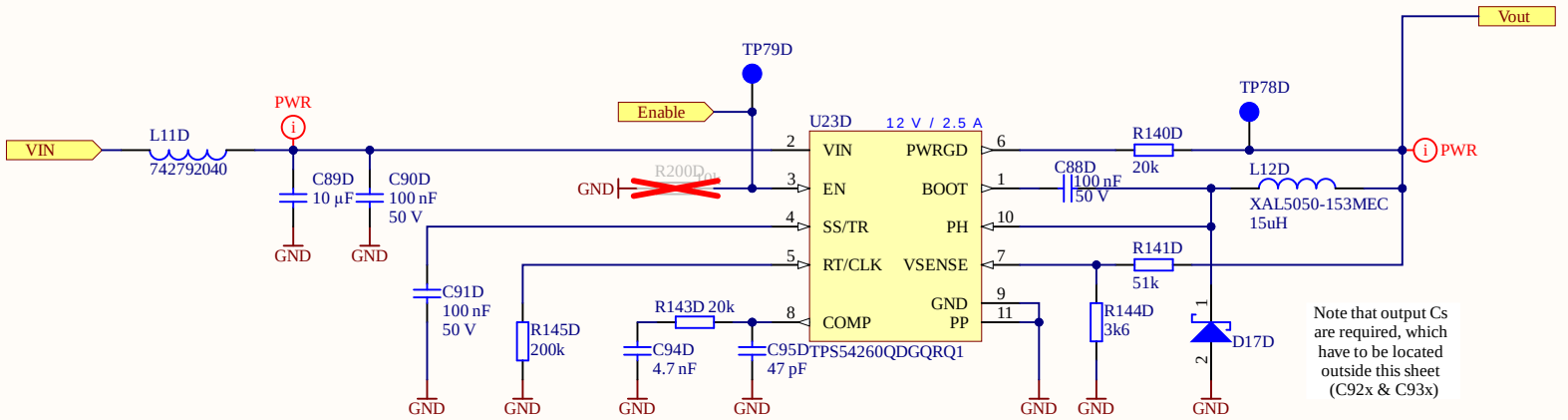
Title isoDebug-FTDI.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 34 of 62	

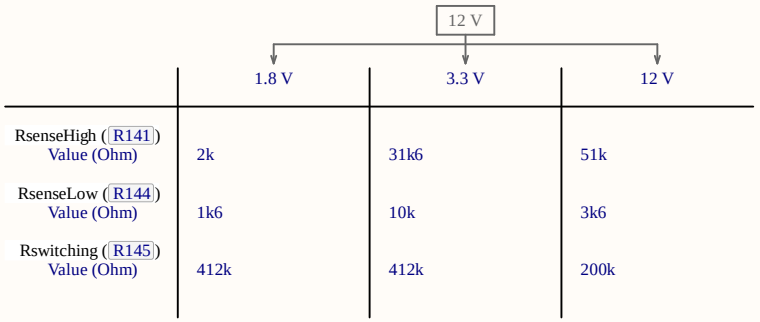


Title isoDebug-Isolation.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 35 of 62	



Title Thermal.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 06	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 36 of 62	

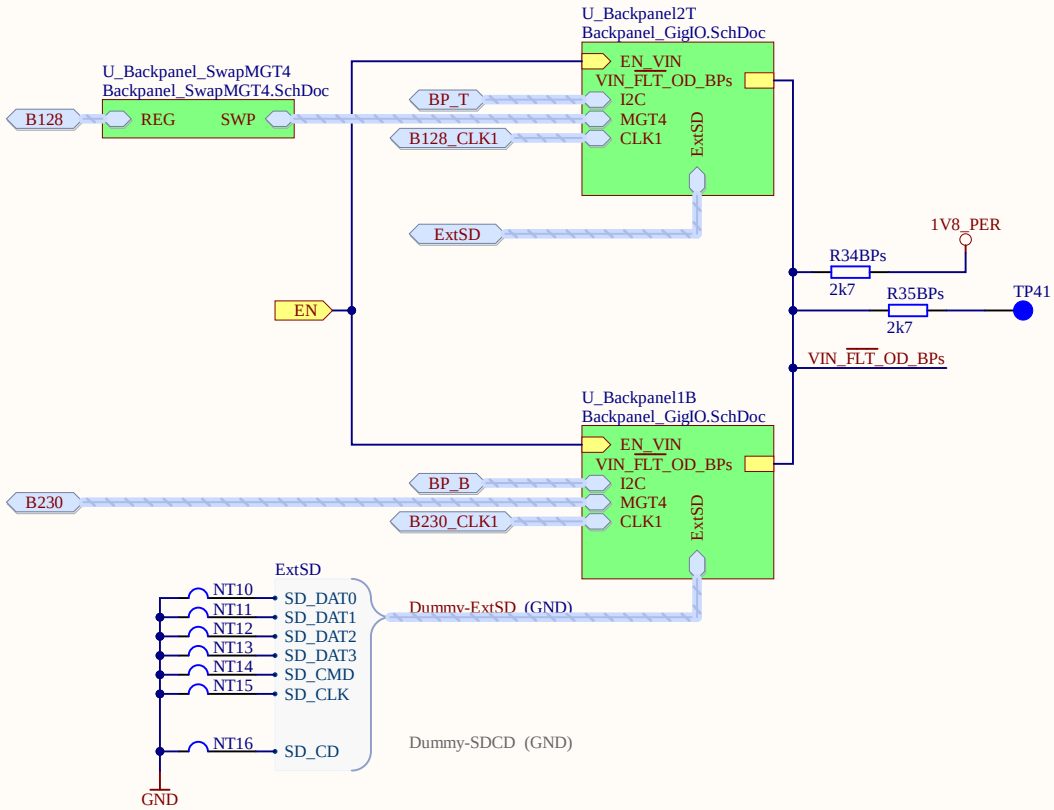




	1.8 V	3.3 V	12 V
RsenseHigh (R141) Value (Ohm)	2k	31k6	51k
RsenseLow (R144) Value (Ohm)	1k6	10k	3k6
Rswitching (R145) Value (Ohm)	412k	412k	200k

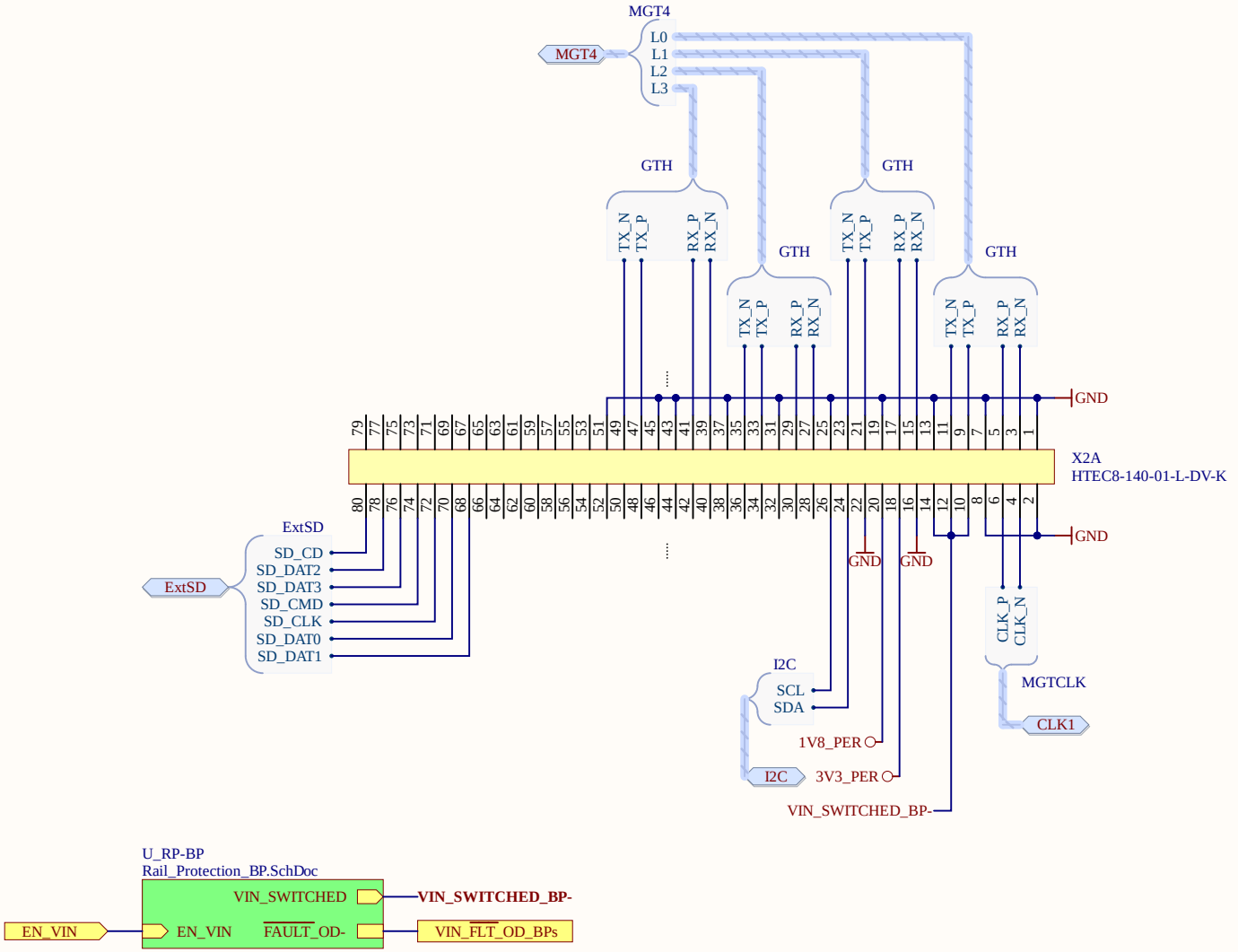
NB: No need to set MPN as parameter!

Title Power_Supply_TPS54260.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 37 of 62

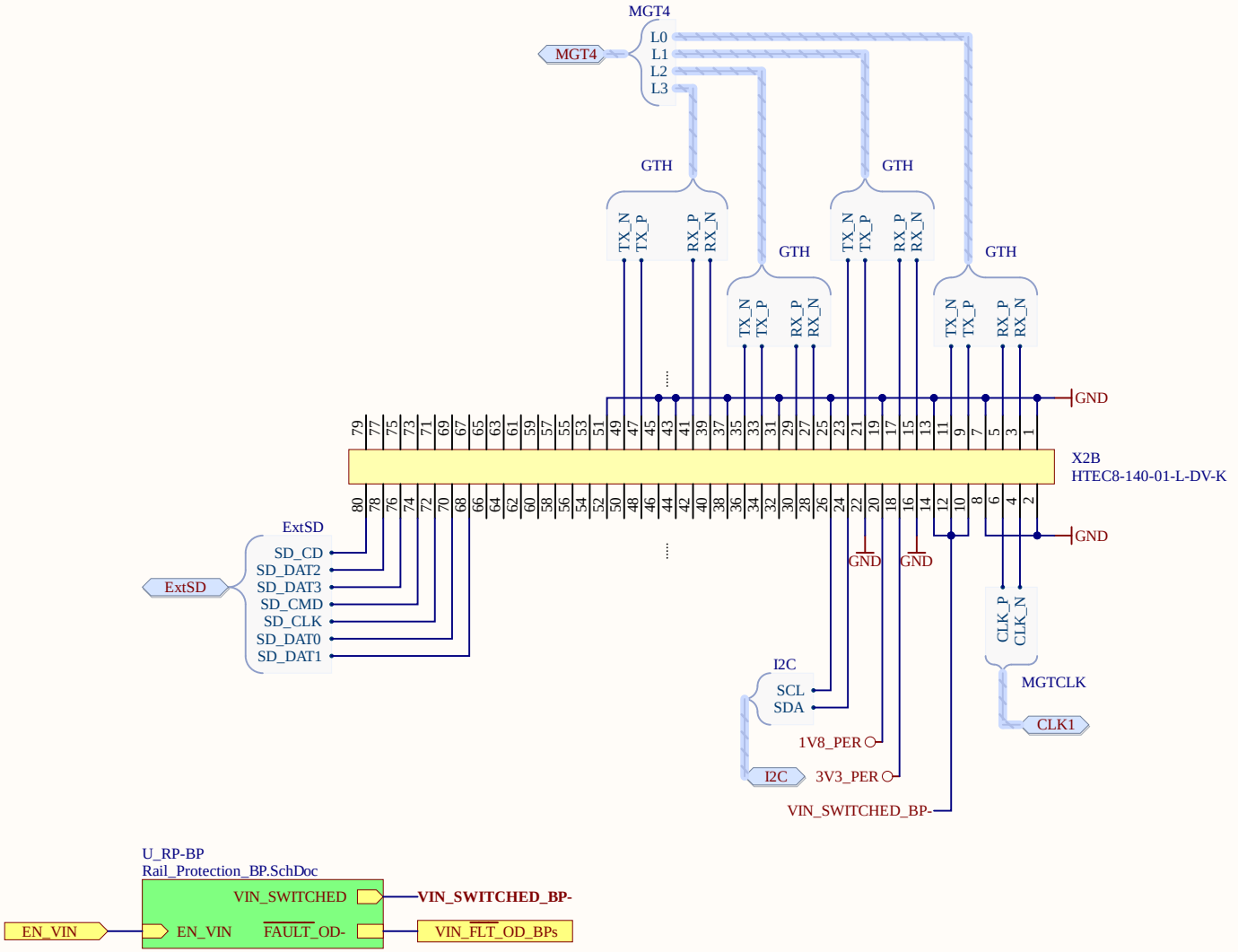


Title Backpanel.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 06	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 38 of 62	

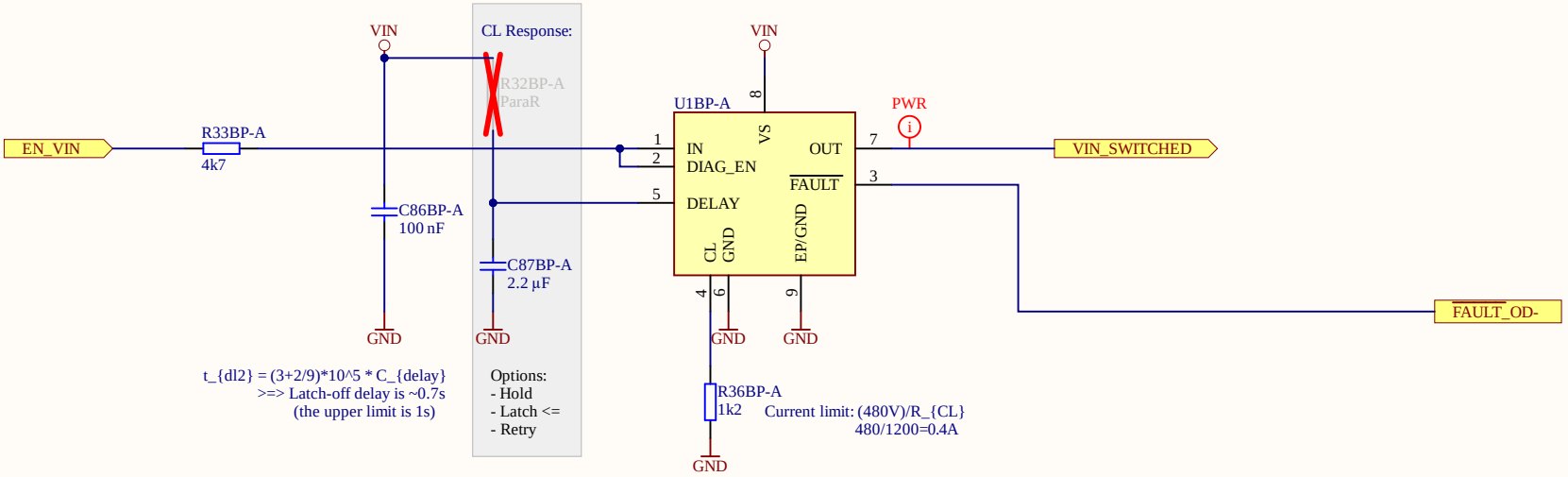
Title Backpanel_SwapMGT4.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 06	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 39 of 62	



Title Backpanel_GigIO.SchDoc		UltraZohm www.ultrazohm.com	
Revision: 06	Design Engineer: AG / EA / MG		
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 40.1of 62	

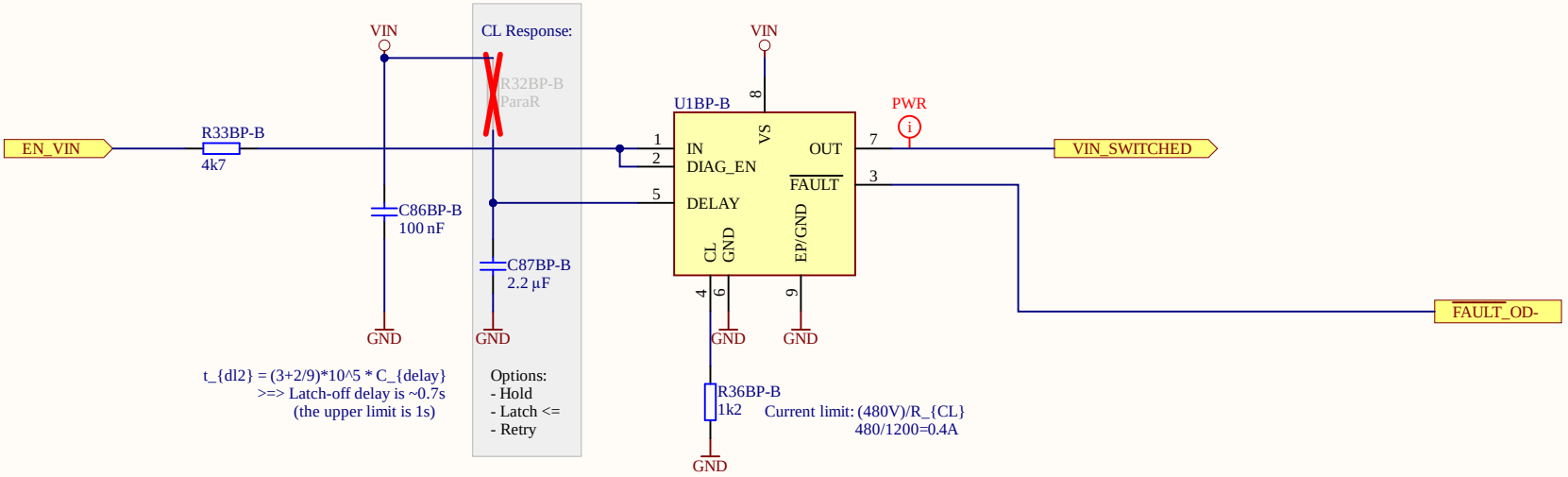


Title Backpanel_GigIO.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 40.2 of 62	



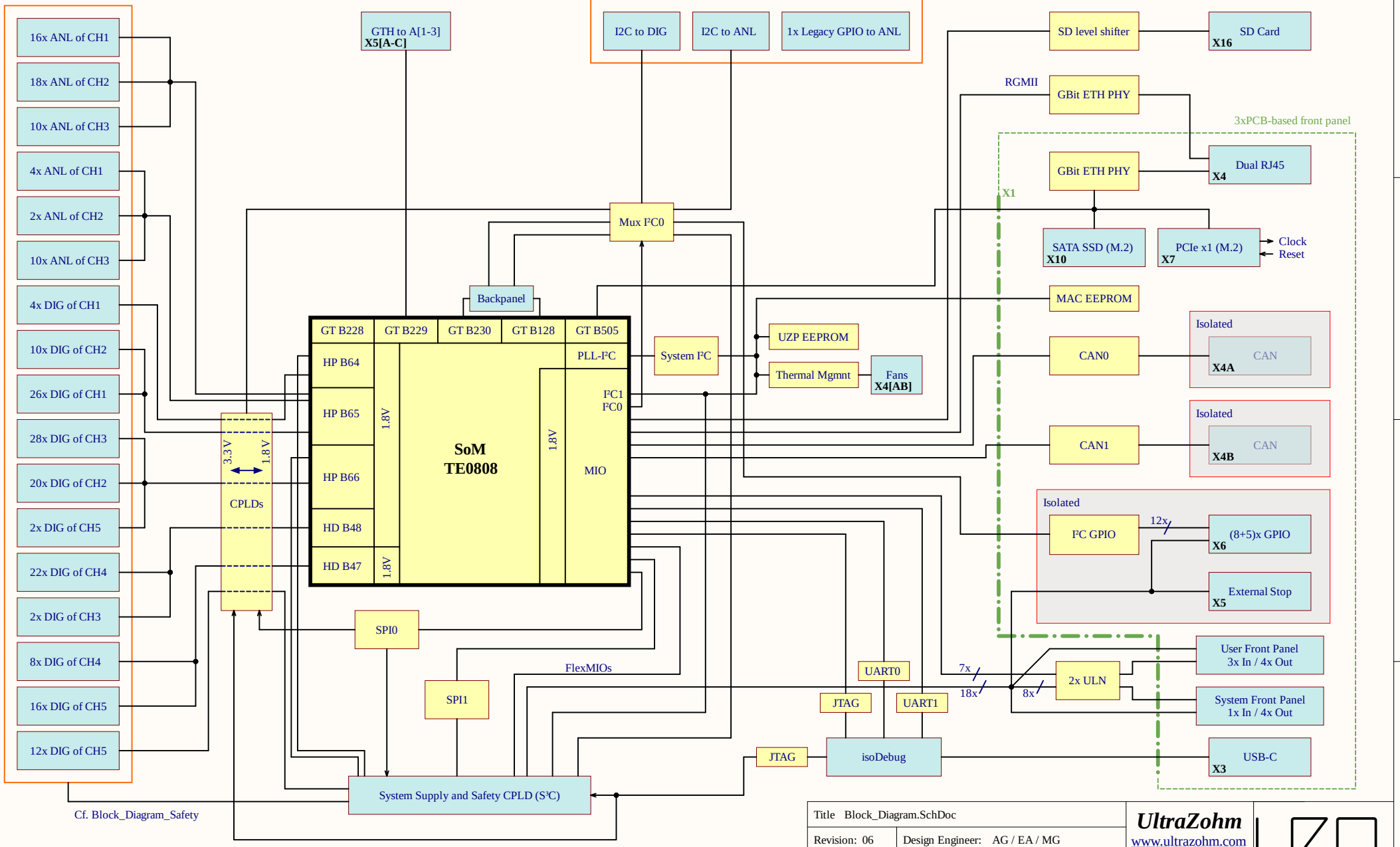
I(off) is in the µA range if IN=DIAG_EN=0

Title Rail_Protection_BP.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 40 of 62	



I(off) is in the µA range if IN=DIAG_EN=0

Title Rail_Protection_BP.SchDoc		UltraZohm	
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025	
		Sheet 40 of 62	



Title Block_Diagram.SchDoc		**UltraZohm**
Revision: 06	Design Engineer: AG / EA / MG	www.ultrazohm.com
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025
		Sheet 41 of 62

Conceptual name:	Type:	Signal source -> sink:	Voltage:	Signal path/name:
5x Output_Enable (PILOT_OUT)	Per-Dx	S³C -> Slot-Conn.	3V3	DIG_S3C.SlotDi.SlotOE
1x FLT (Safe State Request; e.g., External Stop)	Shared	S³C -> Slot-Ctrl.	1V8	DIG_S3C.Shared.ReqSafeState
1x CarrierRdy	Shared	S³C -> Slot-Ctrl.	1V8	DIG_S3C.Shared.CarrierReady
5x !FLT	Per-Dx	Slot-Ctrl. -> S³C	1V8	DIG_S3C.SlotDi.SlotOK
5x OE	Per-Dx	Slot-Ctrl. -> S³C	1V8	DIG_S3C.SlotDi.ReqOE
(PILOT_IN; becomes FLT after fusion in slot c.)	(Local)	Slot-Conn. -> Slot-Ctrl.	3V3	(PILOT_INi and /PILOT_INi?)

System Controller (S³C) - The Overview...

- CPLD (Mach XO2): U19G
- Supply (3V3_S3C): U23 C via F2 / D7 or D6
- S³C banks on 3V3: U19A / U19E / U19F
- S³C banks on 1V8: U19B / U19C / U19D

Auxiliary circuitry (for D-slot-shared interfaces):
- JTAG multiplexing between S³C and Dx: Uj1
- CS generation of PS-SPI0 (same targets): U25

Sequencing- and safety-related remarks:
- The card-driven "OK" signal (PILOT_IN) plus the slot controller's internal state (de)assert OE
- The S³C receives 1 OE per slot, ANDs it with its internal state, and sets per-slot "OE"s (_OUT)

Output_Enable (PILOT_OUT)
FLT
CarrierRdy
!FLT
OE

Power Supply Supervisors (Um1 A/B)

External Stop

SoC

D1-Slot Controller
D2-Slot Controller
D3-Slot Controller
D4-Slot Controller
D5-Slot Controller

PILOT_IN
2x
2x
D1-Slot
D2-Slot
D3-Slot
D4-Slot
D5-Slot

Title Block_Diagram_Safety.SchDoc		UltraZohm www.ultrazohm.com
Revision: 06	Design Engineer: AG / EA / MG	
Project: UZ_CarrierBoard.PrjPcb		Date: 31/07/2025 Sheet 42 of 62